UTM
UNIVERSITI TEKNOLOGI MALAYSIA

FACULTY OF COMPUTING
UTM Johor Bahru

SECR 1013: Digital Logic

Semester 01 2024/2025

Network Packet Transmission Monitoring System

PROJECT REPORT

Faculty of Computing

Prepared by

GROUP 2

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1. Introduction

Network Packet Transmission Monitoring System, is a project being developed to replicate a real-world scenario where data packets are being transmitted between computers in two different labs (Lab 1 and Lab 2) over a single cable. The project has been specifically formulated and designed to apply Digital Logic Design and to build a system regulating and monitoring the data packet being passed from one lab to another.

The project uses Deeds, that is, Digital Electronics Education and Design Suite as the primary tool for designing, simulating, and testing the digital logic circuit. Deeds provides a platform for creating and analyzing digital circuits, making it ideal for the simulation of the packet transmission system.

Objectives

1. Design a Synchronous Counter: Design a 3-bit synchronous counter using T flip-flops to count the packets to be sent.

2. Packet Routing: Use an 8-1 MUX to select a source computer from Lab 1 and another 1-8 DEMUX to route the received data to the destination computer.

3. Packet Transfer Monitoring: Implement a monitoring mechanism to monitor the status of packet transmission and error detection.

4. Error Detection: Design a method of error prevention, such as an interrupt signal (PPM) when either there is a power failure, the counter is not functioning, or MUX/DEMUX malfunctions.

5. System Simulation: Use Deeds to simulate the digital logic circuits to see the system working properly.

With the completion of this exercise, it is hoped that all participants will have attained a high level of understanding of digital logic design, synchronous counters, multiplexers, demultiplexers, and error detection methods Some of the components of the project seem to have an interesting practical side in terms of application.

Objective of the project: How to simulate a Network Packet Transmission System.

2. Problem Background

This section of the project report provides an overview of the underlying issues or challenges within the current system that prompted the need for the project.

• A group of computers in Lab 1 are connected to a group of computers in Lab 2 via one cable.

• We want to transmit a number of packet data (defined from user) from one source computer in Lab 1 to another destination computer in Lab 2.

2.1 Challenges

1. **Project Complexity:** Understanding and implementing the MUX, DEMUX, T flip-flops, and comparators together to make the system.
2. **Accurate Packet Counting:** Designing a synchronous counter that stops automatically upon reaching the appropriate packet count without recycling the counter.
3. **Clock Enabler:** Implementing a verification device by using other components as an input.
4. **Data Sync:** Ensuring that the packet delivery from Lab 1 to Lab 2 is synchronized with the counter.

2.2 Importance of the Project

This project has a practical aspect as it tries to solve an actual problem by putting into practice concepts learned in digital logic design. In this case, the real system is modeled. Through this experience, we gained valuable insights into the complexities of digital system design and improved our problem-solving skills, preparing us for future challenges in the field.

3. **Suggested Solution**

System Overview:Data transfer is accomplished through multiplexing and demultiplexing. These units route information from computers in Lab 1 to Lab 2 during the positive edge of the clock for synchronized, serial transfer.

To supervise data transfer is carried out with the help of a comparator that checks the current data count against a preset maximum value to keep data transfer down to size. This ensures the operation stays within the determined boundaries and that no overflow or inaccuracies take place.

A synchronous 3-bit counter is employed to count the data packets being transmitted. It integrates seamlessly with the file transfer system and provides an accurate method to track the transfer's progress. As a control mechanism, the clock enables and disables the counter according to specified requirements, like system readiness, valid input parameters, and security. Taken together, all components constitute a data transfer system that is efficiently in place and under control.

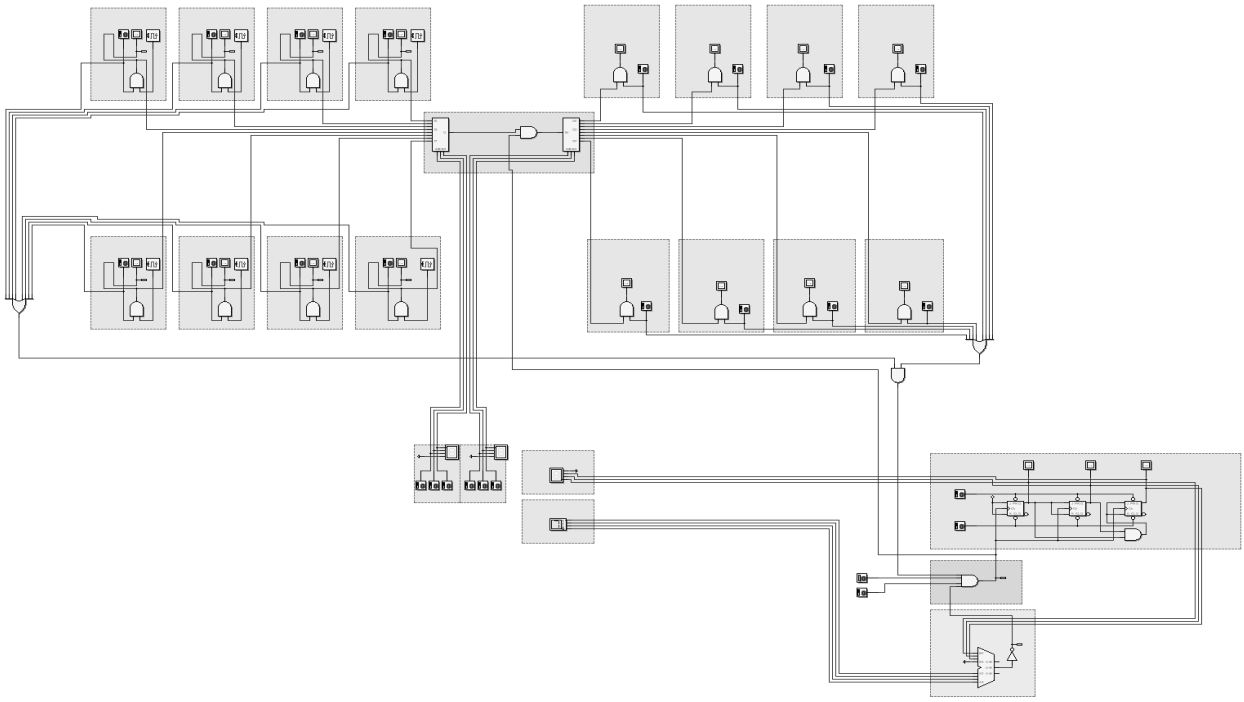


Figure 3.1: Complete Circuit (Basic Functions)

3.1 Component Explanations

1. 8-to-1 MUX (Multiplexer):
    - Selects one of the 8 source computers in Lab 1 to transmit data. It
    - uses 3 select lines to choose the source computer.
2. 1-to-8 DEMUX (Demultiplexer):
    - Routes the transmitted data to one of the 8 destination computers in Lab 2.
    - It uses the same 3 select lines as the MUX to ensure data is sent to the correct destination.
3. Synchronous Counter:
    - Counts the number of packets transmitted using T flip-flops.
    - Stops counting when the maximum packet count is reached (saturated counter).
4. Comparator:
    - Compare the current packet count with the maximum packet count.
    - Stop the counter when the counts match.
5. Clock Enabler:
    - Controls the clock signal to the counter.
    - Disables the clock when the counter reaches the maximum value.
6. Monitoring System:
    - Tracks the status of packet transfer (e.g., power ON, counter status).
    - Detects and reports faults (e.g., power failure, counter malfunction).

3.2 How It Works

1. Packet Transmission:
    - The MUX selects a source computer in Lab 1, and the DEMUX routes the data to a destination computer in Lab 2.
2. Packet Counting:
    - The synchronous counter increments with each packet transmitted.
3. Stopping the Counter:
    - The comparator stops the counter when the maximum packet count is reached.

3.3 Suggestions for Project

These are some of the suggestions that are recommended for the project that we implemented

Suggestions for project complexity: Before starting the implementation, our group conducted a comprehensive research and analysis phase to address the project's complexity. Understanding how the different parts work together to form a working system that can send data and efficiently monitor it using a counter and clock enabler was the first difficulty. We started by creating a simple model, which gave us important information about how the system functions. It was much simpler to move forward with the creation of the advanced features and accomplish a successful project execution thanks to this fundamental understanding.

Suggestions Clock Enabler: The clock enabler acts like a gateway, allowing the counter to start only when certain conditions are met. We designed it using an AND gate, which is connected to the power supply, the system clock, and a comparator. The comparator helps limit data by checking the current packet count against the maximum set value. Later on, we added a more advanced feature: password protection. With this in place, the clock enabler only activates when the correct password is entered. This added an extra layer of security and ensured that the system could only be accessed by authorized users.

Suggestions for Accurate Packet Counting: To make sure the packet counting was accurate, we needed to figure out how to connect the computers' input signals to the counter. We solved this by using the clock enabler, where the input signal became one of the conditions for activating the counter. This approach worked well and helped us ensure accurate counting of packets. Even after that, we had to deal with another challenge—syncing the data transfers with the counter. It took some extra effort to align everything so that the counter and data transfers worked smoothly together, but it was worth it to get the system running accurately.

Suggestions for Data Sync: To make sure the data stayed in sync, we connected the coaxial cable from the MUX and DEMUX to one input of an AND gate. Then we connected the other input of the AND gate to the clock enabler. This setup worked well to keep the data transfers and the system's operations synchronized, ensuring everything ran smoothly.

3.4 Advanced Features

We added these advanced features mentioned below later on:

1. Full Duplex:
We also provided full-duplex communication, wherein data packets may be transmitted and received between the source and destination computers simultaneously. That gave a big boost to the efficiency and improvement of the whole system because both directions can communicate without any hesitation

2. Password Protection:
For security purposes, we included a password authentication mechanism in the system. It will prompt users to enter a predefined password before the actual process of packet transmission starts. The comparator compares the input given by the user with the stored one, and if correct, the clock enabler starts the transmission process. This ensures that the system will only operate when authorized people want to use it; otherwise, there is no other means to enable the controlling operations.

3. Fault Detection:
A system monitoring system was developed to identify any potential component errors within the framework. This system detects two main operational problems as well as counter malfunctions and MUX/DEMUX module defects. When the system detects failures it creates either an interrupt signal (PPM) or an error code. Additional facilities on the monitoring dashboard display error alerts which enable immediate administrative response and maintenance activities. Through its fault detection system the system increases its reliability by finding and resolving problems fast which prevents performance disturbances during packet transfers.

4. System Requirements

This section outlines the hardware, software, functional, and non-functional requirements necessary for the development, deployment, and operation of the system. It ensures users understand the minimum and recommended configurations.

4.1 Hardware Requirements

The hardware requirements for the Network Packet Transmission Monitoring System include the components needed to design and simulate the digital logic circuit. These are:

1. Basic Components:
    - T Flip-Flops: For designing the synchronous counter.
    - MUX (8-to-1): To select one of the 8 source computers in Lab 1.
    - DEMUX (1-to-8): To route data to one of the 8 destination computers in Lab 2.
    - Logic Gates: AND, OR, NOT, XOR, and XNOR gates for designing the comparator, clock enabler, and error detection system.
    - Input Switches: To simulate user inputs (e.g., power ON, start button, maximum packet count).
    - Output Displays: To show the current count, packet transfer status, and error codes.
2. Additional Components:
    - Clock Source: To provide the clock signal for the synchronous counter.
    - Push Buttons: For resetting the counter and manually controlling the clock.

4.2 Software Requirements

The software requirements include the tools and platforms needed to design, simulate, and test the circuit:

1. Deeds (Digital Electronics Education and Design Suite):
    - Used for designing and simulating the digital logic circuit.
    - Provides a user-friendly interface for creating and testing circuits.
2. Documentation Tools:
    - Google Docs: For writing the project report.
    - Canva: For creating the project presentation.
3. Video Recording Software:
    - Tools like OBS Studio for recording the demo video.
4. Online Platforms:
    - YouTube: For publishing the demo video (unlisted link).
    - E-Learning Platform: For submitting the project report, presentation, and Deeds circuit file.

4.3 Functional Requirements

The functional requirements describe what the system should do:

1. Packet Transmission:
    - Transmit data packets from a source computer in Lab 1 to a destination computer in Lab 2.
2. Packet Counting:
    - Use a synchronous counter to count the number of packets transmitted.
    - Stop counting when the maximum packet count is reached.
3. Fault Detection:
    - Detects and reports errors such as power failure, counter malfunction, or MUX/DEMUX faults.
4. Monitoring:
    - Monitor the status of packet transfer (e.g., power ON, counter status).
5. User Control:
    - Allow the user to set the maximum packet count, start/stop the transmission, and reset the system.

4.4 Non-Functional Requirements

The non-functional requirements describe how the system should perform:

1. Reliability:
    - The system should accurately count packets and detect faults without errors.
2. Performance:
    - The circuit should operate efficiently, with minimal delay in packet transmission and fault detection.
3. Usability:
    - The system should be easy to use, with clear input controls and output displays.
4. Scalability:
    - The design should be scalable to support more computers or larger packet sizes if needed.
5. Maintainability:
    - The circuit design should be modular and easy to modify or debug.

5. System Implementation

This section outlines the successful system that has been implemented. It highlights all the main functions and components of the system which is the Computer, Mux/Demux Connection, 3-Bit Up Counter, Clock Enabler, Comparator, Password Module, Fault Detection system and The Dashboard.

5.1 Computer

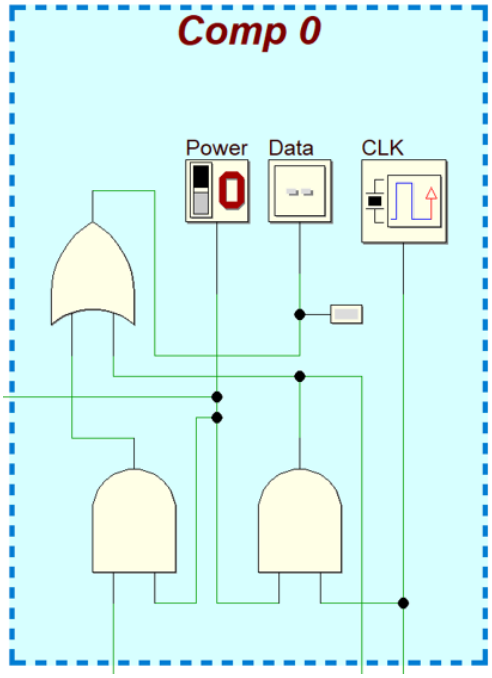


Figure 5.1 : Computer 0

The computer system includes a power button, a clock, a data monitor panel (with a one-bit output), two AND gates, and an OR gate. The computer is turned ON when the user sets the power to HIGH. Data becomes available when the clock detects a positive edge, and it can be monitored through the one-bit output on the data monitor panel. Data can be sent by triggering the clock in the "SEND DATA" section. The two AND gates ensure that data is sent to the OR gate only when the power is HIGH, as one input of each AND gate is connected to the power source. The OR gate receives input either from the Demux or the Clock, and the resulting output can be observed on the one-bit data monitor panel.

5.2 Mux/Demux Connection

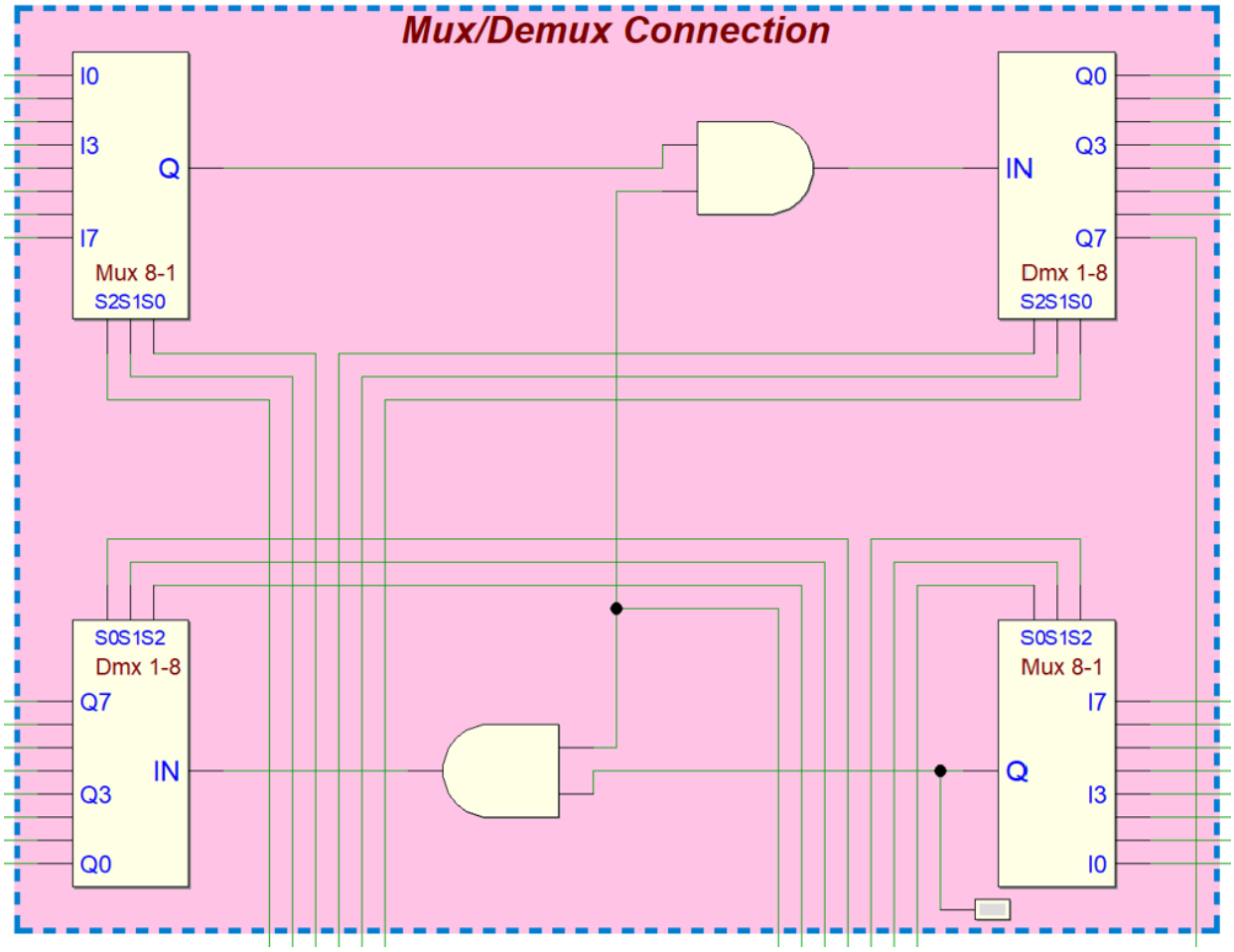


Figure 5.2 : Mux/Demux Connection Circuit

The Mux/Demux connection is responsible for routing received data to the appropriate destination. In this system, an 8-to-1 multiplexer (Mux) is used for data selection, while a 1-to-8 demultiplexer (Demux) handles data distribution. These components were chosen because the system includes only 8 computers in each of the two labs. To achieve full-duplex communication—allowing data transfer in both directions—2 Mux and 2 Demux are implemented. Additionally, the Mux and Demux rely on receiving a clock pulse from the Clock enabler to function, which is facilitated by the use of an AND gate.

5.3 3-Bit Up Counter

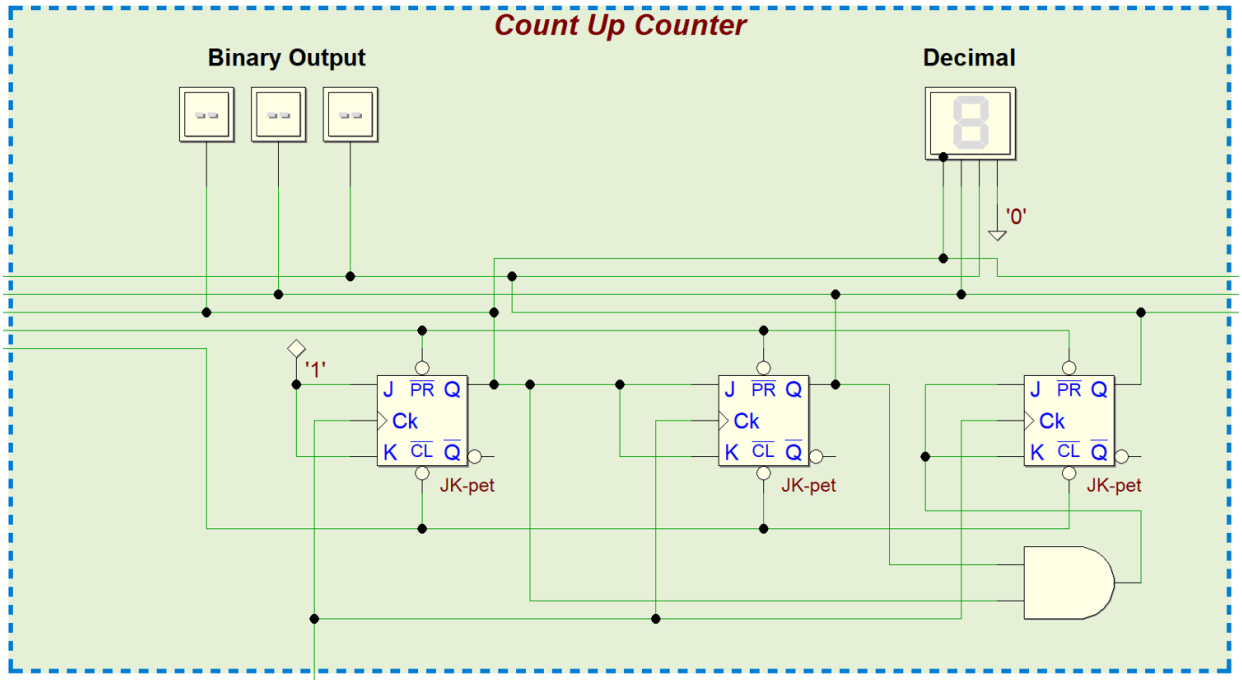


Figure 5.3: 3 Bit Synchronous up Counter circuit

The 3-bit counter that we use is a 3-bit T positive edge count-up counter. The counter would start to count when the synchronous clock is enabled. It will start counting when the clock pulse is sent. In our project, The pulses are sent when the user clicks the clock in the send data section and all of the clock enabler rules are satisfied. The counter will also display the current data sent in decimal and binary format.

5.4 Clock Enabler

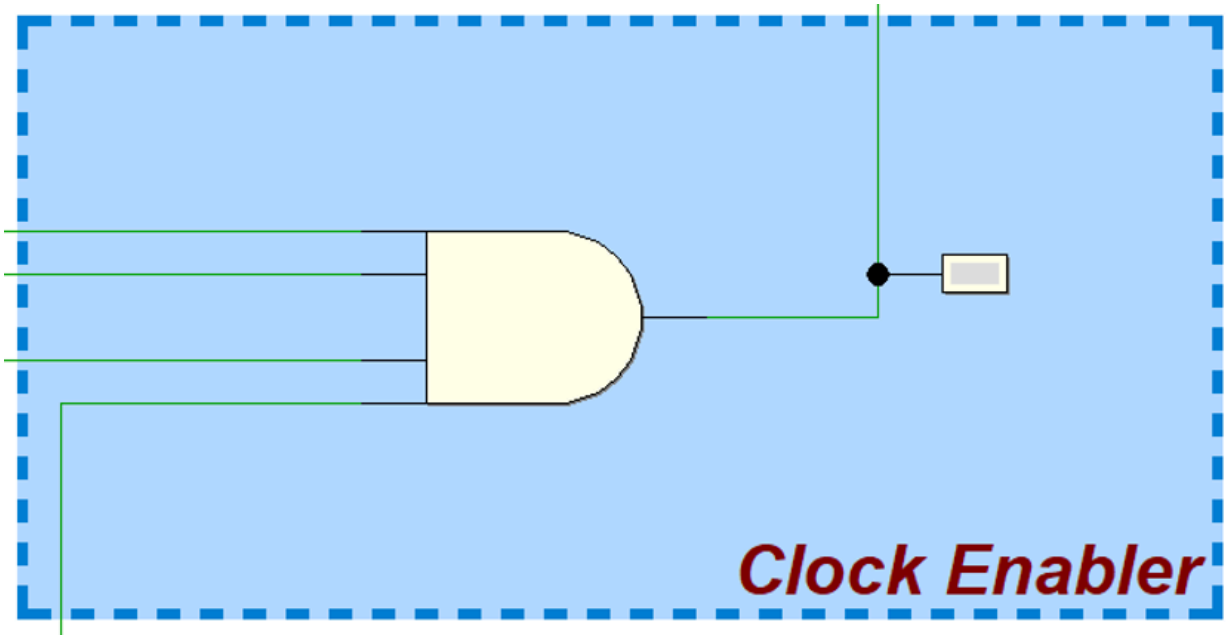


Figure 5.4: Clock Enabler Circuit

The clock enabler is a 4-input AND gate that generates a clock pulse only when all specified conditions are met. These conditions include: both the sending and receiving computers must be turned on, the data being sent must not exceed its limit, the password module must be verified as correct, and the user must click the clock in the "SEND DATA" section. Once all these requirements are satisfied, the clock enabler sends a clock pulse to the counter, allowing data transmission to proceed.

5.5 Comparator

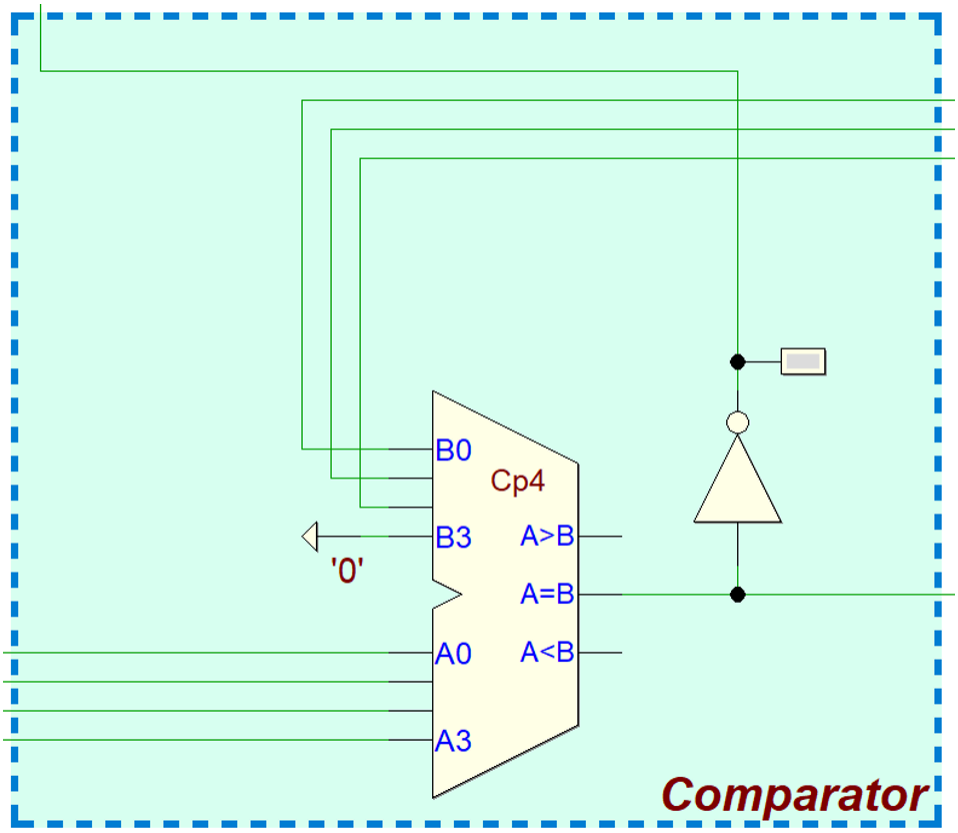


Figure 5.5: Comparator Circuit

The comparator is a system designed to disable the clock enabler when the total data sent equals the maximum data limit set by the user. Initially, the comparator's output is LOW, which passes through an inverter and becomes HIGH, enabling the clock enabler to function since all its inputs are HIGH. However, when the total data sent matches the user-defined maximum limit, the comparator's output switches to HIGH. This HIGH output passes through the inverter, becoming LOW, which disables the clock enabler and stops the counter from operating, effectively halting data transmission.

5.6 Password Module

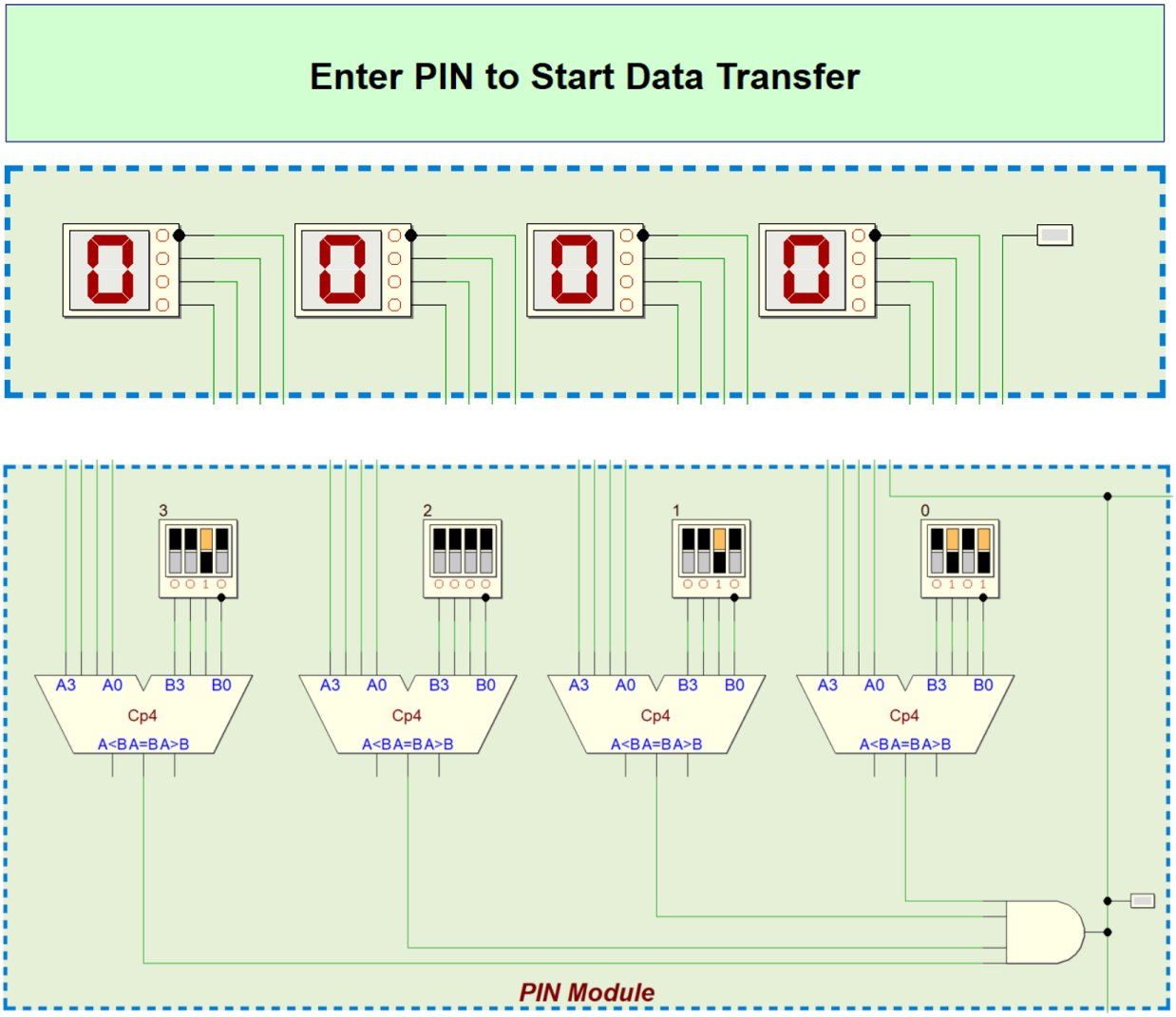


Figure 5.6: Password Module

The password module adds a layer of security to the system. It works by checking a 4-digit password before enabling the clock. Each digit of the password is compared using four comparators, and all the results go through an AND gate. If all the digits match, the clock is enabled; if not, the system stays locked. It's a simple yet effective way to keep the system secure.

5.7 Fault Detection System

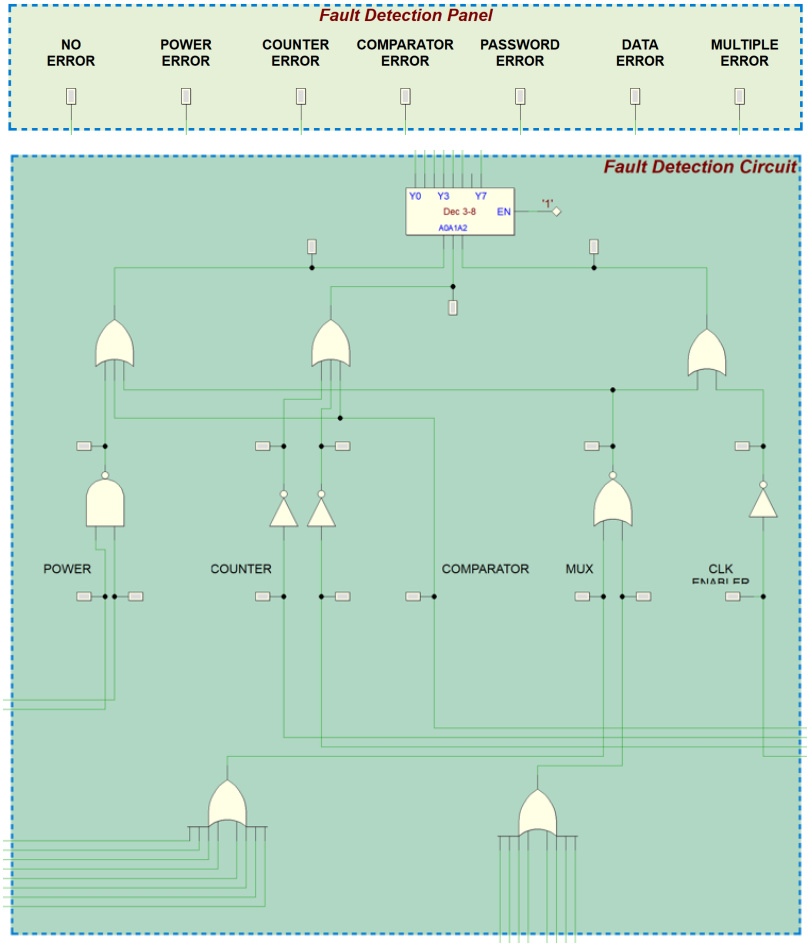


Figure 5.7: Fault Detection Circuit

The fault detection circuit is designed to identify and report errors when the system encounters issues, with six types of errors: Power Error, Counter Error, Comparator Error, Password Error, Data Error, and Multiple Error. Each error is assigned a unique code for easy identification. The **Power Error (001)** is activated if the power on both computers is not set to HIGH, while the **Counter Error (010)** is triggered if the "present" and "clear" buttons are not HIGH. The **Comparator Error (011)** occurs when the data sent matches the maximum data limit set by the user, and the **Password Error (100)** is activated if the user-entered password does not match the PIN module. The **Data Error (101)** is triggered if the clock (CLK) in the selected computer is not at a positive edge, as this prevents data from being sent. Finally, the **Multiple Error (111)** is activated when multiple errors are detected simultaneously. This system ensures efficient fault detection and helps streamline troubleshooting and maintenance.

5.8 The Dashboard

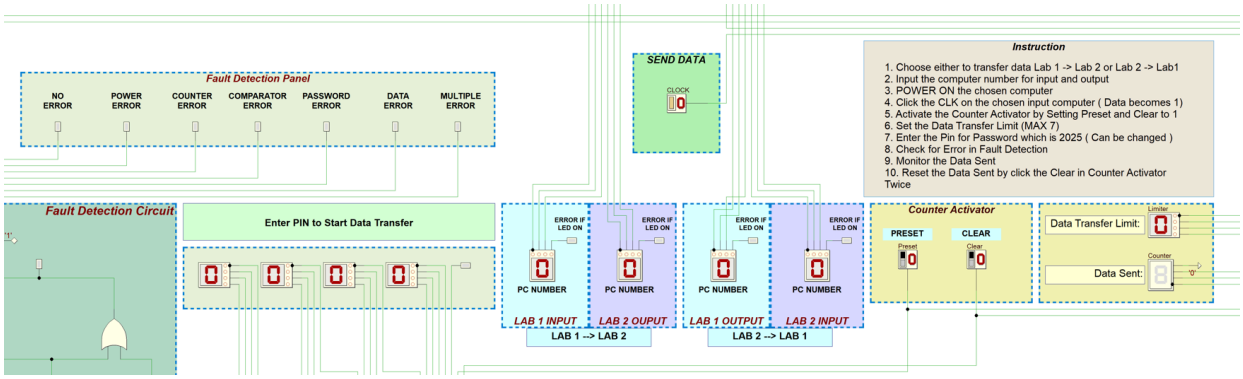


Figure 5.8: Dashboard

The dashboard serves as the central hub of the system, integrating all its functionalities. It allows users to select the source computer for data transmission and specify the destination. Additionally, users can define data transmission limits and monitor the amount of data sent in real-time. The dashboard also provides options to reset the system by pre-setting or clearing the counter as needed. Furthermore, it features a fault detection display that promptly notifies users of any system errors, ensuring comprehensive control and efficient operation.

6. Simulation and Results

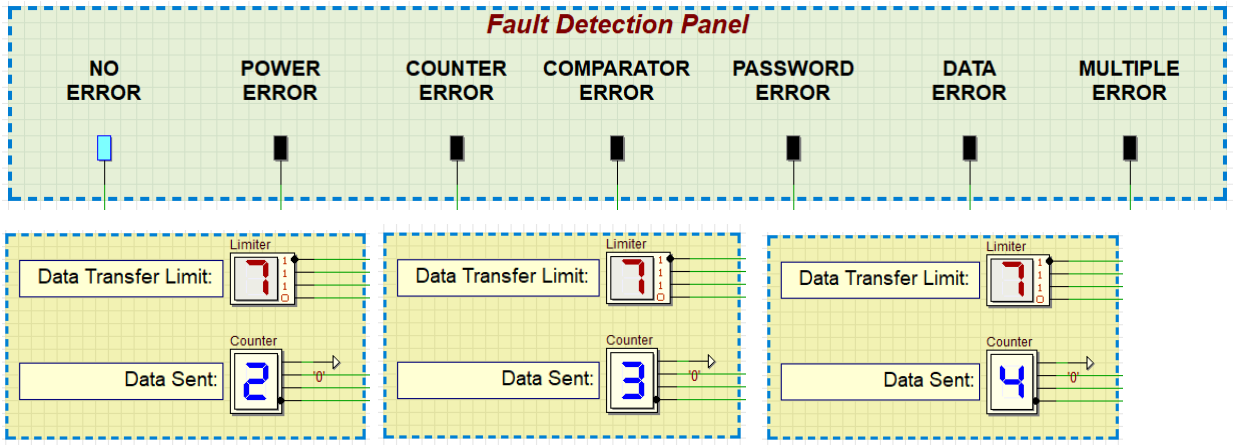
This section covers the simulations run to test the system's performance. The results showed that the system successfully transferred data and detected errors like Power, Data, and Multiple Errors. Overall, the system worked as expected, handling data and errors effectively.

6.1 Successful Simulation

A successful simulation can be achieved if the instructions in the system are followed step by step, as outlined below:

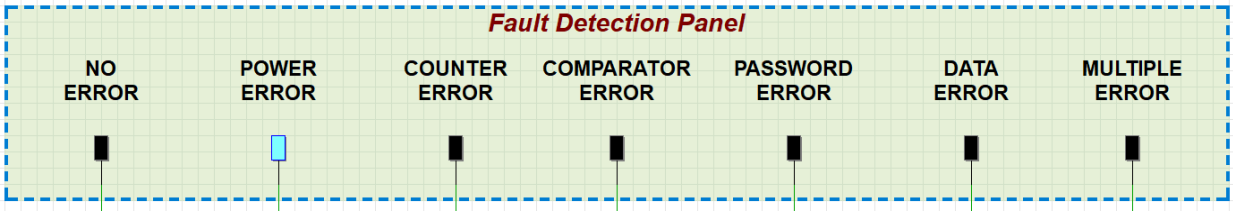
1. Choose either to transfer data Lab 1 -> Lab 2 or Lab 2 -> Lab1
2. Input the computer number for input and output
3. POWER ON the chosen computer
4. Click the CLK on the chosen input computer (Data becomes 1)
5. Activate the Counter Activator by Setting Preset and Clear to 1
6. Set the Data Transfer Limit (MAX 7)
7. Enter the PIN for Password which is 2025 (Can be changed)
8. Check for Errors in Fault Detection
9. Start Sending Data by clicking the Clock in SEND DATA
10. Monitor the Data Sent
11. Reset the Data Sent by click the Clear in Counter Activator Twice

The outcome of the successful simulation is the data will be transferred successfully as shown below:



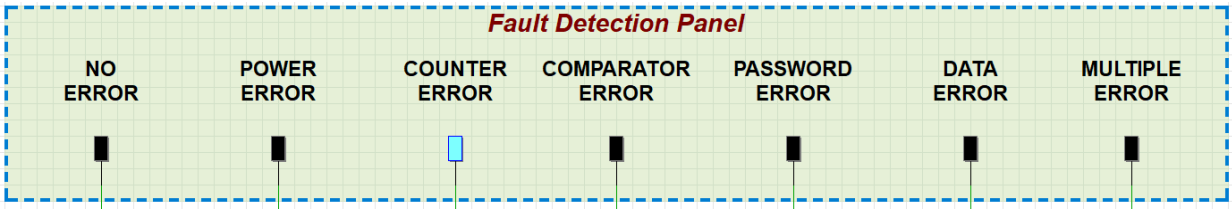
6.2 Power Error

If the user fails to complete step 3, which is changing the Power Switch in the computer section to HIGH, a Power Error will occur. This happens because activating both of the input and output computers is one of the requirements to activate the clock enabler. The outcome of this error will be:



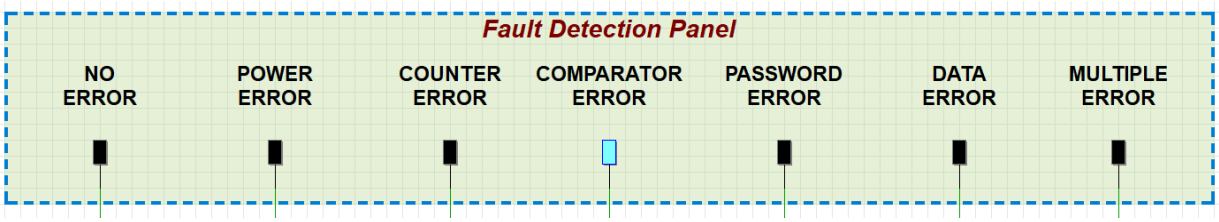
6.3 Counter Error

If the user fails to complete step 5, which is activating the counter activator by setting Preset and Clear to HIGH, a Counter Error will occur. This happens because the counter cannot work if both Preset and Clear are LOW. The outcome of this error will be:



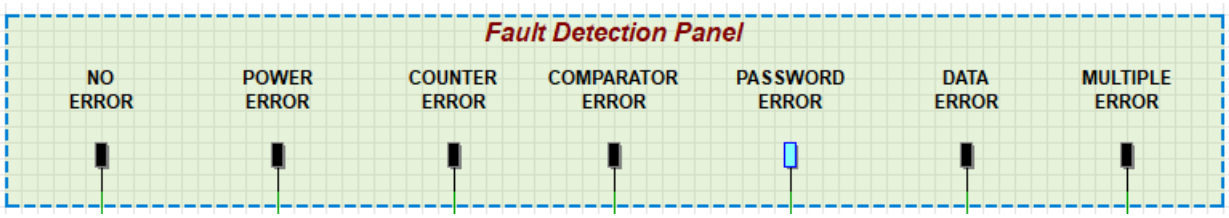
6.4 Comparator Error

If the user fails to complete step 6, which is setting the Data Transfer Limit (MAX 7), a Comparator Error will occur. This happens because one of the inputs in the clock enabler will become LOW if the comparator output A=B becomes 1 . The outcome of this error will be:



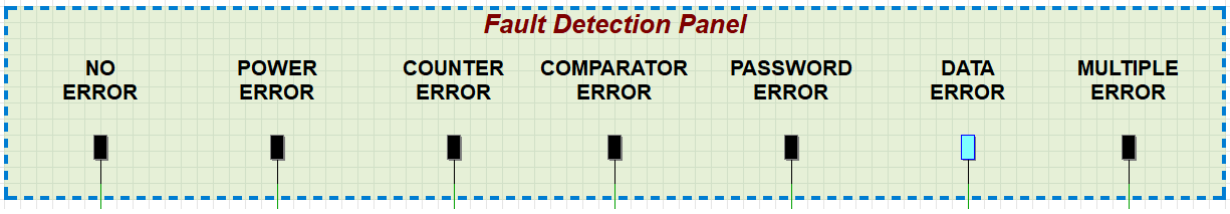
6.5 Password Error

If the user fails to complete step 7, which is entering the correct PIN for Password, a Password Error will occur. This happens because entering the right PIN is one of the requirements to activate the clock enabler. The outcome of this error will be:



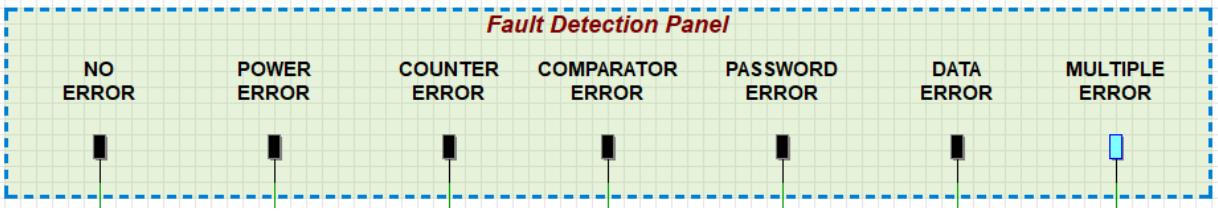
6.6 Data Error

If the user fails to complete step 4, which is changing the CLK (clock) of the computer to HIGH, a Data Error will occur. This happens because when the CLK on the computer is LOW, the system cannot trigger a positive-edge clock pulse, and therefore, no data will be generated or sent to the other lab. The outcome of this error will be:



6.7 Multiple Error

If the user fails to complete multiple steps, all types of errors will be detected, resulting in the activation of a Multiple Error (coded as 111). This occurs when more than one error is present in the system simultaneously, such as failing to turn on the power, incorrectly setting the clock, or other issues. The outcome of this error will be:



Click the link to see the video demonstration of Simulation and Results:

https://youtu.be/PbhI9_Hu_RI

7. **Conclusion and Reflection**

The Network Packet Transmission Monitoring System project has been a comprehensive and rewarding experience, allowing us to apply the theoretical concepts of digital logic design to a practical, real-world scenario. Through this project, we successfully designed and simulated a system that monitors and regulates data packet transmission between two labs using digital logic components such as multiplexers, demultiplexers, synchronous counters, and comparators. The system also incorporated advanced features like full-duplex communication, password protection, and fault detection, enhancing its functionality and reliability.

The Network Packet Transmission Monitoring System project not only achieved its objectives but also provided valuable insights into the practical application of digital logic concepts. We are also grateful for the guidance and support of our lecturer, Dr. Mohd Foad bin Rohani, whose expertise and encouragement were pivotal in the successful completion of this project. This project has been a significant step in our academic journey, and we look forward to applying the knowledge and skills gained to future endeavors in the field of digital logic and beyond.

In addition to achieving the project's objectives, this experience taught us the importance of teamwork, time management, and adaptability. Working together as a group, we learned to distribute tasks effectively, communicate clearly, and support one another through challenges. The project also highlighted the value of iterative testing and debugging, as we continuously refined our design to ensure accuracy and reliability. These skills will undoubtedly be invaluable as we progress in our academic and professional careers.

Furthermore, the project reinforced the significance of understanding both the theoretical and practical aspects of digital logic design. While the theoretical knowledge provided the foundation, the hands-on implementation allowed us to see how these concepts come to life in a real-world application. This balance between theory and practice has deepened our appreciation for the field and motivated us to explore more complex systems in the future.

Overall, the Network Packet Transmission Monitoring System project has been a transformative experience, equipping us with not only technical skills but also problem-solving abilities and a collaborative mindset. We are proud of what we have accomplished and excited to build upon this foundation in our future projects and studies.

8. References

Deeds Software Documentation:

Deeds (Digital Electronics Education and Design Suite). (n.d.). Retrieved from Deeds Website

This resource was used for designing and simulating the digital logic circuit.

YouTube Videos:

Neso Academy. (2020). *Synchronous Counters*. Retrieved from YouTube

This video explained the workings of synchronous counters and how to design them using flip-flops.

Project Guidelines:

Dr. Mohd Foad Rohani. (2024). *Project Digital Logic 2024/2025-1: Network Packet Transmission Monitoring System*.

The project guidelines provided by the lecturer were used to define the scope and requirements of the project.

Digital logic book

Chapter 6: Function of Combinational Logic

Chapter 7: Latches and Flip-Flops

Chapter 8: Counters

University Resources:

Universiti Teknologi Malaysia (UTM). (2024). *Digital Logic Design Lab Manual*.

The lab manual provided guidelines and inspiration for the project design and implementation.

Click the link to see the Presentation Video:
https://youtu.be/JScsWvTmws0

Click the link to see the video demonstration of Simulation and Results:
https://youtu.be/Pbhl9_Hu_RI

Additional challenges

1. Setup times that fit everyone for meetings
2. Submit everything to the group on time
3. Understanding the whole project and adding all the features

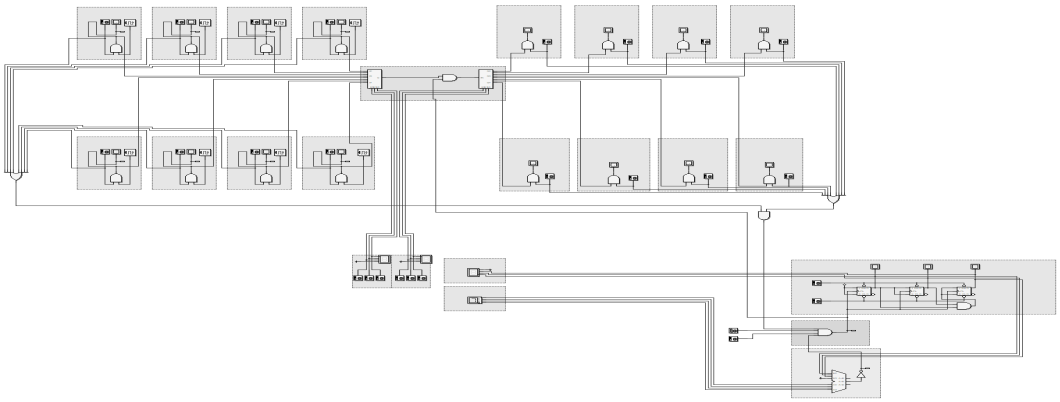


Figure 3.1: Complete Circuit (Basic Functions)

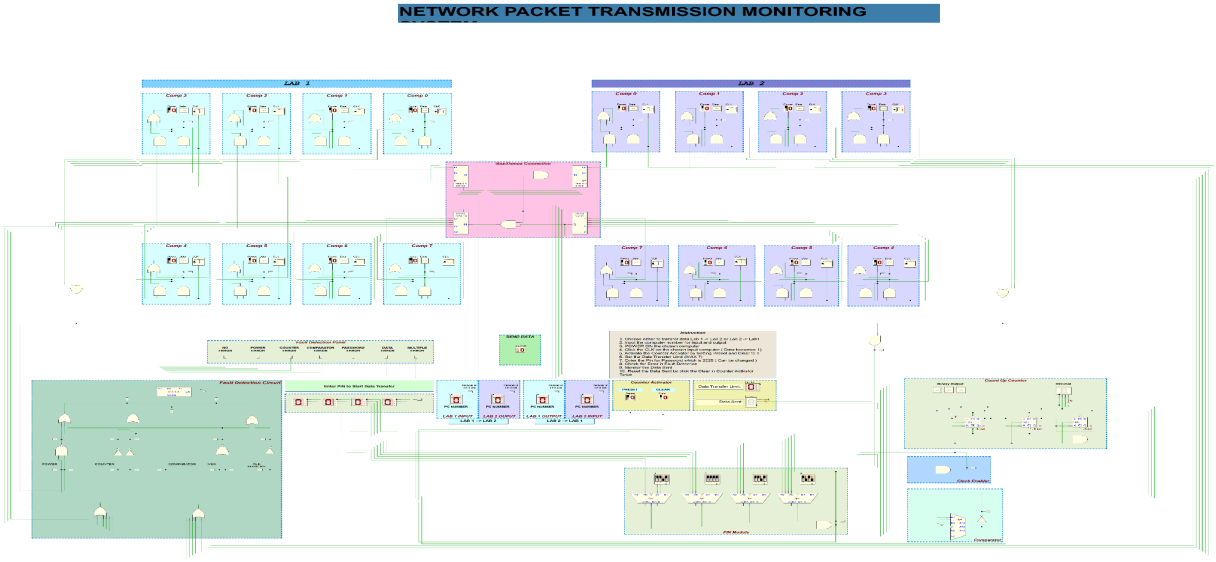


Figure 3.1: Complete Circuit (Advanced)

Additional References

Online Resources:

GeeksforGeeks. (n.d.). Introduction to Multiplexers and Demultiplexers. Retrieved from GeeksforGeeks

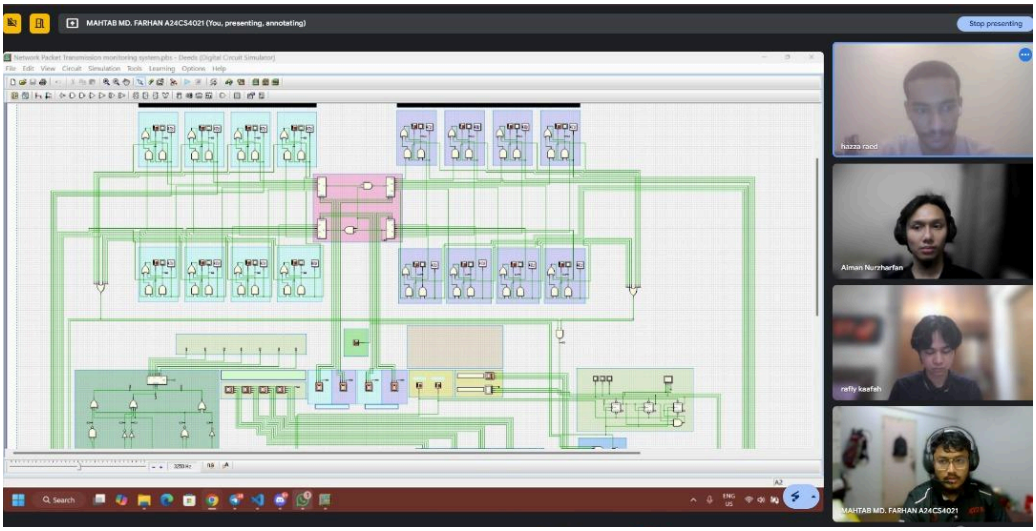
This resource helped in understanding the working of MUX and DEMUX.

Tutorials and Guides:

TutorialsPoint. (n.d.). Digital Electronics Tutorial. Retrieved from TutorialsPoint

This online tutorial helped clarify concepts related to counters, comparators, and fault detection.

Pictures of Our Project Meetings:



Click the link to see all files: *https://shorturl.at/VTbIF*