ECE412 Assignment 5

Han Yu

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I. 6-bit binary-weighted current-mode DAC

a) Fig.1 is the testbench for the 6-bit binary-weighted current-mode DAC. Since it is a 6-bit DAC and the reference voltage is just the full scale value of V_{out}, which is 256mV, $V_{LSB} = \frac{V_{ref}}{2^6} = \frac{256mV}{64} = 4mV$. The replica current source, which equals to the LSB current tail, is $I = \frac{V_{LSB}}{R_{ref}} = \frac{4mV}{50\Omega} = 80\mu A$. DC current is $I_{DC} = (2^N - 1)I = (2^6 - 1)I = 63I = 5.04mA$. Total power consumption is calculated as $P_{DC} = I_{DC} \cdot V_{DD} = (5.04mA)(1.8V) = 9.072mW$. Table.1 summarizes the dimensions and number of gate fingers for the current source MOSFETs and Table.2 summarizes the dimensions and number of gate fingers for the switch MOSFETs. Note that the replica current source follows the same transistor sizing as the LSB current source. From Fig.2 we can see that when all 6 bits are set to 1, the output goes to a maximum value of 252mV, which is the full-scale swing minus 1LSB (i.e. $256\text{mV} - 4\text{mV} = 252\text{mV}$).

Table.1 N_f, L, W_f for the current sources (eglvtpfet MOSFETs)

	d6 (LSB)	d5	d4	d3	d2	d1 (MSB)
N_f	2	4	8	16	32	64
$L(\mu m)$	0.15	0.15	0.15	0.15	0.15	0.15
$W_f(\mu m)$	2	2	2	2	2	2
W(μm)	4	8	16	32	64	128

Table.2 N_f, L, W_f for the switches (slvtpfet_mmw_6t MOSFETs)

	d6 (LSB)	d5	d4	d3	d2	d1 (MSB)
N_f	2	4	8	16	32	64
$L(nm)$	18	18	18	18	18	18
$W_f(\mu m)$	0.5	0.5	0.5	0.5	0.5	0.5
W(μm)	1	2	4	8	16	32

b) Using the input digital signals shown in Fig.2, where we set the LSB bit frequency to the highest (i.e. 1GHz) and lower frequencies for higher bits, we get the DAC transfer function as a staircase response at 65℃, as shown in Fig.3. There are 64 steps (i.e. 2^6) in total, each has a 1LSB (i.e. 4mV) contribution to the output voltage. The offset error for this DAC is $E_{off(D/A)} = \frac{V_{out}}{V_{LSB}}\Big|_{0\ldots0} = \frac{0.135mV}{4mV} = 0.034\ LSB$. The gain error is $E_{gain(D/A)} = \frac{252.078mV - 0.135mV}{4mV} - (2^6 - 1) = -0.01425\ LSB$. The INL and DNL are plotted as a function of the digital input word, as shown in Fig.4. Glitches with different magnitudes are seen when digital input code changes from 0 to 1 or from 1 to 0. For example, when the digital input code changes from 011111 to 100000, the largest glitch occurs since at this point all the 5 LSBs turn off and the MSB turn on. This potentially lets the current due to the LSB switches turn off slightly before the MSB current, causing the current to temporarily fall to a small value. Smaller glitches occur at times when smaller amounts of LSB switches are turned off. This is why glitches are not equal in magnitude. Based on the measurement, the largest glitch which occurs at code 32 is around 118mV.

c) The settling time of the DAC is the time it takes for the converter to settle within 0.5 LSB, which is 2mV in our case. Fig. 5 shows the staircase transfer function of the 6-bit DAC at 65℃ with a 5GHz clock. Fig.6 shows the worst-case settling time to be around 0.0388ns, which happens when the input digital word changes from 011111 to 100000. In this case, the largest glitch is around 119.34mV as shown in Fig.7, which is almost the same as in the previous case. Thus, we can say that the magnitude of the glitches barely changes with the sampling clock frequency.

d) The schematic that includes the 8-bit ideal ADC is shown in Fig.8. Only 6 bits of the 8-bit ADC output are fed into our 6-bit DAC. Fig.9 shows an output response with a 6 GS/s sampling rate and a 100MHz input sinusoid. SDR and ENOB are plotted as a function of frequency (i.e. 100MHz, 1.1GHz, and 2.1GHz) at sampling rates of 6 GS/s (in blue) and 7 GS/s (in orange), respectively, as shown in Fig.10 and Fig.11. The SDR and ENOB data was collected from the DFT spectrum each time (as shown in Fig.12) and been post processed by MATLB. We can tell from these two plots that as the sampling rate of the ideal ADC increases, better SDR and ENOB could be achieved. This is true because a higher frequency sampling clock typically has lower jitter, which improves SDR and therefore ENOB. The effective resolution bandwidth (ERBW) is the bandwidth over which SNDR is within 3-dB of its peak value. From Fig.13, we can see that the ERBW at a sampling frequency of 6 GS/s is around 350MHz and that at a sampling frequency of 7 GS/s is around 380MHz. Looking at the Fig.11, similar conclusion can be made because ERBW can also be found at the bandwidth over which ENOB is within 0.5 bits of its peak value.

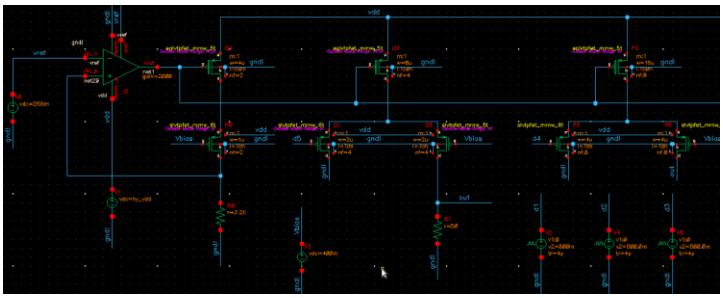


Fig.1 6-bit DAC implementation (only 2 bits are included in the screenshot)

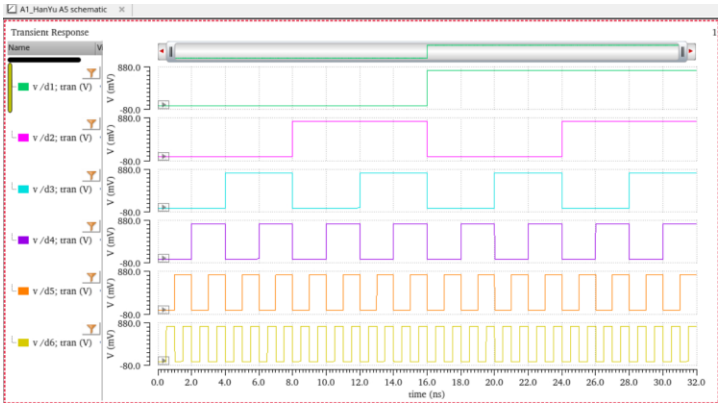


Fig.2 Input voltages (d1 to d6, where d1 is the MSB and d6 is the LSB) to sweep input digital signals from 000000 to 111111

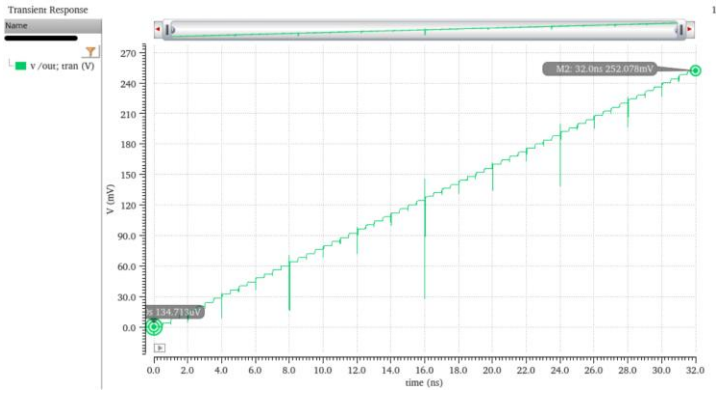


Fig.3 Staircase DAC transfer function with 1GHz clock frequency.

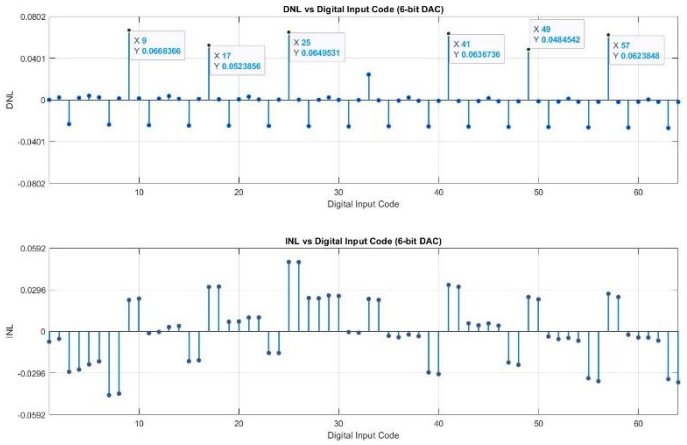


Fig.4 INL and DNL measurement as a function of the digital input word

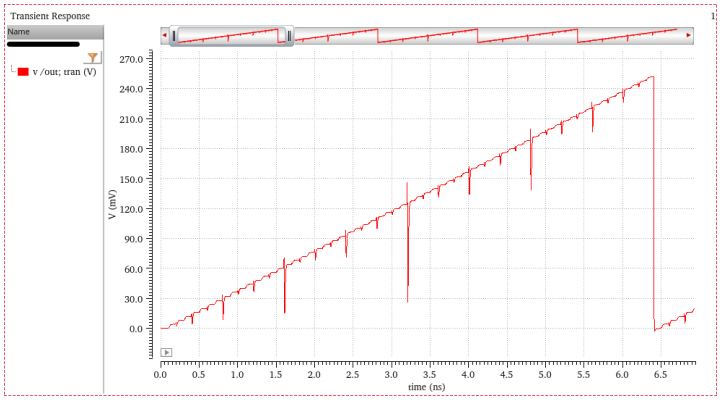


Fig.5 Staircase DAC transfer function with 5GHz clock frequency

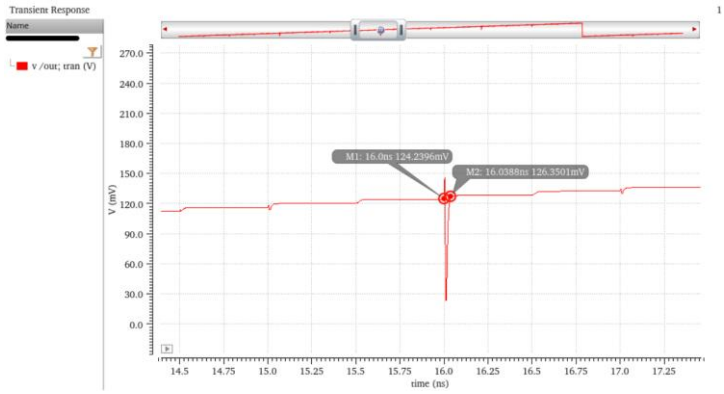


Fig.6 Settling time for the DAC output to settle within 0.5 LSB (worst-case scenario)

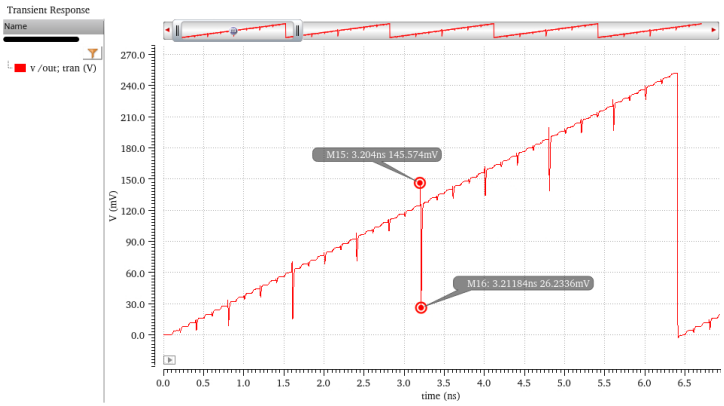


Fig. 7 Worst-case glitch measurement at code 32 with 5GHz clock frequency

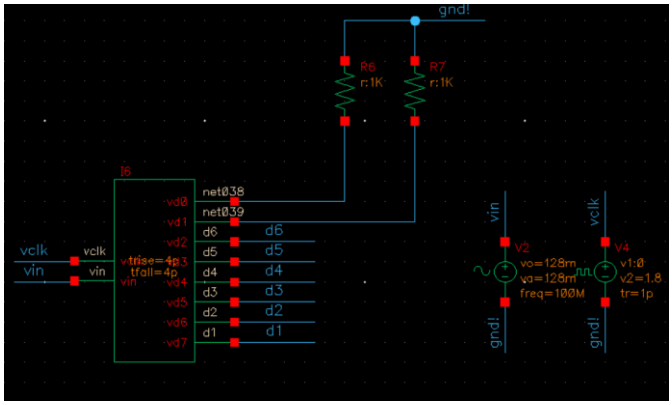


Fig.8 Schematic for setting up the ideal 8-bit ADC which feeds its output 6 bits into the designed 6-bit DAC

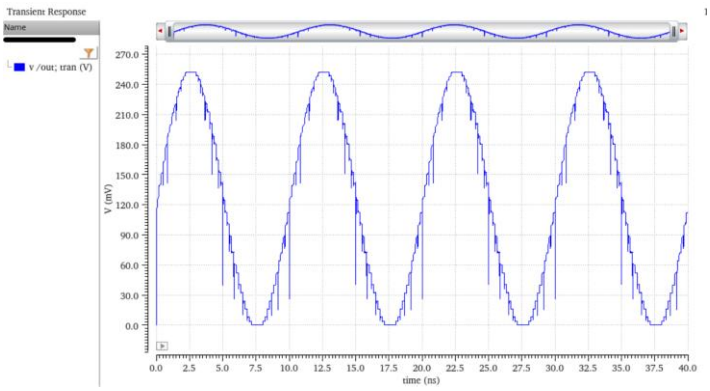


Fig.9 A full scale output sinusoid generated at 100MHz at a sampling rate of 6GS/s

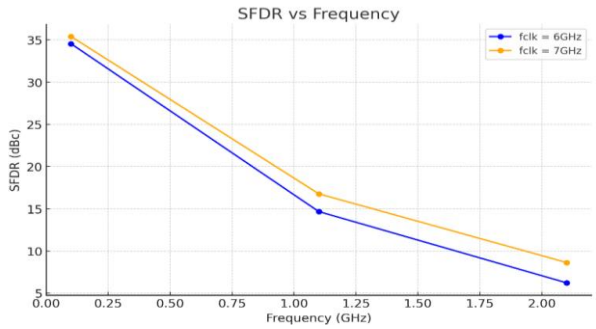


Fig.10 SDR as a function of frequency at sampling rates of 6GS/s (blue) and 7GS/s (orange)

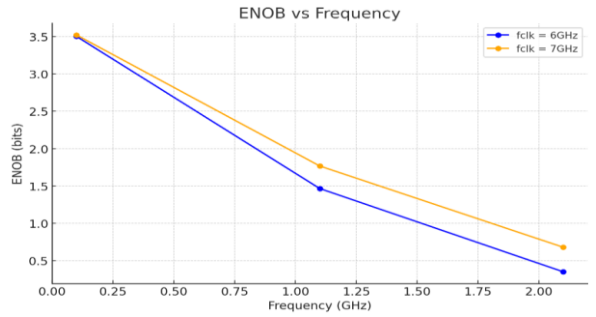
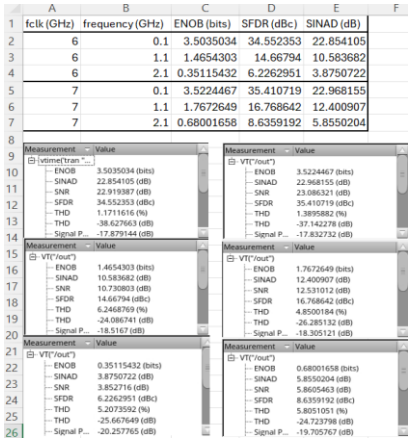


Fig.11 ENOB as a function of frequency at sampling rates of 6GS/s (blue) and 7GS/s (orange)



fclk (GHz)	frequency (GHz)	ENOB (bits)	SFDR (dBc)	SINAD (dB)
6	0.1	3.5035034	34.552353	22.854105
6	1.1	1.4654303	14.66794	10.583682
6	2.1	0.35115432	6.2262951	3.8750722
7	0.1	3.5224467	35.410719	22.968155
7	1.1	1.7672649	16.768642	12.400907
7	2.1	0.68001658	8.6359192	5.8550204

Fig.12 SDR and ENOB data from total 6 cases

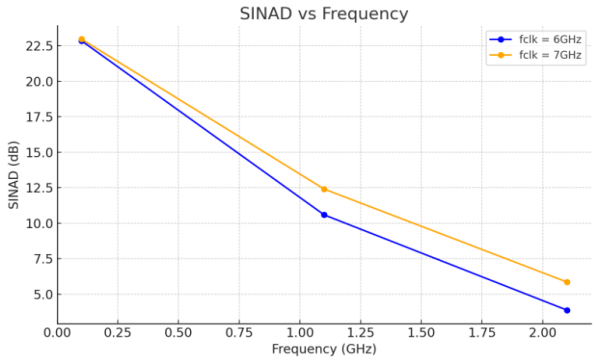


Fig.13 SNDR (SINAD in Cadence) over input frequency. ERBW is found at the frequency where SNDR is within 3-dB of the peak value.