ECE412 Assignment 3

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I. MOSFET switch simulation and modelling

(a) A MOSFET switch is simulated as shown in Fig.1. We can extract $C_{gs}+C_{sb}$ from $imag(Y_{11}+Y_{12})/2\pi f$, C_{ds} from $-\text{imag}(Y_{12})/2\pi f$, and $C_{gd}+C_{db}$ from $imag(Y_{22}+Y_{12})/2\pi f$. Given the MOSFET we use is for mm Wave applications, we choose a reasonable operating frequency at 5GHz to extract the capacitance and resistance per unit gate width. As shown in Fig.2, $C_{gs}+C_{sb}=3.2fF$, $C_{ds}=3.67fF$, $C_{gd}+C_{db}=3.49fF$, $C_{OFF}=6.7fF$. Divide these values by the total gate width and we get the parasitic capacitances per unit gate width: $C'_{gs}+C'_{sb}=3.2fF/8.6\mu m=0.372fF/\mu m$, $C'_{ds}=3.67fF/8.6\mu m=0.427fF/\mu m$, $C'_{gd}+C'_{db}=3.49fF/8.6\mu m=0.406fF/\mu m$, , $C'_{OFF}=0.778fF/\mu m$. $R_{ON}=40.697\Omega$ is obtained from $1/real(-Y_{12})$ when V_c is set to 0.2V, as shown in Fig.3. R_{ON} per unit gate width is then $R'_{ON}=40.697\Omega*8.6\mu m=350\Omega*\mu m$. The figure of merit $FoM=R_{ON}C_{OFF}=40.697\Omega*6.7fF=0.273ps$, which is quite small in our case.

(b) As shown in Fig.4, increasing the DC voltages of the two psin sources from 0V to 0.2V drops C_{OFF} from 6.7fF to 6.111fF. This is because as the applied voltage increases, the depletion region becomes wider. Since the junction capacitance $C_{junction}\propto\frac{1}{W_{depletion}}$, the capacitances will decrease. Fig.5 plots the new R_{ON}, where we can see R_{ON} increases from 40.697Ω to 140.7 Ω due to the decrease of V_{gs}. The new FoM is calculated as: $FoM=R_{ON}C_{OFF}=140.7\Omega*6.111fF=0.86ps$. The overall FoM increases as the increase in R_{ON} dominates.

II. Switched capacitor simulation and charge injection

(a) Fig.6 shows the testbench for the CMOS switched capacitor. Non-overlapping sampling clock signals are generated with a 25% duty cycle and 2GHz frequency, as shown in Fig.7. These non-overlapping clocks ensure that when the first TG is ON, the second TG is OFF, and vice versa. Signal waveforms at input, output, and *store* nodes are simulated as Fig.8 shows, with a 100mV amplitude, 400mV DC biased input sinusoidal source. We can clearly see that the output signal is smoother and has smaller glitches than that at the *store* node because charge injection transients are reduced by the RC filter (LPF).

(b) The equivalent resistance of the switched capacitor is calculated as $R_{eq}=\frac{T}{C}=\frac{1}{Cf_s}=\frac{1}{200fF*2GHz}=2.5k\Omega$. The 3dB bandwidth of the LPF formed with the load capacitance of 200fF is $f_{3dB}=\frac{1}{2\pi R_{eq}C_{load}}=\frac{1}{2\pi*2.5k\Omega*200fF}=318.31MHz$.

(c) Charge injection errors happen when the switches are turned OFF, and the charge stored in the channel of the MOSFETs is injected into the *store* node, causing a voltage error. Fig.9 shows the maximum error due to charge injection on the held output signal at the *store* node, which is around 0.041mV. The charge difference is: $\Delta Q=C\Delta V_{max}=200fF*(0.041mV)=8.2*10^{-18}C$.

(d) The SDR (SFDR in Cadence) at the output of the circuit is about 26.96dBc, as depicted in the DFT spectrum result in Fig.10. It is calculated as $SDR=\frac{output\ fundamental\ power}{dominant\ distortion\ tone}=-20.921dB-(-47.8816dB)=26.96dB$.

(e) The channel charge (of a NMOS) can be expressed as $Q=-WLC_{ox}V_{eff}=-WLC_{ox}(V_{GS}-V_t)$. Also, since $\Delta V_{max}=\frac{Q}{C}$, the max error due to charge injection change will be approximately multiplied by 10 when the transistor size is increased by a factor of 10.

(f) If we replace the two CMOS transmission gates by four NMOS, the maximum error due to charge injection will increase. This is because in a CMOS transmission gate, NMOS and PMOS inject opposite charge components, partially canceling each other out. With only NMOS, however, there is no PMOS to compensate, so more charge will be injected when the switch turns OFF. As a result, larger glitches will appear at the *store* node. The SDR will be reduced, since more glitches introduced by the NMOS-only switches means more signal distortion at the output.

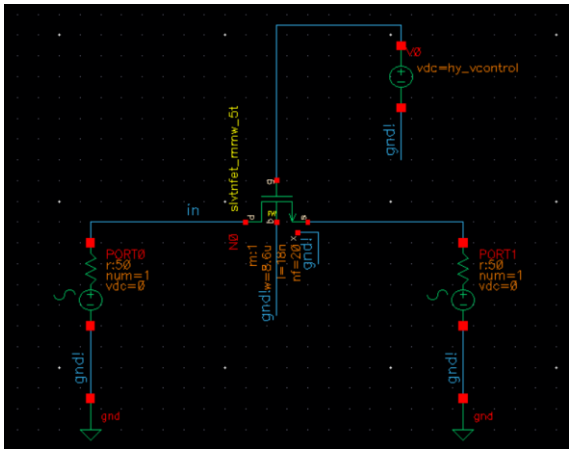

Fig.1 MOSFET switch testbench

Fig.2 $C_{gs}+C_{sb}$, C_{ds}, $C_{gd}+C_{db}$ and C_{OFF} when DC voltage of the two psin sources is 0V

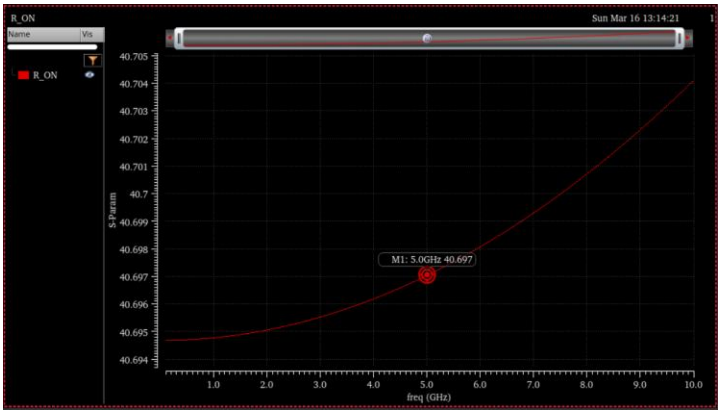

Fig.3 R_{ON} when $V_c = 0.8V$ and DC voltage of the two psin sources is 0V

Fig.4 $C_{gs}+C_{sb}$, C_{ds}, $C_{gd}+C_{db}$ and C_{OFF} when DC voltage of the two psin sources is 0.2V

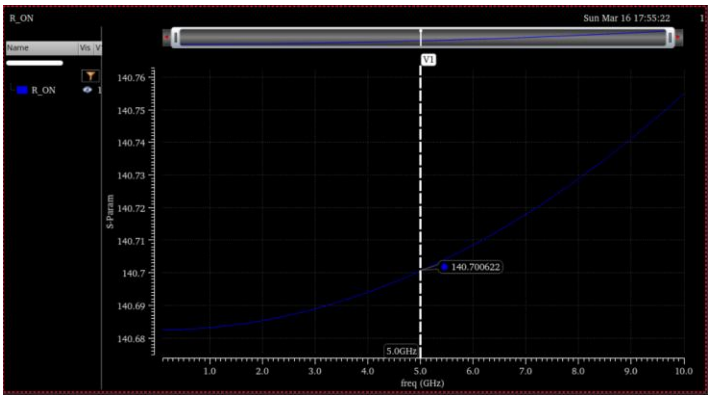

Fig.5 R_{ON} per unit gate width when $V_c = 0.8V$ and DC voltage of the psins is 0V

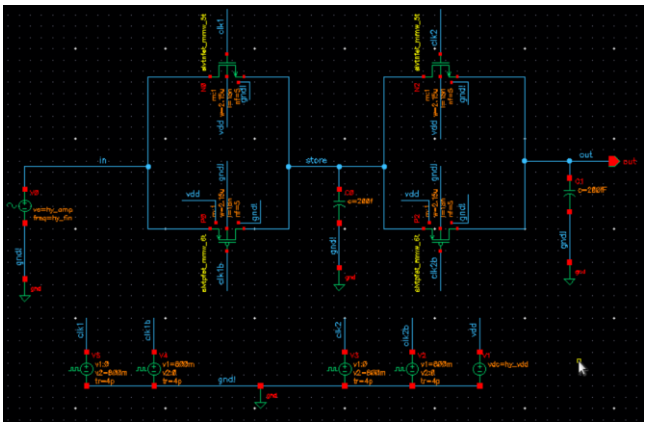

Fig.6 CMOS switched capacitor testbench

Fig.7 non-overlapping 2GHz sampling clock signals

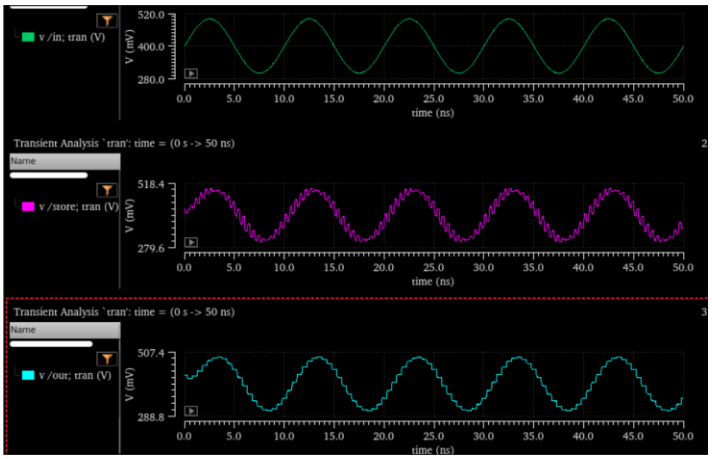

Fig.8 Signal waveforms at the input(top), output(bottom) and *store*(middle) nodes

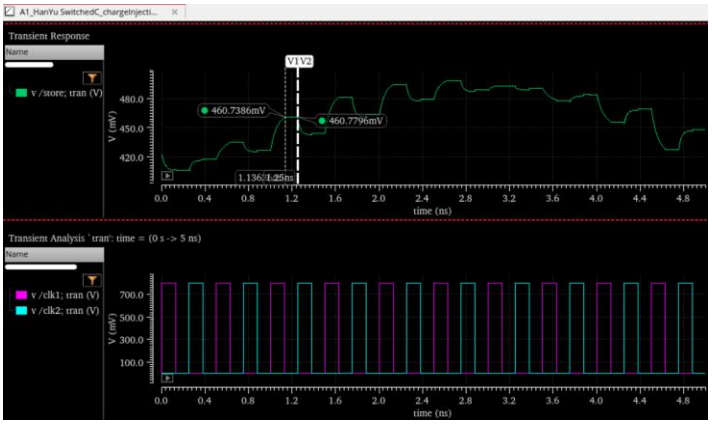

Fig.9 Maximum error due to charge injection on the held output signal at the *store* node

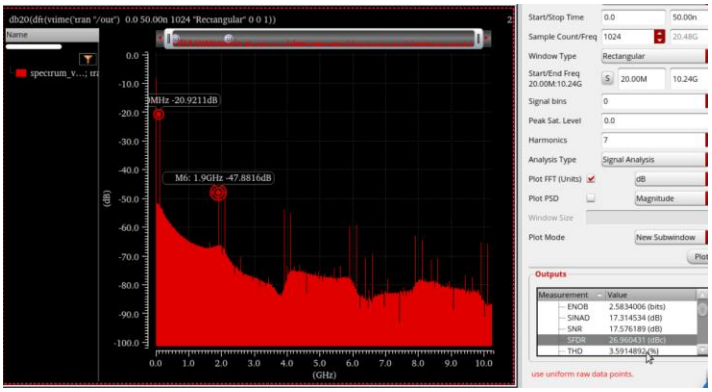

Fig.10 DFT spectrum at output node of the CMOS SC circuit