ECE412 Assignment 1

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I. Op-amp integrator simulation

a) An ac simulation for the testbench shown in Fig.1 outputs the transfer function shown in Fig.2. From the diagram, we can see the small signal response of the integrator from 1kHz to 20GHz. Theoretically, the general form of a first-order filter is $H(s) = \frac{k_1 s + k_0}{s + \omega_0}$. For such an op-amp integrator low-pass filter, k_1 is 0, making the transfer function becomes $H(s) = \frac{k_0}{s + \omega_0}$. ω_0 is calculated using the equation $\omega_0 = 1/A_0 RC = 10^8\ rad/s$. At very low frequencies, $H(s) = \frac{k_0}{\omega_0} = A_0 = 100$, where A_0 is the gain of the op-amp, which gives $k_0 = 100, \omega_0 = 10^{10}\ rad/s$. From Fig.2, the cut-off frequency is at 13.367MHz, so $\omega_0 = 2\pi * 13.367MHz = 0.84 * 10^8\ rad/s$. Then, $k_0 = 100\omega_0 = 0.84 * 10^{10}\ rad/s$. $k_1 = 0$. The actual values are very close to the theoretical ones.

b) Fig.3 shows the 1MHz input sinusoidal signal with 1mV amplitude and the corresponding output signal with noise. From the transient noise simulation result, we can see small distortions present in the output signal due to the flicker and thermal noise contribution from the resistor and the op-amp. Next, using the Cadence Measurement calculator, DFT spectrum is plotted for the output signal, as shown in Fig.4. A DC component of around -8dB is found at 0MHz, which matches the expected value calculated by $20\log_{10} 0.4 = -7.95dB$. A -20.35dB is found at the fundamental harmonic, and a -82.97dB and a -86.86dB are found at the 3rd and 5th harmonics, respectively. SFDR is found to be 45.19dBc. THD is found to be 0.09%.

c) Now, if we increase the input amplitude from 1mV to 5mV and repeat (b), we get the input and output signals (with noise) transient result shown in Fig.5 and the DFT spectrum shown in Fig.6. We can observe a higher distortion directly from the output as it's almost like a square wave. From the DFT measurements, SFDR decreases to 15.24dBc, which means linearity is worsen in this case; and THD increases to 17.5%, which implies a higher distortion in higher order harmonics compared to the fundamental component. This is because THD typically increases with the input signal amplitude. As the input signal amplitude increases, the odd-order harmonics become more dominant and grow in power, which reduces the SFDR.

d) Replacing R_1 with an NMOS as shown in Fig.7, we can get a MOSFET-C Opamp integrator. The NMOS is operated in triode region as $V_{gs} > V_{tn}, V_{ds} < V_{eff}$, and its drain current follows $I_d = \mu_n C_{ox} \frac{W}{L}\left(\left(V_{gs} - V_{th}\right)V_{ds} - \frac{V_{ds}^2}{2}\right)$. This can be checked by running a DC response of I_d when sweeping V_{ds} from 0V to 0.8V, as shown in Fig.8. The near-linear relationship between I_d and V_{ds} makes the NMOS mimicking the behavior of a resistor. Thus, by adjusting V_{ds}, the effective resistance of the MOSFET can be controlled, making it possible for us to fine tune the overall resistance within the integrator circuit. We can plot the 3dB bandwidth of the integrator as a function of the control voltage on the gate of the MOSFET when control voltage changes from 0 to 0.8V with a linear step size of 100mV. Fig.9 shows the frequency response under control voltage changes from 0 to 0.8V. Fig.10 plots the 3dB bandwidth at different control voltage at the gate of NMOS. We can observe that the 3dB bandwidth has experienced a significant boost as control voltage increases. This trend with the theoretical analysis: given that at triode region, $r_{ds} = \frac{1}{\mu_n C_{ox}(\frac{W}{L})(V_{gs} - V_{tn})}$, as we increase the control voltage, r_{ds} decreases, which increases the cutoff frequency (bandwidth) since $f_c = \frac{1}{2\pi r_{ds} C}$. Now, with the new integrator we just created, set the control voltage to 0.6V and input amplitude to 5mV. We plot the DFT spectrum of the output again, with the results shown in Fig.11. In this case, SFDR is 15.17dBc, and THD is 17.64%, which are very close to the results from an op-amp-RC integrator we simulated before. This is because the replacement of the NMOS acts as a tunable resistor which mimics the behavior of the resistor in the Opamp-RC integrator. In conclusion, the advantage of using a MOSFET-C Op-amp integrator is that it allows for dynamic control of the integration time constant, which in turn, allows for control of output bandwidth by simply adjusting the gate voltage of the MOSFET. Note that this only applies when the MOSFET is in its triode region.

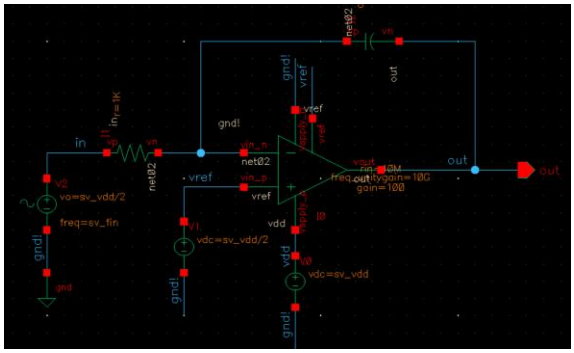

Fig.1: Opamp-RC integrator testbench

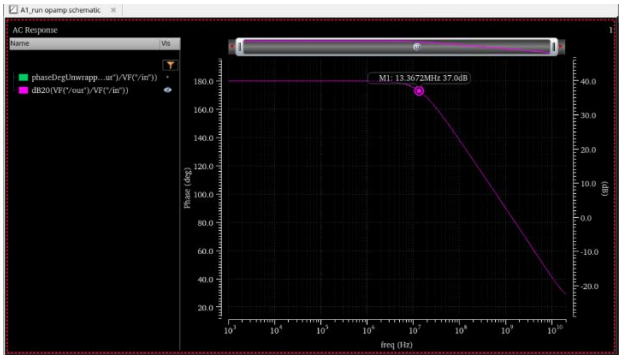

Fig.2: Transfer function of the Opamp-RC integrator with frequency swept from 1kHz to 20GHz

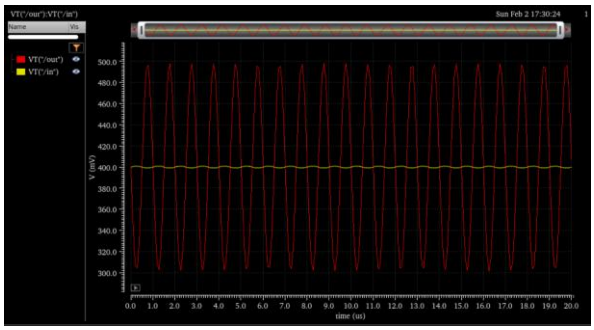

Fig.3: transient noise simulation of a 1mV, 1MHz input sinusoidal signal (yellow) and the output (red)

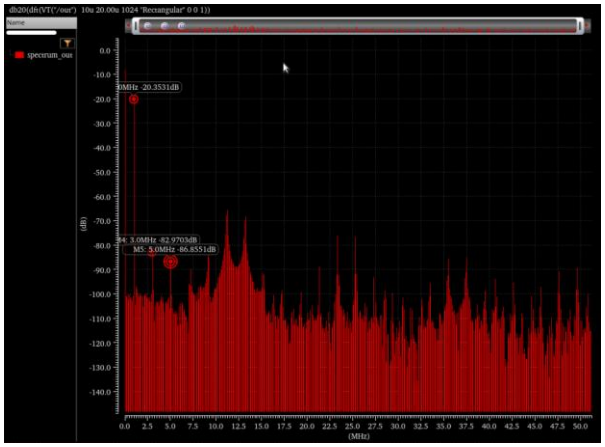

Fig.4: DFT spectrum of the output signal from Fig.3

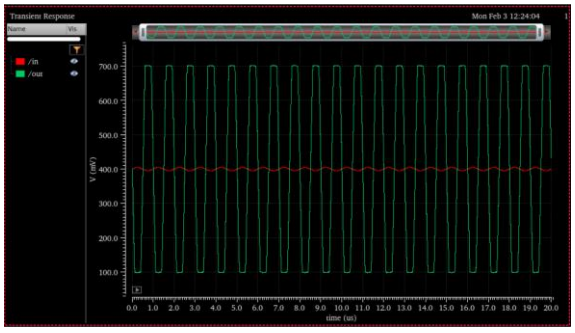

Fig.5: transient noise simulation of a 5mV, 1MHz input sinusoidal signal (red) and the output (green)

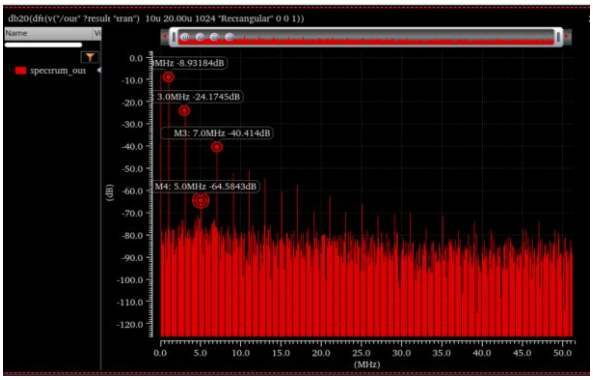

Fig.6: DFT spectrum of the output from Fig.5

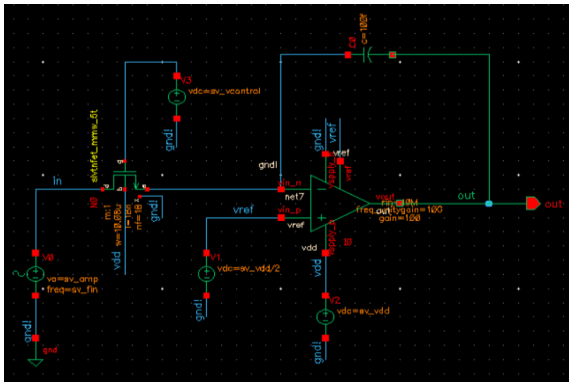

Fig.7: MOSFET-C Op-amp integrator testbench

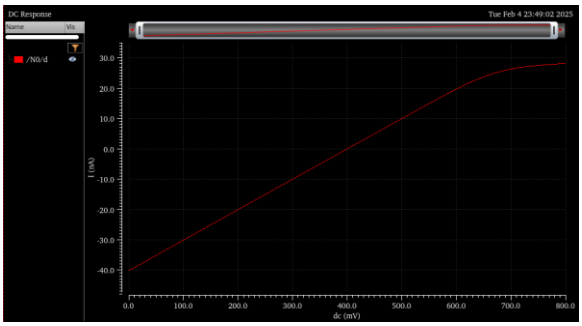

Fig.8: DC response of NMOS drain current vs. V_{ds} (triode region)

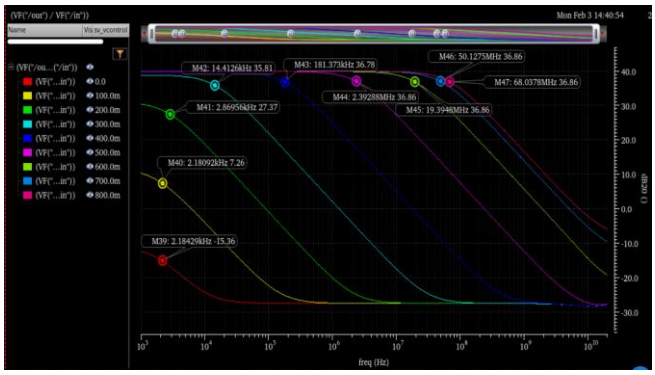

Fig.9: AC sweep of the integrator across V_{gs}

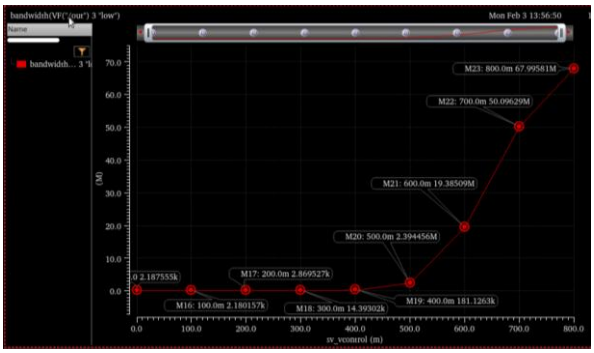

Fig.10: 3dB bandwidth as a function of control voltage V_{gs}

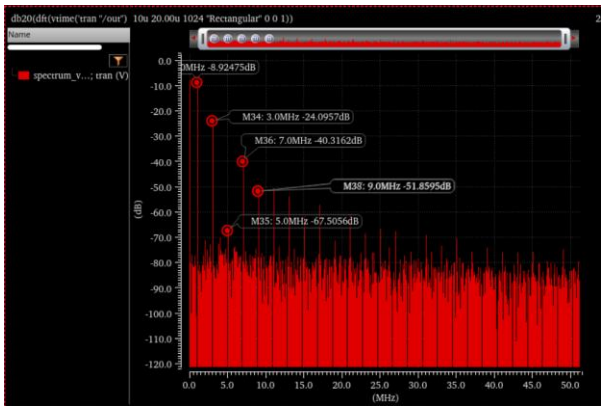

Fig.11: DFT spectrum of the output with 5mV, 1MHz input for the MOSFET-C Op-amp integrator