ECE412 Assignment 2

Han Yu

Feb 26, 2025

I. Reference Oscillator Phase Noice Model

The general phase noise equation is given by:

$$L(f) = \frac{h_3}{f^3} + \frac{h_2}{f^2} + \frac{h_1}{f} + h_0 \quad (1)$$

For the reference oscillator, since there is only $\frac{1}{f^2}$ dependence at low and middle frequency offsets, $h_3 = h_1 = 0$. Given that its phase noise has a noise floor of -160 dBc/Hz at large frequency offset, we get the relationship from (1): $L_{ref}(f) = -160 = 10log_{10}(h_0)$, where we get $h_0 = 10^{-16}\frac{rad^2}{Hz}$. We are also told that at 10 kHz frequency offset the phase noise is -140 dBc/Hz, so we get $10^{-14} = \frac{h_2}{(10\ kHz)^2} + 10^{-16} \approx \frac{h_2}{(10\ kHz)^2}$, and $h_2 = 10^{-6}\frac{rad^2}{Hz}$. Overall, the phase noise equation is

$$L_{ref}(f) = \frac{10^{-6}}{f^2} + 10^{-16}\frac{rad^2}{Hz} \quad (2)$$

Fig.1 shows $L_{ref}(f)$ characteristics (in red) in dBc/Hz vs. frequency using a logarithmic frequency axis.

II. Voltage-Controlled Oscillator Phase Noise Model

The phase noise of the VCO can also be described by (1). Given that there's no $\frac{1}{f^1}$ or $\frac{1}{f^2}$ dependence, we know that $h_1 = h_2 = 0$. Since a noise floor of -140 dBc/Hz appears at large f_m, we get the expression $L_{vco}(f) = -140 = 10log_{10}(h_0)$, from which we then get $h_0 = 10^{-14}rad^2/Hz$. According to *Table* 1 in the assignment handout, at 1MHz offset frequency, the phase noise is -96 dBc/Hz, so $10^{-9.6} = \frac{h_3}{(1\ MHz)^3} + 10^{-14} \approx \frac{h_3}{(1\ MHz)^3}$, and we get $h_3 = 2.51 \times 10^8 rad^2/Hz$. Overall, the phase noise equation for this VCO is

$$L_{vco}(f) = \frac{10^{-2.51\times10^8}}{f^3} + \frac{10^{-14}rad^2}{Hz} \quad (3)$$

Fig.1 shows $L_{vco}(f)$ characteristics (in blue) in dBc/Hz vs. frequency using a logarithmic frequency axis.

III. Third-order PLL Design

Below are steps to design a third-order PLL. Design specifications are taken from the assignment handout and are summarized in Table 1.

Table 1. Third Order PLL Design Specifications

Surname start with	$f_{osc}(GHz)$	$K_{vco}(MHz/V)$	$L_{vco}@1MHz$	$f_{ref}(MHz)$
Y	62-65	2200	-96 dBc/Hz	33.75

a) We choose a single VCO frequency at 64.8 GHz within the given range, from which we can calculate $N = \frac{f_{osc}}{f_{ref}} = \frac{64.8\ GHz}{33.75\ MHz} = 1920$.

b) VCO gain constant K_{osc} is 2200 MHz/V.

c) Use Q=0.5 to achieve a relatively minimal peaking or fast settling of the loop.

d) According to the *pll_bandwidth_choice_and_jitter.pdf*, a good choice for f_{3dB} is at the intersection point of $L_{vco}(f)$ and $L_{ref}(f) + 20log_{10}(N)$. The $L_{ref}(f) + 20log_{10}(N)$ characteristics can be found in Fig.1 (in green). This f_{3dB} point is selected specifically as it represents the frequency at which the contributions from the multiplied reference noise and the VCO noise are roughly equal. The intersection is roughly at 8.77× 10^5 Hz as shown in Fig.1. Therefore, the loop bandwidth $\omega_{3dB}\ is\ 2\pi \times 8.77 \times 10^5\ rad/s$.

e) For Q=0.5, $\omega_{pll} = 0.4\omega_{3dB} = 0.8\pi \times 8.77 \times 10^5 rad/s$.

f) For a charge-pump integer-N PLL, the following formula applies:

$$\frac{I_{ch}}{C_1} = \omega_{pll}^2 \frac{2\pi N}{K_{osc}} \quad (4)$$

We already know the values of ω_{pll}, N, and K_{osc}, (4) gives $\frac{I_{ch}}{C_1} = (0.8\pi \times 8.77 \times 10^5)^2 \times \frac{2\pi\times1920}{2\pi\times2200\times10^6} = 4.24 \times 10^6 V/s$. Take $C_1 = 10pF$, then $I_{ch} = 42.5\mu A$.

g) Resistor R is chosen so that $\omega_z = Q\omega_{pll} = 0.5 \times 0.8\pi \times 8.77 \times 10^5 = 0.4\pi \times 8.77 \times 10^5\ rad/s$. Then, $R = \frac{1}{\omega_z C_1} = 226.8\ k\Omega$.

h) Finally, the de-glitching capacitor $C_2 = \frac{C_1}{10} = 1pF$.

Table 2. below summarizes the design parameters of the 3rd order PLL.

Table 2. Summary of the Third Order PLL Design Parameters

$h_{2,ref}[rad^2/Hz]$	$h_{0,ref}[rad^2/Hz]$	$h_{3,vco}[rad^2/Hz]$	$h_{0,vco}[rad^2/Hz]$
10^{-6}	10^{-16}	2.51×10^8	10^{-14}

N	Q	$\omega_{3dB}[rad/s]$	$\omega_{pll}[rad/s]$	$\omega_z[rad/s]$
1920	0.5	$2\pi \times 8.77 \times 10^5$	$0.8\pi \times 8.77 \times 10^5$	$0.4\pi \times 8.77 \times 10^5$

$I_{ch}[\mu A]$	$R[k\Omega]$	$C_1[pF]$	$C_2[pF]$
42.5	226.8	10	1

The open-loop response of PLL is defined as:

$$L(s) = \frac{K_{pd} K_{lp} K_{osc} H_{lp}(s)}{Ns} \quad (5)$$

For a 3rd-order (Type-II) PLL, the loop filter gain is:

$$K_{lp} H_{lp}(s) = \frac{1}{s(C_1 + C_2)} \cdot \frac{1 + sRC_1}{1 + sR\left(\frac{C_1 C_2}{C_1 + C_2}\right)} \quad (6)$$

We also know that $K_{pd} = \frac{I_{ch}}{2\pi}$. Substituting the design parameters into (5), we get:

$$L(s) = \frac{I_{ch} K_{osc}}{2\pi \cdot N} \cdot \frac{1 + sRC_1}{s^2(C_1 + C_2)\left(1 + sR\left(\frac{C_1 C_2}{C_1 + C_2}\right)\right)} \quad (7)$$

The bode plots of the PLL loop gain (i.e., $L(s)$) is shown in Fig.2. The unity gain frequency ω_t is found when the magnitude response is at 0dB, which gives roughly $\omega_t = 1.46\ MHz$. At ω_t, the phase response increases from -180° to -124°, which indicates a phase margin of 56°. Fig.3 shows the magnitude response of the jitter transfer function, where we found $\omega_{3dB} = 1.49\ MHz$. The $L_{out}(f)$ characteristics (in yellow) is plotted in Fig.1. At 1 MHz offset frequency, the main phase noise contributor is the VCO since $L_{out}(f_m = 1MHz)$ is the same as $L_{vco}(f_m = 1MHz)$.

The rms random jitter can be calculated using the formula:

$$\sigma_{jrms} = \frac{1}{2\pi f_{out}} \cdot \theta_{rms} \quad (8)$$

, where

$$\theta_{rms} = \sqrt{2\int_0^\infty L(f_m) df_m} \quad (9)$$

is the rms phase error.

To calculate the rms phase error, we need to know the contribution of noise sources. At low frequency, i.e. frequencies below $10^5\ Hz$, L_{ref} dominates, especially the term $\frac{10^{-6}}{f^2}$. Between $10^5\ Hz$ and the loop bandwidth, $8.77 \times 10^5\ Hz$, the 10^{-16} term from L_{ref} is the dominant noise source. At frequencies above the loop bandwidth, VCO becomes the main source of phase noise: Between $8.77 \times 10^5\ Hz$ and $3 \times 10^7\ Hz$, the $\frac{10^{-2.51\times 10^8}}{f^3}$ term from L_{vco} is the main noise source. Finally, between $3 \times 10^7\ Hz$ and $10^{10}\ Hz$, the 10^{-14} term from L_{vco} dominates.

Integrate all the noise contributions above and we get the rms phase error from (9):

$$\theta_{rms} = \left(2\left[\int_{10^3}^{10^5} \frac{10^{-6}}{f^2} df_m + \int_{10^5}^{8.77\times 10^5} 10^{-16} df_m + \int_{8.77\times 10^5}^{3\times 10^7} \frac{10^{-2.51\times 10^8}}{f^3} df_m + \int_{3\times 10^7}^{10^8} 10^{-14} df_m\right]\right)^{\frac{1}{2}} = 1.81 \times 10^{-2}\ rad$$

Now, substitute θ_{rms} into (8) to calculate the rms PLL jitter:

$$\sigma_{jrms} = \frac{1}{2\pi f_{out}} \cdot \theta_{rms} = \frac{1}{2\pi \times 64.8\ GHz} \cdot 1.81 \times 10^{-2} = 0.044 ps.$$

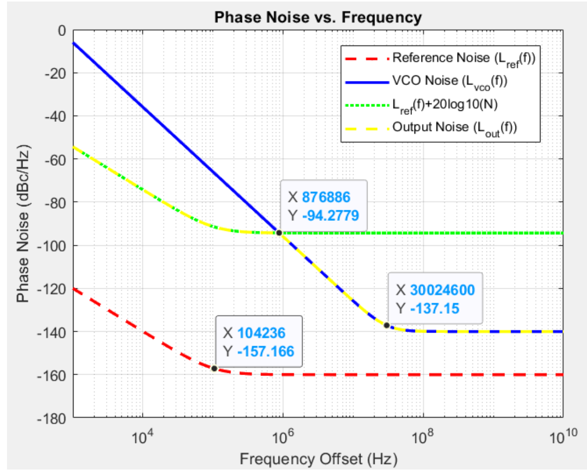

Fig.1 Phase Noise vs. Frequency for $L_{ref}(f)$, $L_{vco}(f)$, $L_{ref}(f) \times N^2$ and $L_{out}(f)$. 3dB bandwidth is at the intersection of $L_{vco}(f)$ (in blue) and $L_{ref}(f) \times N^2$(in green).

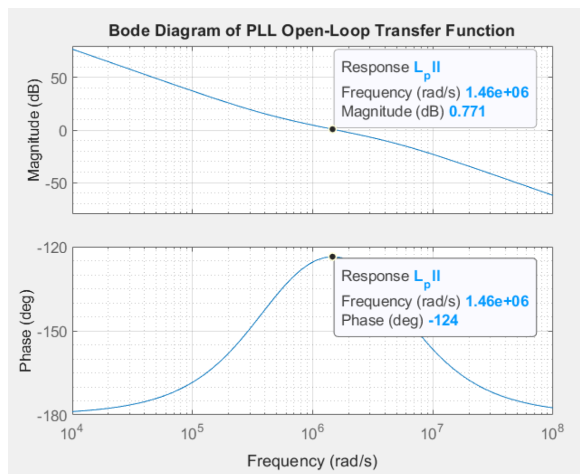

Fig.2 Magnitude (in dB) and phase response of the PLL loop gain in the phase domain. The unity gain frequency (ω_t) is marked in the plots.

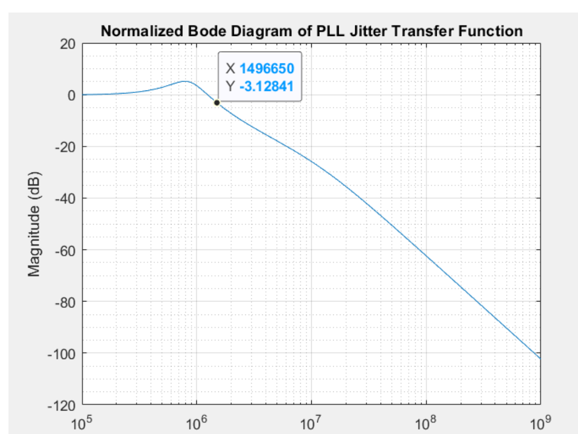

Fig.3 3dB bandwidth of the PLL jitter transfer function