ECE412 Assignment 4

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I. CMOS T/H and S/H simulation

a) The 3-dB bandwidth in tracking mode from the input to the first hold capacitor and to the second hold capacitor is given in Fig.1, 4.5GHz and 2.9GHz for input to tha and input to output, respectively. From hand analysis, the 3dB bandwidth at S/H node is calculated as: $f_{3dB} = \frac{1}{2\pi R_{eq} C_{load}} = \frac{1}{2\pi \times \frac{1}{Cf_s} \times C_{load}} = \frac{1}{2\pi \times \frac{1}{200fF \times 10GHz} \times 200fF} = 1.6GHz.$

b) Isolation is how effectively the input signal is blocked from reaching the output when the circuit is in hold mode (all switches are turned off). It is illustrated in Fig.2. The isolation is not infinite in this case due to charge injection and clock feedthrough. At higher frequency the isolation gets worse because the impedance of parasitic capacitors is inversely proportional to the frequency.

c) Waveforms at the input, T/H, and S/H nodes are shown in Fig.3. Fig.4 shows the pedestal step at the T/H node, with a 1GHz sinusoidal input signal with 300mV amplitude, which is around 0.62mV. The pedestal at the T/H node is indeed signal-dependent. Specifically, while the clock feedthrough is a signal-independent offset and is usually less important, the charge injection error in the total pedestal error is signal-dependent. Given its formula is $\Delta V' = -\frac{C_{ox} WL (V_{DD} - V_{tn} - V_{in})}{2C_{hld}}$, we can see the charge injection error, therefore the pedestal step, is dependent on the input signal. The spectrum at the input node and at the output node are shown in Fig.5 and 6, respectively. As we can see, there is a huge degradation in terms of SDR (SFDR) at the output compared to the input. This is mainly due to: clock feedthrough (This is why we observe peaks around 10GHz, 20GHz, 30GHz, etc.) and charge injection.

d) Waveforms at the input, T/H, and S/H nodes are shown in Fig.7. Fig.8 shows the pedestal step at the T/H node, with a 1GHz sinusoidal input signal with 5mV amplitude, which is around 0.085mV. The pedestal at the T/H node is signal-dependent. This proves our previous claim that the pedestal at the T/H node is signal-dependent. The spectrum at the input node and at the output node are shown in Fig.9 and 10, respectively. SFDR is around 6.77dBc at the output.

e) IIP3 is calculated by the equation: $IIP_3 = \frac{\Delta P|_{dB}}{2} + P_{in|_{dBm}}$. As shown in Fig.11, the spectrum at the output node shows that the power density at 200MHz and 250MHz are -10.41dB and -10.45dB, respectively, and that at 150MHz and 300MHz are -50.52dB and -46.42dB, respectively. Therefore, $P_{in|_{dBm}} = \frac{-10.41dB + (-10.45dB)}{2} = -10.43dB$. $\frac{\Delta P|_{dB}}{2} = \frac{-10.43dB - (-50.52 - 46.42/2)}{2} = 19.02dB$. $IIP3 = 19.02dB - 10.43dB = 8.59dB$.

f) Fig.12 shows the SDR for input frequencies ranging from 100MHz to 900MHz, with a step size of 200MHz and amplitude of 300mV. Since the step size is a little bit large, we approximate the large signal bandwidth of the SHA to be at 168.7MHz.

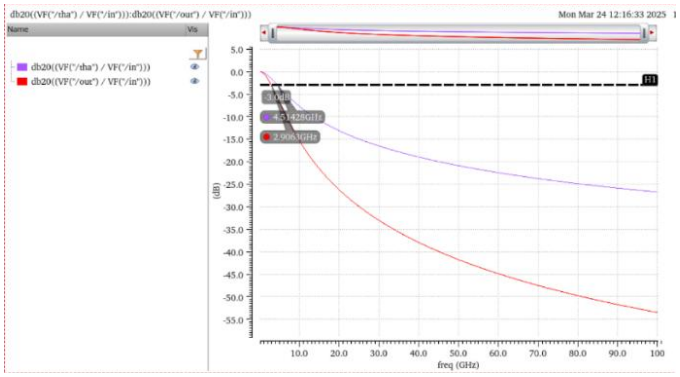

Fig.1 Transfer function in dB from input to the T/H (in purple) and S/H nodes (in red)

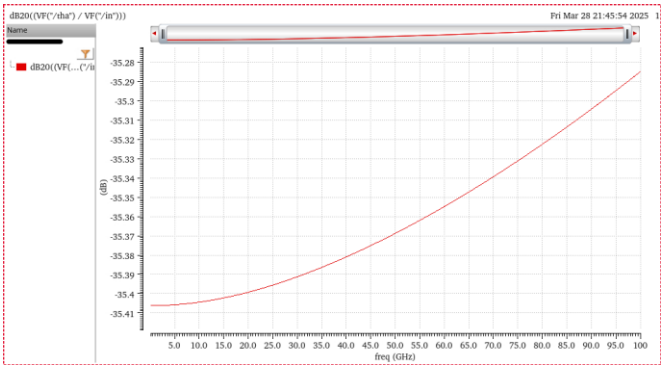

Fig.2 Isolation of the first track and hold mode over frequency

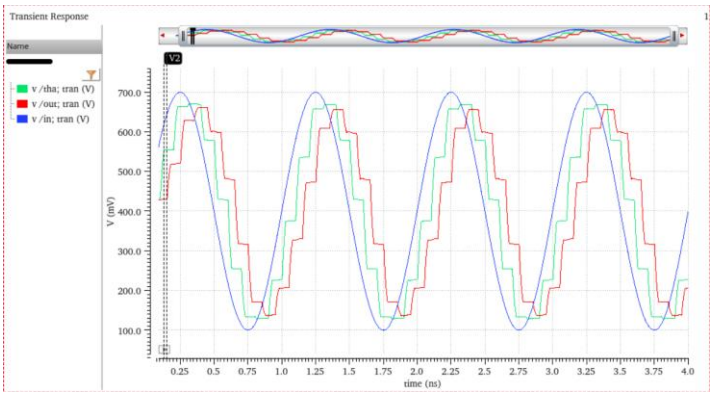

Fig.3 Waveforms at the input node (blue), T/H node (green), and S/H output node (red)

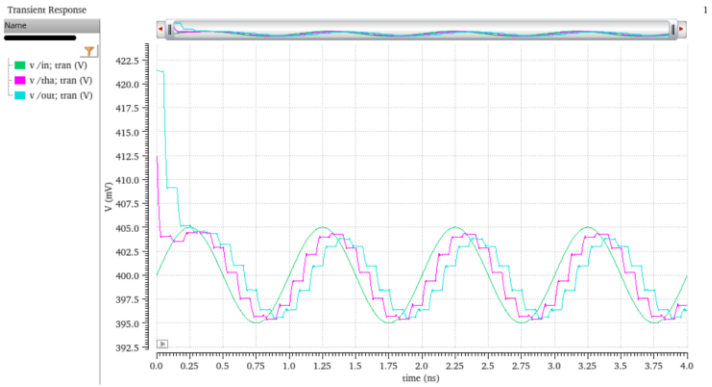

Fig.7 Waveforms at the input node (green), T/H node (purple), and S/H output node (blue)

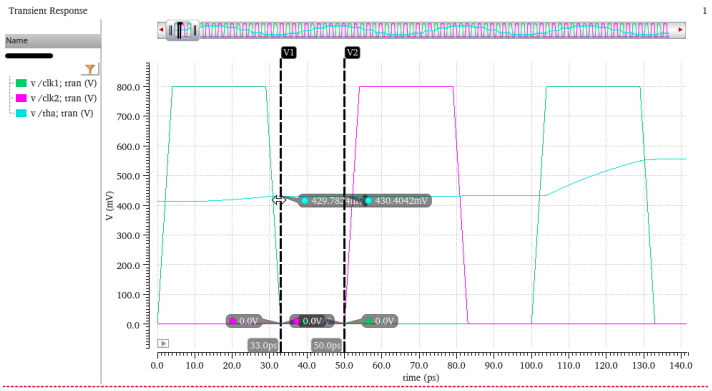

Fig.4 Pedestal value at the T/H node with 1GHz 300mV sinusoidal input signal

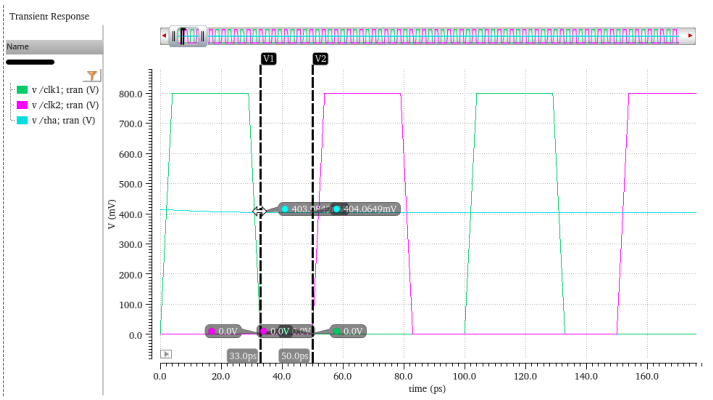

Fig.8 Pedestal value at the T/H node with 1GHz 5mV sinusoidal input signal

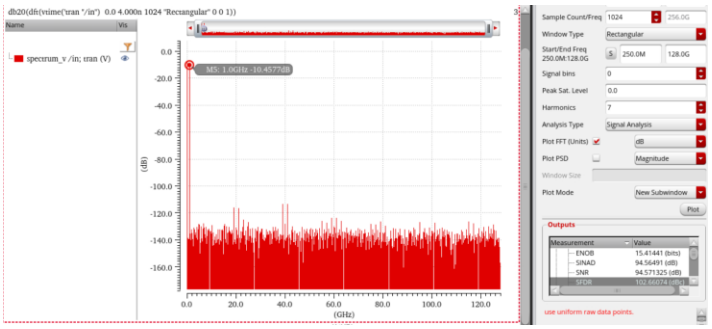

Fig.5 DFT spectrum at the input node with 300mV input amplitude. SFDR is 102.66dBc.

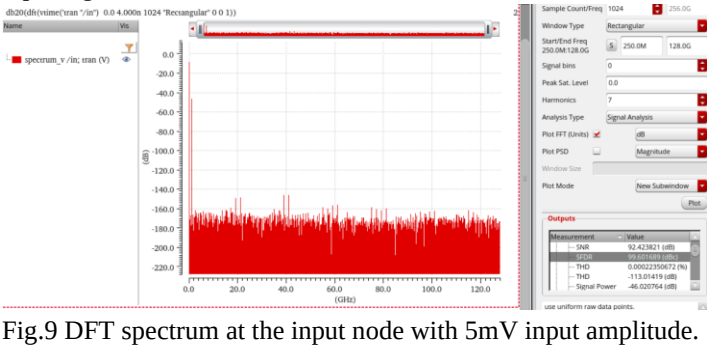

Fig.9 DFT spectrum at the input node with 5mV input amplitude. SFDR is 99.6dBc.

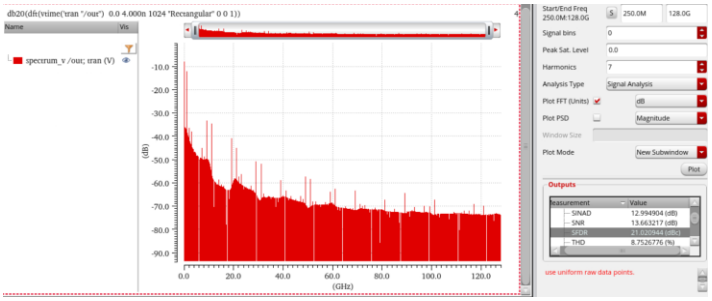

Fig.6 DFT spectrum at output node with 300mV input amplitude. SFDR is 21.02dBc.

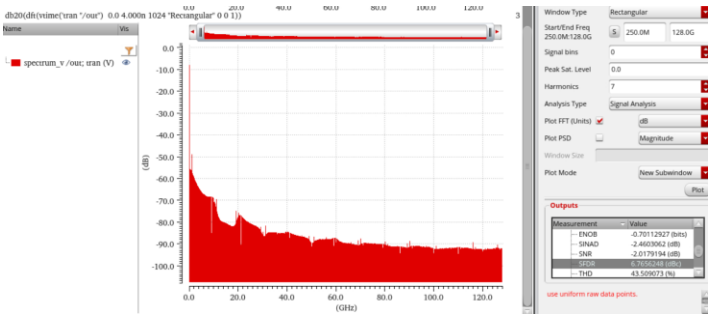

Fig.10 DFT spectrum at the output node with 5mV input amplitude. SFDR is 6.77dBc.

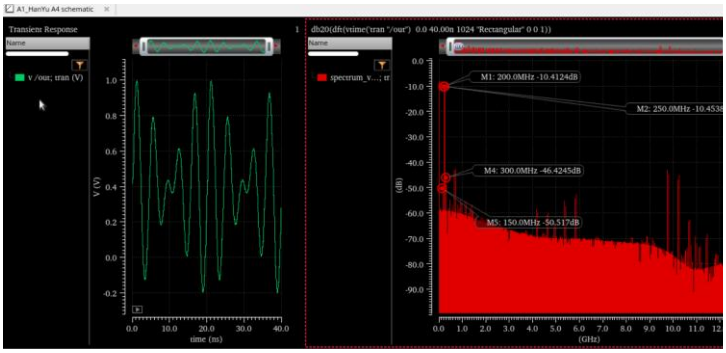

Fig.11 DFT spectrum at the output node with a 300mV two tone input at 200MHz and 250MHz

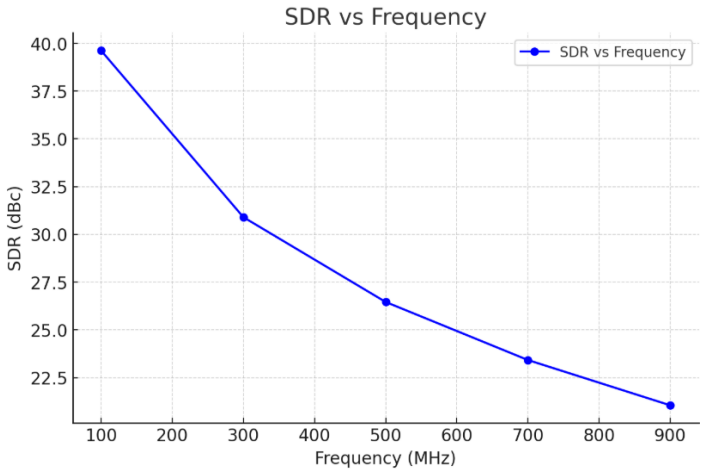

Fig.12 SDR as a function of frequency at 300mV input amplitude with 200MHz frequency steps