TS-960e SERIES

PXIE SEMICONDUCTOR TEST SYSTEM WITH TIMING PER PIN DIGITAL SUBSYSTEM

- 21-slot, PXI Express architecture provides high-performance digital, mixed-signal, and RF test capabilities in a compact, single chassis footprint
- Industry leading digital subsystem offers timing per pin architecture with sub-nanosecond edge placement & 64 time sets for no-compromise digital test capability
- Available with Keysight Technologies' comprehensive portfolio of PXIe RF instrumentation for addressing a wide range of RF applications
- Integrated platform includes ATEasy® test executive / test development software and comprehensive software tools for test development, debug, and file translation
- Bench top and integrated manipulator configurations

DESCRIPTION

The TS-960e PXI Express Semiconductor Test System is an integrated test platform that offers comparable system features and capabilities found in proprietary ATE systems. Available as a bench top system or with an integrated manipulator, the TS-960e takes full advantage of the PXI architecture to achieve a cost-effective and full-featured test solution for device, SoC and SiP test applications. The test system incorporates a high power (60 watts per slot), 21-slot, PXIe chassis and a custom-designed, performance test interface that supports the use of PCB DUT (Device Under Test) boards - a proven and high-performance method for interfacing to the device under test. Additionally, the receiver interface's pin blocks are field configurable, allowing users to upgrade the receiver when they modify or upgrade the system for new applications. The configuration of the receiver can support up to 512 digital channels, as well as a range of analog, device power supply (DPS) and RF resources.

The basic system includes 64, digital I/O channels; 64 static digital I/O channels; a programmable DPS; a system self-test and fixture; software for digital waveform editing / display; ICEasy - device test development tools; and Marvin Test Solutions' ATEasy software which provides an integrated and complete test executive and test development environment, allowing users to quickly develop and easily maintain test applications. With an additional 15 PXI slots available for digital, analog and RF test resources, the TS-960e is the ideal test solution for semiconductor OEMs, fabless semiconductor vendors, incoming inspection / counterfeit detection labs and packaging / test vendors needing a cost-effective, open architecture, configurable test system.

For production test applications requiring integration with an automated handler, the TS-960e is available with the Reid - Ashman OM1069 manipulator which provides precise positioning of the test head and the flexibility to interface to automated probers and device handlers. The manipulator's spring loaded design allows for easy alignment and docking to handlers - eliminating the need for a complex receiver interface. The TS-960e features a handler compatible slide receiver, which offers the flexibility to interface to virtually any device handler. In addition, fixture compatibility is maintained with both the TS-900 and TS-960 test systems, allowing users to interchange load boards between system types.

FEATURES

The base TS-960e platform uses the advanced GX5296 - a 3U PXI, 32 channel 125 MHz digital I/O card featuring timing and PMU per pin capability with sub-nanosecond edge placement resolution. A wide range of digital and analog instrument test options can easily be incorporated into the TS-960e, offering users a compact test system that can support both functional and DC parametric test capabilities. And with the incorporation of an integral, modular test interface, the TS-960e offers users an application ready test system which can be upgraded or reconfigured in the field if needed. The system is also supplied with various software development and digital vector conversion tools, including support for ASCII, WGL, STIL, VCD/eVCD and ATP vector formats.

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For RF test applications, the TS-960e is available with Keysight Technologies' comprehensive portfolio of PXIe RF instrumentation which can address a wide range of RF products & technologies including WLAN, Bluetooth, Cellular, EW, and RF transceivers. Available instrumentation options include Keysight Technologies' vector transceivers, vector signal analyzers and generators, and vector network analyzers; offering wafer and packaged RF test capabilities from 9 KHz to 27 GHz.

TS-960E CORE SYSTEM CONFIGURATION

The TS-960e core system includes the following test resources and capabilities:

- 21-slot, high-power PXI Express chassis with integral receiver interface
- Embedded i7 controller with Windows® OS
- 64 125 MHz digital channels with per pin PMU and per pin timing (expandable to 256)
- 64 static digital channels (expandable to 128), which can be used for fixture ID, UUT static control or DUT board relay control
- Programmable 0 to 48 V DPS (expandable to multiple channels)
- System self-test fixture and test program
- ATEasy test executive and programming environment
- Advanced digital waveform editing and display tool
- ICEasy test software development tools

SOFTWARE

The test system is supplied with ATEasy and all instrument drivers, virtual instrument panels, and a system self-test as well as ICEasy test software tools which facilitates device test development and characterization.   ATEasy supports a wide variety of Windows- based APIs including ATEasy, LabVIEW, CVI, Microsoft® and Borland® C/C++, Microsoft Visual Basic®, and Borland Delphi.

APPLICATIONS

- Design verification for devices and modules
- Pilot production and focused production test
- Automated failure analysis and test
- Counterfeit device detection
- RF component and module test

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SPECIFICATIONS

TS-960E PLATFORM

Number of Slots	1 controller, 8 PXI-1, 8 Hybrid, 4 PXIe
System CPU (Embedded)	Intel Core i7, 2.4 GHz, single slot controller 4x4 PCIe bus configuration 8 GB of RAM
System Hard Disk	320 GB (min)
CPU Interfaces	Front panel: • (2) USB, Ethernet Rear panel: • HDMI, USB
Cooling	Four 100 CFM fans for system cooling. Integrated temperature monitoring via an on-board microcontroller with audible and software notification when preset temperature limits are exceeded. Fan speed control and monitoring is automatic and can be controlled / monitored via the GxChassis software.
PXI Clock	Integrated 10 MHz PXI clock with auto-detect function. Presence of an external 10 MHz PXI clock will disable the internal clock. PXI clock is distributed to all peripheral slots. Optional external clock via slot 2
Temperature Monitoring	Per slot monitoring, 1 reading/sec/slot 4 second moving average value User selectable alarm criteria: • Maximum slot temperature • Average slot temperature Accuracy: ± 2 °C Default warning and shutdown limits: +50 °C & +70 °C Warning and shutdown limits programmable via software driver Status: Query via software driver and audible alarm for a warning limit condition
Power Supply Monitoring	Monitored voltages: 3.3, 5, +12, -12, VIO value Accuracy: ± 2% of reading
PXI Triggers	Slots: 2 – 21 Number: 8 per segment Software controlled segment mapping supports: • Isolate a trigger line within a segment • Map a trigger line left to right • Map a trigger line right to left
PXI Clock and Synchronization Resources	Integrated 10 and 100 MHz clock with an auto-detect function. Presence of an external 10 MHz PXI clock will synchronize the 100 MHz clock to the external 10 MHz source 100 MHz clock accuracy: ± 30 ppm Synchronization signals: SYNC100 & SYNC_CTRL
External 10 MHz Clock Input	An external 10 MHz clock source (TTL level) can be provided via a rear panel BNC or via a PXI Express System Timing Controller

10 MHz Clock Output	10 MHz output is available via a rear panel BNC connector, TTL compatible level
Slots	(1) PXI Express Controller (1) PXIe Timing Controller (3) PXI Express (8) PXI Hybrid (8) PXI-1
System Power	1600 W
Input AC Power	120 VAC, ±15%; 20 A max (PFC) 240 VAC, ±10%; 10 A max (PFC) 47 Hz to 440 Hz
UUT Interface	Modular, pogo-pin interface Supports up to 14 module blocks for digital, power, analog or RF applications Block connector interfaces: • 68 pin VHDC • 78 pin D-sub • 25 pin D-sub • SMA
Manipulator Option	Reid-Ashman OM-1069

DYNAMIC DIGITAL I/O SUBSYSTEM

Number of Digital I/O and PMU Channels	64 (base configuration)
Maximum Configuration	256 channels
Maximum Clock Rate	125 MHz
Drive Voltage Range	-2 V to +7 V, Drive Hi & Drive Lo, maximum swing is 8 V
Memory	64 Mb per channel
Data Output Formats (per channel)	Drive Hi, Drive Lo, Hi-Z Formatted Data: No return, Return to 1, Return to 0, Return to Hi-Z, Return to complement, Surround by complement; selectable on a per channel basis
Drive Data Timing (per channel)	Data assert / de-assert based on Phases 1-4
Capture Mode (per channel)	Mask Opening edge of Window Closing edge of Window Window – data is valid for entire window duration

Test Modes

Drive / Expect Mode	Output: Drive Hi, Drive Lo, Hi-Z Expect: 1, 0, OK, between states, or mask Keep last Toggle last

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Recording Modes (per sequence step)	Record errors for programmable inputs that have Good 1 & Good 0 Record errors for inputs that have only a Good 1 Record raw data based on NOT a Good 0 Record raw data based on a Good 1
Error Address Record	Record address for memory errors 1K deep error memory

Timing

Master Clock (PLL) Frequency Range	1 MHz (min); 125 MHz (max)
Resolution	5 digits
Accuracy	Greater of (±1 Hz or ±0.02% of programmed value) + accuracy of reference clock (PXI 10 MHz or external reference clock)
Jitter	±20 mUI of internal clock frequency, max
Reference	PXI 10 MHz clock or XClk (external clock) input
Clocks per Vector Range	Programmable, 1 to 256
Time Sets (TS0 - TS3)	4 phases, 4 windows; user assigned to DIO channels
Timing Set Sequence Control	64 Timing Sets with 4 Phases, 4 Windows, and 4 K sequence steps
Phase and Window Timing Resolution	1 ns, using the 125 MHz master clock
Minimum Phase / Window Pulse Width; Assert / Return Or Open / Close	5 ns
Phase / Window Reference	Phase: System or Pattern Clock (selectable per Seq Step) Window: Pattern clock only

External Status and Control Signals

Logic Levels	LVTTL or programmable level using one of the four Aux pin electronics channels.
Trigger Source	Software, PXI trigger bus, External event, External trigger input
Sync Outputs	Start of Sequence; Start of Sequence Step
Input Aux I/O Selections	Synthesizer reference clock, System clock, Break (System Clutch), Halt (Pattern Clutch), Sequence Jump signals
Output Aux I/O Selections	Phase, Window, Waveform, Syncs, Seqflag, Seq Active, Seq Idle, T0_Clk , Pat_Clk,

Sequencer

Commands	Jump, Conditional Jump, Loop, Call Subroutine, Return, Pause, Halt

Loop Counters	16, can be nested Only one can end on a sequence step Loop count range: 1 - 64K or continuous
Test Inputs	External: PXI triggers, Aux I/O Internal: Data sense, Edge or level
Sequencer Memory	4096 Steps
Phase Trigger	T0_CLK or PAT_CLK
Window Trigger	PAT_CLK
Patterns per Sequence Step	1 to 64M
Sequence Loop	1 to 1M, continuous
Current Step Loop	1-65535, continuous
Multi Step Loop	1-65535, nested 16 deep
Jump	Conditional / Unconditional
Jump Conditions	Error True, Sequence Timeout True, Signal Level (High / Low), Signal Edge (Rising / Falling)

Parametric Measurement (PMU)

Number of Parametric Measurement Units	32, one per channel 4, one per auxiliary channel (for timing /control & static I/O functions)
Configurations	Force Voltage/Measure Current (FVMI) Force Current/Measure Voltage (FIMV) Force Voltage/Measure Voltage (FVMV) Force Current/Measure Current (FIMI)
Force Voltage Range	-1.5 V to +7 V
Force Voltage Accuracy	±20 mV
Force Voltage Resolution	16 bits
Force Current Ranges	±32 mA, ±8 mA, ±2 mA, ±512 uA, ±128 uA, ±32 uA, ±8 uA, ±2 uA FS
Force Current Accuracy: Compliance Range: +1.75V to +7V @ 32 mA -1.5V to +7V @ no load	±120 uA, 32 mA range ±40 uA, 8 mA range ±5 uA, 2 mA range ±1.2 uA, 512 uA range ±600 nA, 128 uA range ±160 nA, 32 uA range ±80 nA, 8 uA range ±20 nA, 2 uA range

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Current Measurement Accuracy (60 Measurements / Sec) Compliance Range: +1.75V to +7V @ 32 mA -1.5V to +7V @ no load	±120 uA, 32 mA range ±40 uA, 8 mA range ±5 uA, 2 mA range ±1.2 uA, 512 uA range ±600 nA, 128 uA range ±160 nA, 32 uA range ±80 nA, 8 uA range ±20 nA, 2 uA range
Measure Voltage Range	-2 V to +7 V
Measure Voltage Accuracy	±1 mV (measurement rate < 200 measurements / sec)
High and Low Commutation Voltage Range	VCLo: -2 V to +5 V VCHi: 0 V to +7 V
Voltage Clamp Accuracy	±100 mV

STATIC DIGITAL INSTRUMENT

Number of Static Digital I/O Channels	64, expandable to 128 48 Input/Output (programmable I/O in groups of eight) 16 inputs for fixture ID
Logic Levels	LVTTL compatible
Source / Sink Current	24 mA (max)

USER POWER

Configuration	Single channel, floating output with remote sense
Programmable Voltage Range	0 to 48 V
Output Voltage Accuracy	±0.2%, ±25 mV
Output Noise	1.5 mV$_{RMS}$, 6 mV$_{PP}$, full load. Measurement BW 1 MHz
Output Current	2 A @ 20 V, 0.8 A @ 48 V
Current Limit Range	0 to 2 A, 34 μA resolution
Current Readback Accuracy	±0.2% of reading, ±5 mA
Voltage Readback Accuracy	±0.1% of reading, ±10 mV
Remote Sense Voltage Difference	Up to 0.25 V for each connection

SOURCE / MEASURE UNIT (SMU) OPTION

Configuration	4-channel, 4 quadrant operation, isolated outputs, common ground, with remote sense
Programmable Voltage Range	0 to ±20V
Output Voltage Accuracy	±0.05% of programmed value + 2 mV
Output Noise	<20 mV p-p, 20 MHz BW, full load
Output Current	±2.5 uA to ±250 mA in decade ranges, any one channel can supply up to 1A
Output Current Accuracy	±0.05% of programmed value + 0.05% of FS
Voltage Measurement Accuracy	±0.03% of programmed value + 2 mV
Current Measurement Accuracy	Ranges: 2.5 uA to 250 mA in decades Accuracy: ±0.05% of reading + 0.05% of FS range
Measurement Resolution	Programmable, 18 to 24 bits

RF INSTRUMENTATION OPTION

Keysight Technoloogies Signal Analyzers	M9420A, Vector Transceiver M9421A Vector Transceiver M9393A, Vector Signal Analyzer M8381A, Vector Signal Analyzer
Keysight Technologies Vector Network Analyzers	M9485A, Multi-port, VNA M9370A Series, VNA
Keysight Technologies Signal Generators	M9830A, CW Signal Generator M9381A, Vector Signal Generator

ENVIRONMENTAL

Operating Temperature	0 °C to +50 °C
Storage Temperature	-20 °C to +60 °C
Relative Humidity (Non-Condensing)	90%
Altitude	30,000 ft
Weight	100 lbs, core system
Chassis Size	22" D x 17.5" W x 14" H

Note: Specifications are subject to change without notice

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ORDERING INFORMATION

TS-960e	PXIe Semiconductor Test System with Timing per Pin Digital Subsystem
TS-960e-OM	PXIe Semiconductor Test System with Timing per Pin Digital Subsystem & manipulator
OPTIONS	
TS-960-OPT64	64 Additional Dynamic Channels for use in TS-960

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