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AXIe DD192

Digital 192 Channel (DD192) Pin Card

AXIe 3.1 Compatible Instrument with 192 Flexible Digital Channels

DD192 Pin Card Features

- 192 digital channels with per pin PMUs
- 2 1G x 64 bit wide 1333MTps DDR3 SODIMMs
- AXIe 3.1 compatible
- PCIe 4 lane GEN2 endpoints

Driver, Comparator & Load Features

- 3 level driver (Vih, Vil, Vtt)
- Single level comparator (Voh)
- -1.5v to +6.0v Range
- Active load up to 12mA source and sink

Per Pin PMU Features

- Force V, Measure I; Force I, Measure V
- Voltage clamps
- 5 current ranges (2uA to 20mA)
- -1.5v to +6.0v Range
- Hardware measurement averaging

Pattern Generator Features

- 128M deep vector memory
- 12 unique 2G SCAN chains (Drive & Compare) per board
- 24 unique 8 bit wide Source/Capture engines per board with a 128K deep Source/Capture memory per engine
- Match mode, parallel and serial
- Industry standard micro-instructions for pattern control
- Flexible mixed signal triggering

Timing & Formatting Features

- 100 Mvps data rates
- 32 per pin flexible edge sets, 1.25nS resolution
- 32 period sets (10ns to 500mS periods)
- 127 global timing sets on-the-fly
- Strobe compare format
- Flexible drive formats supporting mixed-signal applications
- 2 flexible per pin edges for unique drive formats
- 2 flexible per in edges for unique compare formats

Applications

- Characterization and Validation, Wafer Sort, Final Test
- Multi-Site Automated Production Test
- Low-cost IC Test
- Mixed Signal Test

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1 General Description

The digital system supports up to 192 channels of sequencer controlled digital vectors operating at DUT vector rates as high as 100Mvps with per pin timing, formatting and levels.

Each DD192 has four sequencer controllers with pattern generators, and integrated timing generators connected to integrated pin electronics. The DD192 pin card can operate as 4 independent 48 channel sub-systems, synchronized as 2 independent 96 channel sub-systems, synchronized as an independent 192 channel subsystem, or synchronized with other pin cards controlled by a separate Digital Synchronization Module provided on the System Module installed in the system backplane.

Each DD192 Pin Card has 24 Digital Source & Capture engines. Each engine can operate either independently across 8 channels, or be grouped together to form a larger source or capture segment for wider busses. Also, each source and capture engine can be configured to operate in serial mode (LSB or MSB first). Each source and capture engine has access to 128K deep memory, shared between one source and one capture engine, providing ample storage capability.

As part of the AXIe standard, each DD192 Pin Card has an Intelligent Platform Management Controller for the measurement and monitoring of board voltage levels, device temperatures, general board temperature, and board identification via the Field Replaceable Unit (FRU) EEPROM.

The DD192 pin card has 3 main components:

1. (2) Digital Segments, each with a dedicated FPGA (DSEG0 and DSEG1), each FPGA supporting dual 48 digital channel subsystems with per pin PMUs.
2. The Interface FPGA.
3. The Intelligent Platform Management Controller (IPMC).

The Digital Segments:

Each digital segment supports the follow:

1. A single 1G x 64 bit wide 1333Mtps DDR3 SODIMM.
2. 96 channels with integrated programmable level drivers, comparators, loads (DCL) and per pin parametric measurement units (PPMUs) otherwise referred to as the Pin Electronics (PEs).
3. PPMU Measurement System consisting of an ADC per 16 Digital Channels.
4. A PCIe 4 lane GEN2 endpoint for fast test computer communications.
5. A Trigger interface to the Interface FPGA utilizing the DSTAR trigger bus on the AXIe 3.1 backplane.
6. A Fail and Synchronization interface to the Interface FPGA.
7. Two 48 channel Digital Subsystems each with a micro sequencer based engine.

The Interface FPGA:

The Interface FPGA provides the following interfaces on the DD192 Pin Card:

1. The SPI interfaces for the 192 channel Digital Segment Pin Electronic devices.
2. The SPI interfaces for the 12 ADCs associated with the 192 digital channel PPMU measurement system.
3. A Trigger interface to the 2 DSEG FPGAs and to the AXIe 3.1 DSTAR Trigger Interface to the backplane.
4. A Fail and Synchronization interface to both DSEG FPGAs.
5. An I^2C interface to the programmable clock system.
6. An I^2C interface to the Programmable power supply system.
7. A PCIe 1 lane GEN1 endpoint for fast test computer communications.

The Intelligent Platform Management Controller (IPMC):

The IPMC provides the following capability:

1. Power System Voltage Monitoring Interface:
    i. An I^2C interface to the Programmable power supply system for the purpose of monitoring the voltage levels of all programmable power supplies.
    ii. ADC Interface for measuring fixed power system voltages.
2. A temperature measurement system used for monitoring the temperatures of the following devices:
    i. All 96 Dual PE devices associated with the 192 digital channels.
    ii. Both DSEG FPGAs
3. I^2C interface to the Field Replaceable Unit (FRU) EEPROM

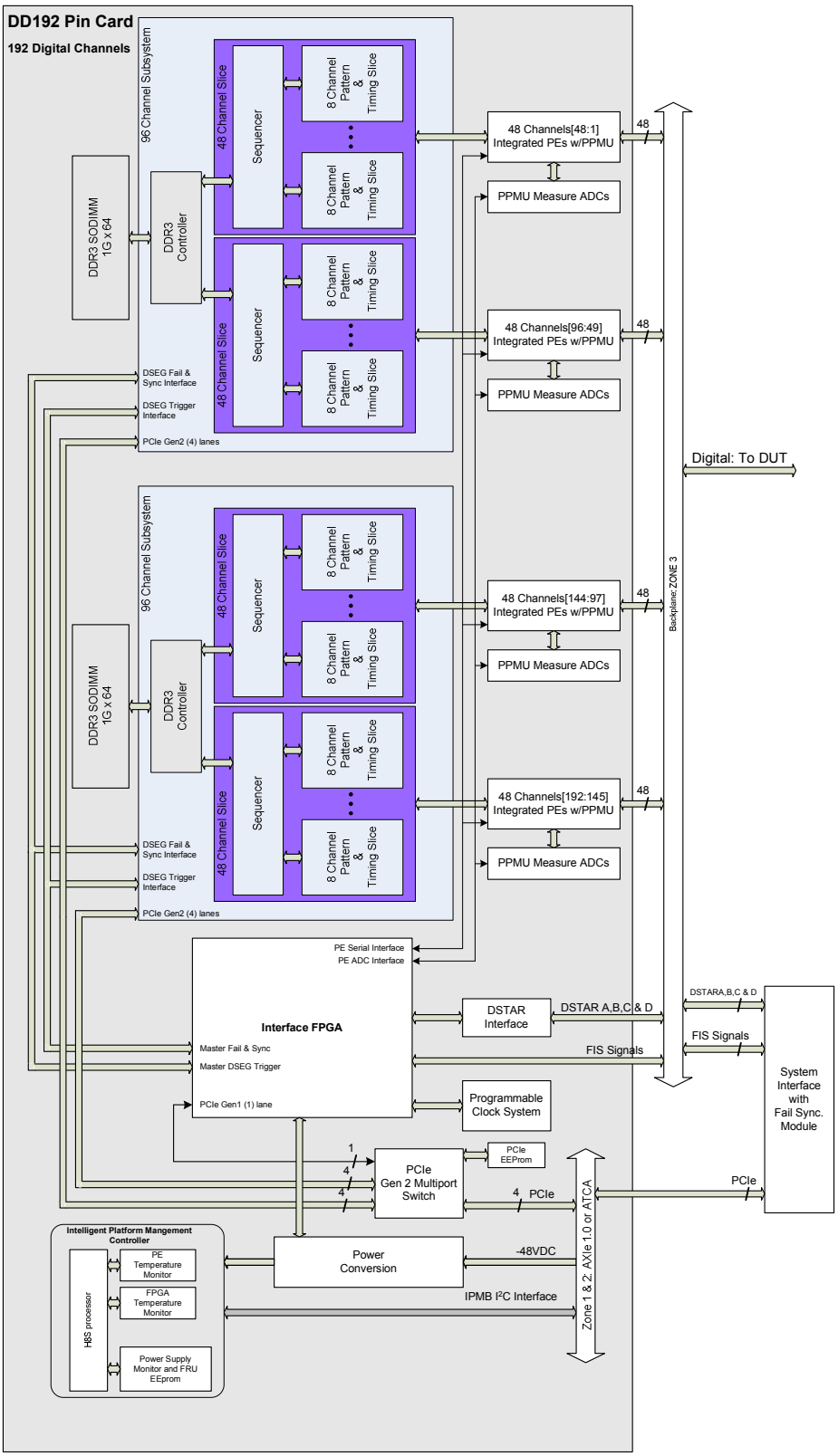

Figure 1: DD192 Pin Card Block Diagram

2 Timing & Formats

The timing architecture provides an on-the-fly selection of 127 timing sets. A timing set specifies 1 of 32 global period sets and a per pin edge set. A global period set map is used to map the 127 possible timing sets to 32 on-the-fly period sets during pattern execution. The per pin edge set map is used to map the 127 possible timing sets to one of 32 on-the-fly edge sets.

2.1 Clock Generation

The digital subsystem clock source is provided by a 100MHz clock and can be phase locked to an external 10MHz coherent reference.

2.2 Period Generation

The period generator has up to 32 period sets which can be changed on-the-fly during pattern execution. Each period set consists of a T0 period duration and an integer number of C0 periods to be sourced during the T0 period. The minimum period for T0 and C0 is 10ns.

Each channel can be referenced to either the T0 or the C0 cycle. The T0 cycle is the default reference cycle for all channels. The T0 cycle represents the base vector rate for Sequencer instructions while the C0 cycle allows clock channels to operate at a higher rate than data channels. Channels referenced to the C0 cycle must be drive ONLY.

The DUT period and T0 Period is described below for each of the marker modes:

T0 Sequencer Rate:		
T0 Frequency Range T0 Period Range T0 Period Resolution	2Hz to 100MHz 500mS down to 10nS 1.25nS	Edge placement is limited to 163.8uS
DUT Data Rate:	100Mvps Max.	Equal to T0 Frequency
DUT Period	10.0nS Min.	Equal to 100% of T0 Period
Number of Period Sets	32	

2.3 Edge Generation

2.3.1 Timing Generators per Channel

A digital channel has 2 drive and 2 compare edges per DUT cycle supporting NRZ, Return-to, clock and static drive formats as shown below:

2.3.1.1 Drive Format Capability

Format Name	Description
NRZ	Non-Return to Zero
NRZC	Non-Return to Zero, complement
RZ	Return to Zero
RZC	Return to Zero, complement
RO	Return to One
ROC	Return to One, complement
RT	Return to Tri-state
RTC	Return to Tri-state, complement
CLK	Clock High independent of pattern data
CLKC	Clock High Complement independent of pattern data
HI	Drive High independent of pattern data
LO	Drive Low independent of pattern data
OFF	Driver Tri-State independent of pattern data

2.3.1.2 Receive Format Capability

Format Name	Description
Strobe	Compare Edge Strobe

2.3.1.3 Pass/Fail Generation

Compare	Description
High	Above Voh
Low	Below Voh
Mask	Don't compare

2.3.2 Edge Range

Minimum: 0 nS
Maximum, the smaller of 2*(T0 Cycle) or 163.8uS

2.3.3 Edge Resolution

Edge resolution 1.25nS

2.3.4 Edge Placement Accuracy

Edge:

D0 & D1 (Drive Edges)	± 500pS
C0 & C1 (Compare Edge Strobe)	± 500pS

Note:

1. Edge placement accuracy applies at the DUT I/O connector of the test head when driving zero or one and comparing high or low at 3V.

3 SCAN Testing

Scan vector data and linear pattern data share the LVM. A SCAN channel's vector data is linked to 8 channels of LVM. Each DD192 pin card allows up to 12 independent SCAN chains where each SCAN chain has a SCAN IN and SCAN OUT channel. In addition, each SCAN IN and SCAN OUT channel can be connected to a maximum of 8 channels supporting multisite applications.

SCAN IN (Drive) Channel:

Pin State	Driver State
0	Low
1	High
X	Hiz

SCAN OUT (Compare) Channel:

Pin State	Compare Expect
0	Low
1	High
X	Mask

SCAN Memory Depth

SCAN Chains	Vector Depth	SCAN IN Channels/DD192	SCAN OUT Channels/DD192	Max. SCAN
12	2G	24 (max)	24 (max)	100Mvps

3.1 Pattern Control

3.1.1 Cycle Counter

The 32 bit cycle counter contains the number of cycles executed by the pattern. Since the pattern can have repeat instructions, the number of vectors in a pattern and the number of cycles executed is often different.

3.1.2 Fail Counter

The 32 bit fail counter contains the number of failing cycles executed by a pattern.

3.1.3 History Ram

The 1K deep History Ram (HRAM) is used to capture the state of the system during pattern execution. The HRAM is used during pattern debugging. There are several modes of operation:

1. Trigger on pattern label (address)
2. Trigger on pattern cycle
3. Capture all cycles or vectors
4. Capture only failing cycles
5. Capture the first 1K triggered cycles
6. Capture the last 1K triggered cycles

3.1.4 Keep Alive Operation

Keep Alive operation is supported by allowing a pattern of any size to execute while modifying unused memory locations.

4 Waveform Source and Capture

Each DD192 pin card contains 24 8-bit Source and 24 8-bit Capture engines configured in source/capture engine pairs. Each source and capture engine pair has 128K deep memory per channel that can be used to source or capture serial or parallel data, controlled by the digital pattern. The Source and Capture engine pairs can operate independently of each other, and can also be combined with other Source & Capture engine pairs to form larger parallel busses.

The Source and Capture engines are generally useful for ADC and DAC testing, for general serial busses, and for DUT configuration register setup and testing.

5 Programming

- Drivers for C++, LabWindows/CVI
- Inherent support for multi-site, pattern and waveform editing, and debugging.

6 Specifications

DD192 Overview	
I/Os per board:	192 digital channels
192 Digital Channels	Per pin three level driver (Vih, Vil, Vt), Per pin comparator (Voh), Per pin active current load (Iol, Ioh, Vc), Per pin PPMU with an ADC per 16 channels
Date Rate:	100Mvps
Source/Capture Engines	1 per 8 channels, 24 total per board
SCAN Pattern Engines	1 per 16 channels, 12 total per board
PMU Measure ADC	1 per 16 channels, 12 total per board
Mixed Signal Triggers	4 per board: DSTAR_A, DSTAR_B, DSTAR_C, DSTAR_D
Vector Memory	128M deep per channel
Source/Capture Memory	128K deep per Source/Capture Engine
SCAN Pattern Memory	2G deep per SCAN Pattern Engine (Max)
History Memory	1K deep per channel
Micro Instructions:	NOP, REP, HALT, LCNT, ENDL, JMP, JMPI, CJMP, JSR, CJSR, JSRI, RET, RCODE, CWAIT, HALT
Nested Subroutine Levels	16
Nested Loop Levels	16
T0 Period (Max)	500mS with edge placement to 163.8uS
Period Sets	32 global
Timing Sets	127 global
Edge Sets	32 per channel
Edge Placement Resolution	1.25nS
Edge Delay (Max)	163.8uS
Edge Placement	0 to 2x period with no dead time
Timing Edges per channel	4 flexible edges: 2 for drive and 2 for compare
Period Resolution:	1.25nS
Compare Formats	Strobe
Drive Formats	NRZ, NRZC, RZ, RZC, RO, ROC, RT, RTC, CLK, CLKC, HI, LO, OFF
Test Computer Communication Port:	PCIe: • PCIe 4 Lane GEN 2 from backplane to Multiport Switch • 2 PCIe 4 Lane GEN 2 endpoints, 1 per 96 digital channels • PCIe 1 Lane GEN 1 endpoint to Interface FPGA
Triggers	AXIe 3.1 compatible bidirectional backplane triggers: • DSTAR_A • DSTAR_B • DSTAR_C • DSTAR_D
Intelligent Platform Management Bus (IPMB)	Chassis Health Monitor subsystem used to monitor DD192 voltage and temperatures.

6.1 Driver, Comparator, Load (DCL)

Driver (3 Level Driver)	
Voltage Levels:	Driver Range: -1.5V to +6.0V Vil: -1.5V to +5.9V Vih: -1.4V to +6.0V Vtt: -1.5V to +6.0V
Voltage Accuracy	±30mV (-2.0V to 6.0V)
Voltage Resolution	244 uV (-2.0V to 6.0V)
Minimum Voltage Swing:	50mV (Typ.) into a 50 Ohm load
Driver ON Resistance:	50 Ohms (Typ.)
Drive Current (DC):	±75mA
Leakage Current (OFF)	20nA

Comparator (Single Level Comparator)	
Voltage Levels:	Comparator Range: -1.5V to +6.0V Voh: -1.5V to +6.0V
Voltage Accuracy:	±25mV
Voltage Resolution:	122 uV (Typ.)
Minimum Voltage Swing:	100mV

Reflection Clamps	
Voltage Levels:	Clamp Range: -2.0V to +6.5V Vclo: -2.0V to +5.7V @ 1mA Vchi: -1.2V to +6.5V @ 1mA
Voltage Accuracy:	±(0.7% + 8mV)
Voltage Resolution:	1mV (Typ)
Voltage Clamp Current:	±60mA (min)

Current Load	
Current Levels:	Current Range: ±12mA Iol: 12mA Ioh: 12mA
Current Accuracy:	±(0.5% + 85uA)
Current Resolution:	2uA (Typ)
Commutation Voltage:	-1.75V to +5.75V
Commutation Voltage Accuracy:	±(0.2% + 10mV)
Commutation Voltage Resolution:	244uV (Typ.)

6.2 Per Pin PMU

PPMU FV/MI	
Force Voltage Range:	-1.5V to +6.0V
Force Voltage Accuracy:	±20mV
Force Voltage Resolution:	122uV
Measure Current Ranges:	20mA, 1mA, 100uA, 10uA, 2uA Average Measurements: • Period: 20uS to 500mS • Period Resolution: 1uS • Number of Samples: 1 to 64K

20mA	±(0.8% + 200uA + 6uA/V)
1mA	±(0.3% + 5uA + 0.4uA/V)
100uA	±(0.3% + 300nA + 40nA/V)
10uA	±(0.3% + 60nA + 4nA/V)
2uA	±(0.3% + 40nA + 1nA/V)
Measure Current Resolution:	
20mA	4uA (Typ.)
1mA	258nA (Typ.)
100uA	17nA (Typ.)
10uA	4nA (Typ.)
2uA	258pA (Typ.)

PPMU FI/MV	
Force Current Ranges:	20mA, 1mA, 100uA, 10uA, 2uA
Force Current Accuracy:	
20mA	±(0.8% + 200uA + 6uA/V)
1mA	±(0.4% + 5uA + 0.4uA/V)
100uA	±(0.4% + 200nA + 40nA/V)
10uA	±(0.4% + 40nA + 4nA/V)
2uA	±(0.4% + 20nA + 1nA/V)
Force Current Resolution:	
20mA	488nA (Typ.)
1mA	31nA (Typ.)
100uA	12nA (Typ.)
10uA	122pA (Typ.)
2uA	31pA (Typ.)
Measure Voltage Range:	-1.5V to +6.0V Average Measurements: • Period: 20uS to 262mS • Period Resolution: 1uS Number of Samples: 1 to 64K
Measure Voltage Accuracy:	±20mV
Measure Voltage Resolution:	129uV
Voltage Clamps:	Clamp Range: -1.5V to +6.0V Vcl: -1.5V to +4.0V Vch: -0.0V to +6.0V
Voltage Clamp Accuracy:	±200mV (High Clamp: -0.5V to 3.5V) ±300mV (High Clamp: -1.5V to 6.0V)

6.3 General Specifications

Power Consumption	48VDC @ 6.25A
Compliant with	AXIe-3.1
Operating Environment:	
Ambient Temperature:	20℃ to 27℃
Humidity:	30% to 60% relative humidity
Storage Temperature:	-40℃ to 70℃
Weight:	1.36kg (3.0 lbs)