Design and Optimization of a 500 MHz Low-Noise Amplifier (LNA)

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Abstract

This project presents the design, implementation, and optimization of a Low Noise Amplifier (LNA) operating at 500 MHz. The main objective was to minimize input and output reflections while maintaining sufficient gain, using a combination of simulation in Keysight ADS, Smith Chart analysis, and laboratory validation with a vector network analyzer. Several impedance-matching strategies were tested, evolving from theoretical Tapped-C networks to practical LC networks, to achieve improved system performance.

Introduction

Low Noise Amplifiers are fundamental in RF input stages, boosting weak signals while introducing minimal additional noise. The aim of this project was to design a 500 MHz LNA (see Figure 1), optimize its S-parameters, and experimentally validate its performance.

The methodology followed three stages:

1. Biasing circuit design to establish correct transistor operation.
2. Simulation of S-parameters without matching networks as a reference.
3. Design and tuning of input/output matching networks to minimize reflections and ensure maximum power transfer.

The Smith Chart played a central role in visualizing impedance mismatches and guiding iterative adjustments of capacitors and inductors.

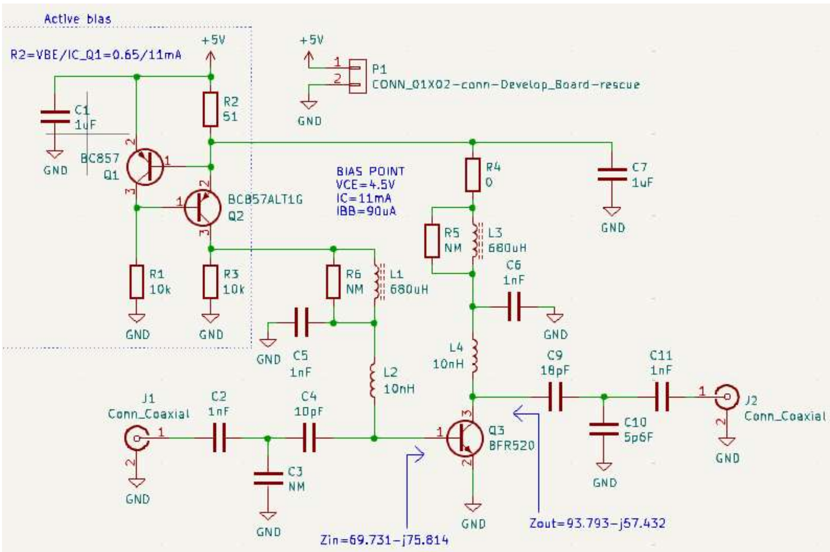

Figure 1. Schematic of the LNA.

System Design

The amplifier used a BFR520 high-frequency NPN transistor as the active device, biased through a current-source circuit built from BC857 transistors (see Figure 2). Passive components, such as resistors, inductors, and capacitors were carefully dimensioned to establish the correct operating point.

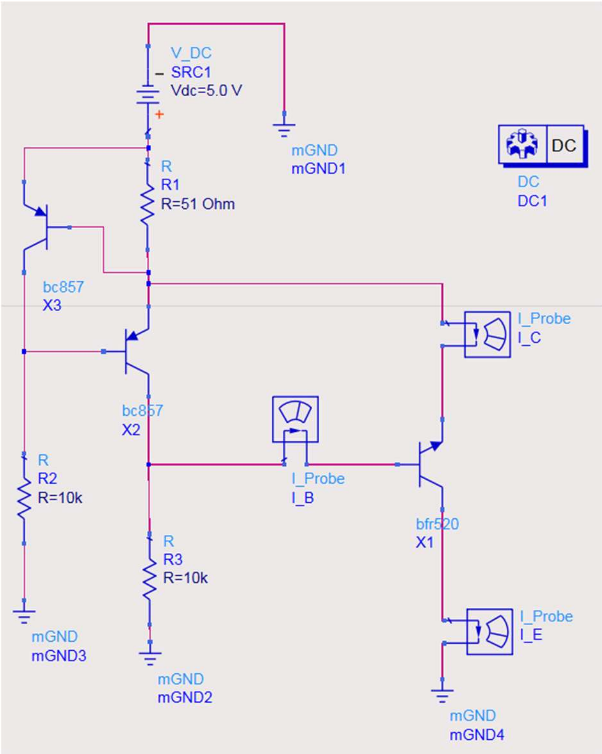

Figure 2. Polarization circuit.

As shown in Figure 3, initial ADS simulations revealed that:

- S21 (gain) was around 20 dB over a broad frequency range.
- S12 (reverse isolation) remained at approximately –20 dB or lower.
- S11 and S22 (input/output reflection) deviated from the 50 Ω reference at higher frequencies, highlighting the need for matching networks.

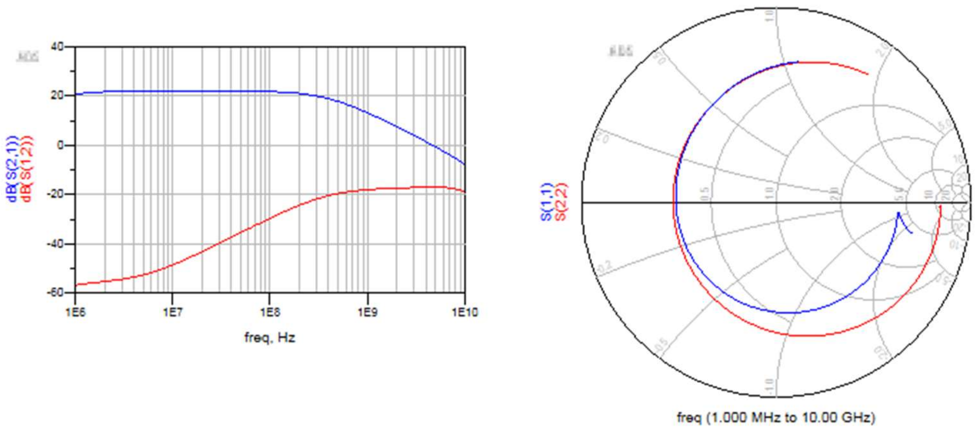

Figure 3. Simulated S-parameters.

A Tapped-C topology was first chosen for both input and output matching, as it fit theoretical requirements and PCB layout constraints. Values were optimized for 500 MHz, and Smith Chart plots confirmed an improved match in simulation.

Implementation & Results

Once the PCB was assembled, real measurements were performed with a Vector Network Analyzer (VNA). Discrepancies appeared between simulated and measured results due to parasitics and manufacturing tolerances.

Without any matching, S11 was approximately –12.6 dB and S22 around –10.1 dB at 500 MHz (see Figure 4).

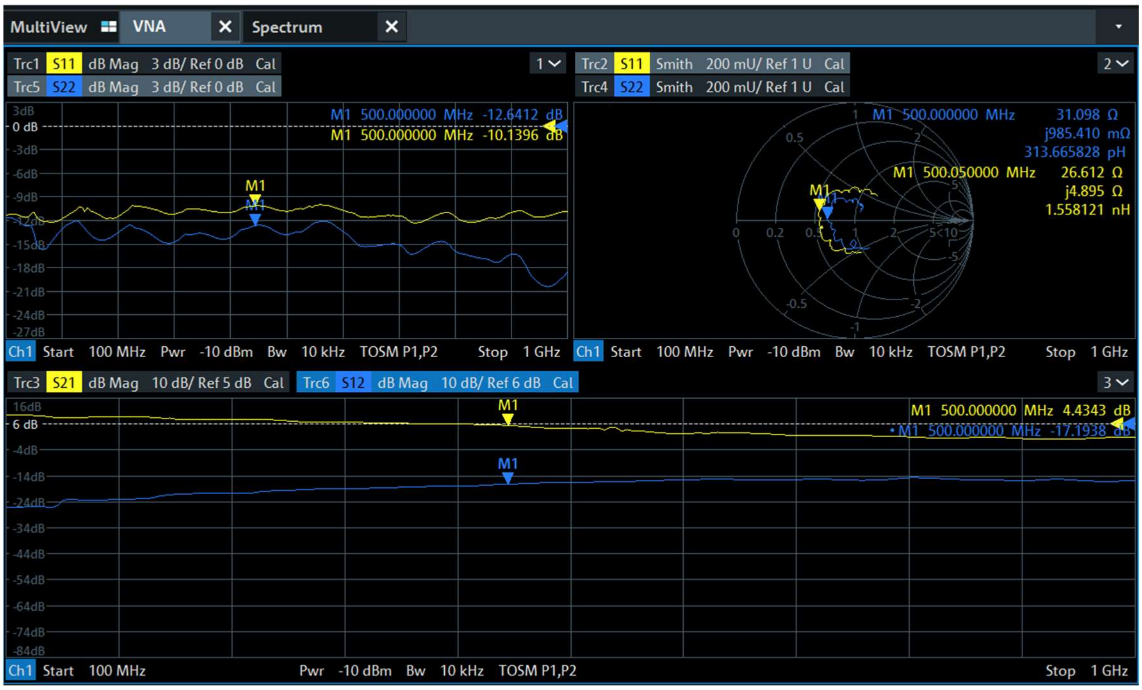

Figure 4. Initial measurements without matching network.

Introducing the first LC matching network improved S22 to –15 dB, however, S11 degraded to –9 dB. Iterative adjustments of the inductance and capacitance shifted the resonant frequency closer to 500 MHz. After several refinements, S11 reached –15.2 dB and S22 –14.8 dB around the target frequency (see Figure 5).

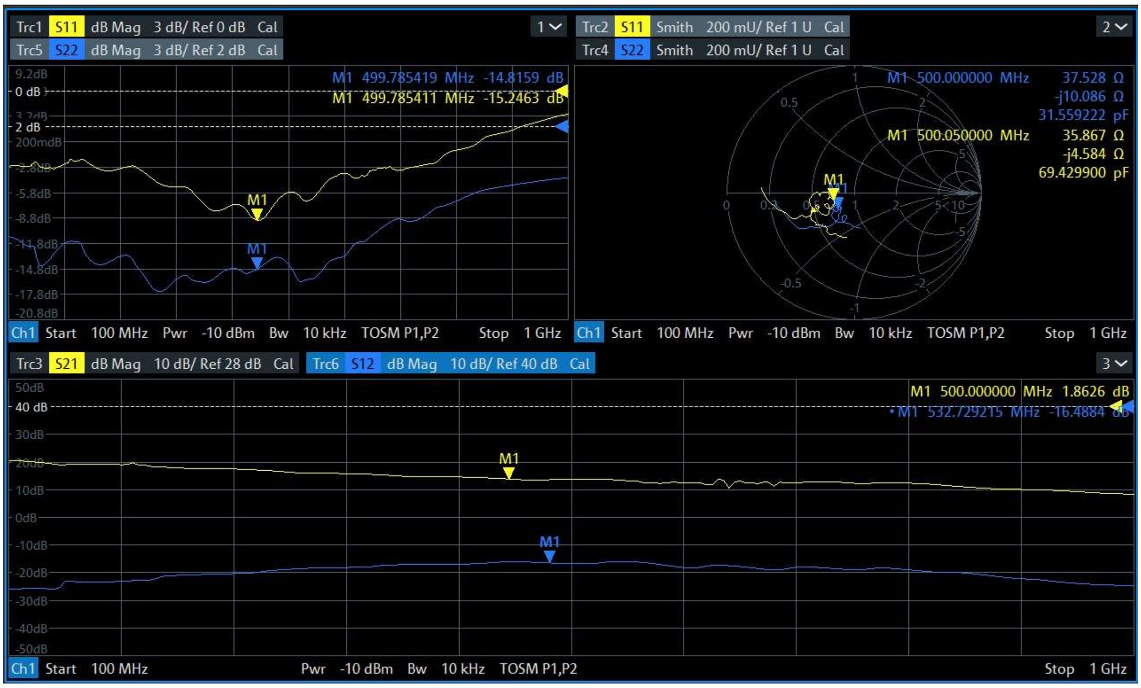

Figure 5. Measurements after tuning the LC matching network.

Transmission gain (S21) stabilized between 1 and 4 dB depending on the configuration, while isolation (S12) remained below –16 dB.

In a final experiment, two 4.7 kΩ resistors were added in parallel with the matching coils. This increased the gain to approximately 4 dB but worsened reflections, demonstrating the strong interdependence of parameters in RF design.

Conclusion

The project successfully demonstrated the full cycle of LNA design, from theoretical biasing and matching to practical optimization of S-parameters. Through simulations, Smith Chart analysis, and laboratory validation, the amplifier achieved acceptable reflection coefficients (S11 ≈ –15 dB, S22 ≈ –14 dB) and useful forward gain at 500 MHz.

The project highlighted the importance of iterative fine-tuning in RF design, where every change in components influences the entire system response. This work strengthened skills in ADS simulation, impedance matching, spectrum analysis, and practical circuit debugging, essential competences for RF and microwave engineering.