**Operating Systems**

**Homework #1-Part A**

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| **Name:** | Yan Yu |

**Part A: Computer System Overview**

1. Using the image in section titled "Interrupts", Stallings textbook, chapter 1, briefly describe the various steps involved in interrupt driven I/O. Ensure your description includes brief descriptions about the following terms: PSW, interrupt controller, PC, and control stack. [**2 points**].

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| 1. The hardware issues an interrupt signal to the processor 2. The processor finishes the current instruction before responding to the interrupt 3. The processor checks for pending interrupt requests, determines that if there is any interrupt needs to respond to, if there is one, the processor will send an acknowledgement signal to the corresponding hardware which issued the interrupt. The acknowledge allows the hardware remove the interrupt signal. 4. The processor then starts preparing to transfer the control to the interrupt toutine. To begin, it saves the information needs to resume the current program at the point of interrupt. The program status word(PSW) and the memory address of the next instruction to be executed (contained in PC) will be push into the control stack. 5. The processor then loads the entry location of the interrupt-handling routine into the program counter. Once the program counter has been loaded with new value, the processor proceeds to next instruction cycle, which begins with and instruction fetch. Because the instruction is determined by the program counter, the control then is transferred to the interrupt-handler program. 6. Up to this point, the program counter and PSW relating to this interrupted program have been saved on the control stack. And then, all of the registers related to program being interrupted also will be saved into the control stack. The stack pointer inside the CPU will be updated to point to the new top of the control stack, at the same time, the program counter is also updated to point to the beginning of the interrupt service routine. 7. Next, the interrupt handler may proceed to process the interrupt. |

1. Briefly describe (1 sentence will suffice) each one of the following terms: [**8 points**]
   1. PC

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| PC stands for program counter which stores the next instruction to be fetched from memory |

* 1. IR

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| IR stands for instruction register which stores the instruction loaded from memory |

* 1. AC

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| AC stands for accumulator which is a temporary storage. |

* 1. SIMD

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| SIMD stands for single instruction multiple data, which describe the ability that one instruction can process multiple data |

* 1. ISR

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| ISR stands for interrupt service routine which is responsible for handling the interrupt issued by hardware etc. |

* 1. Using the image in section titled “Interrupts” in Chapter 1, mention name of three stages and write one line description of the function of each one of the 3 stages.

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| 1. fetch stage – fetch instruction from memory  2. execution stage – execute instruction loaded from memory  3. interrupt stage – check for if there is any pending interrupt signal |

1. Provide suitable response to each of the following questions regarding a modern PC.
   1. What is the expansion of the acronym RAM? What is DDR RAM? [**1 points**]

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| RAM stands for random access memory  DDR RAM stands for double data rate random access memory |

* 1. What is the expansion of the acronym ROM? What is the difference between RAM and ROM? [**1 points**]

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| ROM stands for Read-only memory  RAM is voltage memory and ROM is non-voltage memory |

* 1. What is a microprocessor aka CPU? List at least 3 major subcomponents of a CPU? [**2 points**]

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| CPU stands for central processing unit  Often, inside CPU, the major components are PC, IR, MAR, MBR, cache etc. |

* 1. What is a dual-core or multi-core CPU? [**1 point**]

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| Two or more processors (cores) are combined into one single piece of silicon. (each core contains all the components of an independent processor) |

1. Complete the missing values in each row of the following table using the indicated value. The first row of the table is already filled-in to illustrate an example. [**7 points**]

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| **Value in decimal** | **Value in 8-bit 2’s complement binary** | **Value in 8-bit hexadecimal** |
| -110 | 1111 11112 | FF16 |
| -128 | 1000 00002 | FF80 |
| 127 | 01111111 | 7F16 |
| -510 | 11111011 | FFFB |
| 85 | 0101 01012 | 55 |

1. Describe (4 to 5 sentences) the little endian storage scheme used in x86 processors using a suitable example. [**3 points**]

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| Endian storage scheme is a type of byte order scheme, the requested address (0) points to the lower order byte of the result, and the higher order byte of the result is taken from the next higher sequential address (1). |

1. Use the x86 architecture memory layout (Addresses range from *0x100* to *0x10B*), memory contents (all values are in hexadecimal), and the symbol table shown below to provide suitable responses to the following questions.

**Memory Layout: Opcode Table:**

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| --- | --- | --- | --- | --- | --- |
| ***0x100*** | ***0x101*** | ***0x102*** | ***0x103*** | ***0x104*** | ***0x105*** |
| 3109  ***Address*** | 5108 | 110A | 3107 | 3106 |  |
|  |  |  |  |  |  |
| ***0x106*** | ***0x107*** | ***0x108*** | ***0x109*** | ***0x10A*** | ***0x10B*** |
| 0000 | 0002 | 0001 | 0001 | 0000 |  |

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| ***Opcode*** | ***Instruction*** |
| 0001 | Store AC to memory |
| 0011 | Load AC from memory |
| 0101 | Sub to AC from memory |

CPU registers

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| ***Register*** | ***Contents*** |
| PC | 100, |
| IR |  |
| AC | 0004 |

* 1. What is the final value in ac register after executing all instructions? [**2 points**]

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| AC: FFFE |

* 1. Mention all the values of the PC, IR, and AC (show me all the steps). [**3 points**]

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| PC: 100 -> 101 -> 102 -> 103 -> 104 -> 105 (stop)  IR: 3109 -> 5108 -> 110A -> 3107 -> 3106  AC: 0004 -> 0001 -> 0000 -> FFFE |
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