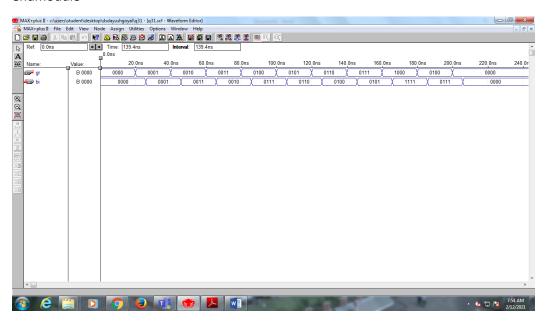
```
Ayush Goyal
190905522
                        DSD Lab 3 (Week 3)
Q1)
module q31(gr, bi);
        parameter n = 4;
       input [n-1:0]gr;
        output [n-1:0]bi;
        reg [n-1:0]bi;
        integer i;
        always@(gr)
        begin
        bi[n-1]=gr[n-1];
        for(i=n-2;i>=0;i=i-1)
        begin
        bi[i]=bi[i+1]^gr[i];
```

end

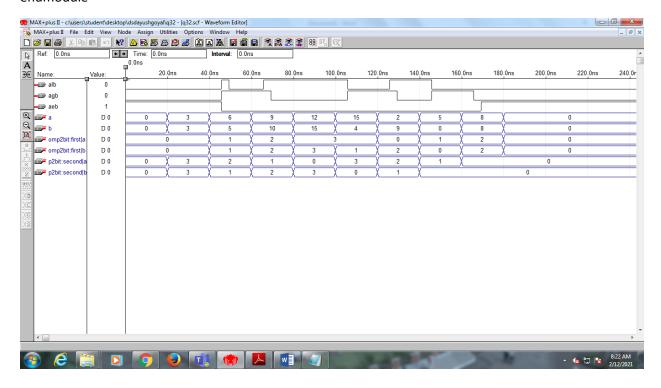
end



```
Q2)
module comp2bit(a,b, agb, aeb, alb);
input [1:0]a,b;
output agb, aeb, alb;
  wire w1,w2,w3,w4,w5,w6,w7,w8,w9,w10;
  not (w1,b[1]);
  and (w2,w1,a[1]);
  not (w3,b[0]);
  and (w4,a[0],w1,w3);
  and (w5,a[1],a[0],w3);
  or (agb,w2,w4,w5);
  not (w6,a[1]);
  not (w7,a[0]);
  and (w8,w6,b[1]);
  and (w9,w6,w7,b[0]);
  and (w10,w7,b[1],b[0]);
  or (alb,w8,w9,w10);
  xnor (aeb,alb,agb);
endmodule
module q32(a,b,agb,aeb,alb);
        input [3:0]a, b;
        output agb, aeb, alb;
       wire l1,e1,g1,l2,e2,g2,d1,d2;
        comp2bit first(a[3:2],b[3:2],g1,e1,l1);
        comp2bit second(a[1:0],b[1:0],g2,e2,l2);
        and (d1,e1,g2);
```

and (d2,e1,l2);

```
or (agb,g1,d1);
or (alb,l1,d2);
xnor(aeb, alb, agb);
```

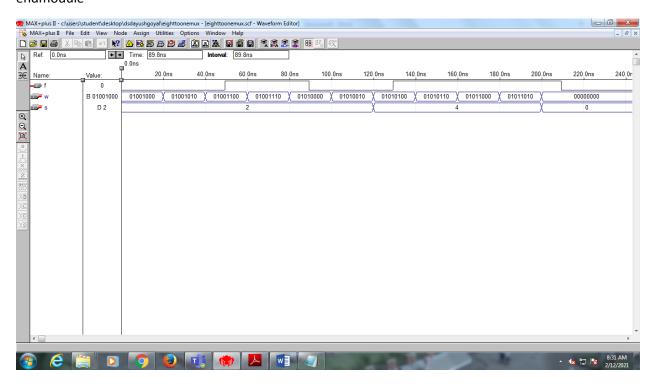


Q3) i)

```
module eighttoonemux(w,s,f);
input [7:0]w;
input [2:0]s;
output f;
reg f;
always @(w or s or f)
begin
case(s)
0:f=w[0];
1:f=w[1];
```

2:f=w[2];

```
3:f=w[3];
4:f=w[4];
5:f=w[5];
6:f=w[6];
7:f=w[7];
endcase
end
```



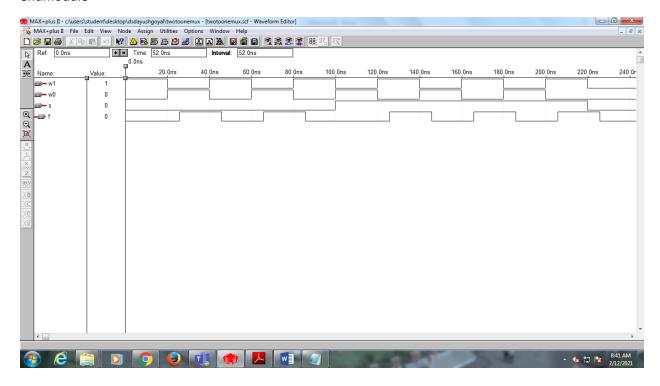
Q3) ii)

```
module twotoonemux(w0,w1,s,f);
input w0,w1,s;
```

```
output f;
reg f;
always @(w0 or w1 or s)
begin
if(s==0)
```

assign f = w0;

```
else
assign f = w1;
end
```



Q3) 16to1 MUX

endmodule

```
module sixteentoonemux(w,s,f);
    input [15:0]w;
    input [3:0]s;
    output f;
    reg f;
    reg s1,s2;
    eighttoonemux first(w[7:0],s[2:0],s1);
    eighttoonemux second(w[15:8],s[2:0],s2);
    twotoonemux last(s1,s2,s[3],f);
```

