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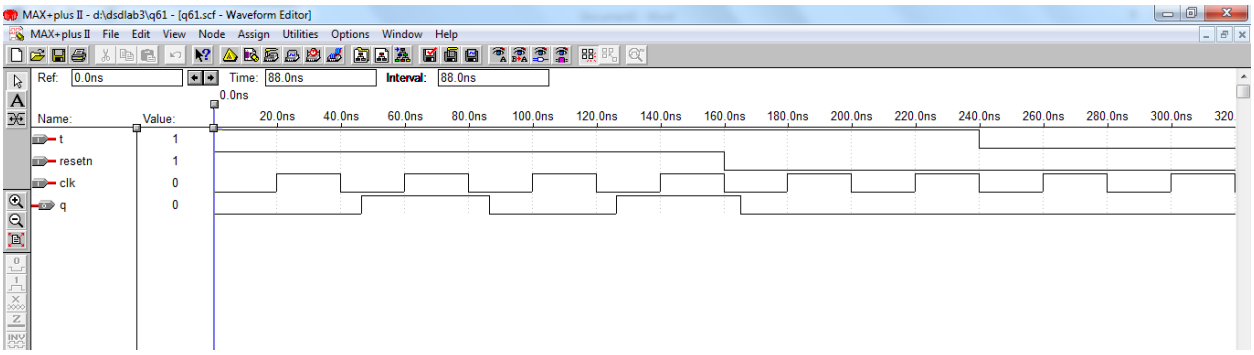
DSD Lab 6 (Session 3)

Q1) Write behavioral Verilog code for a negative edge triggered T FF with asynchronous active low reset.

Code:

```
module q61(t,clk,resetn,q);
        input t,clk,resetn;
        output q;
        reg q;
        always @(negedge clk or negedge resetn)
        if(!resetn)
        q<=0;
        else
        if(t)
        q<=~q;
        else
        q<=q;
endmodule
```

Output:

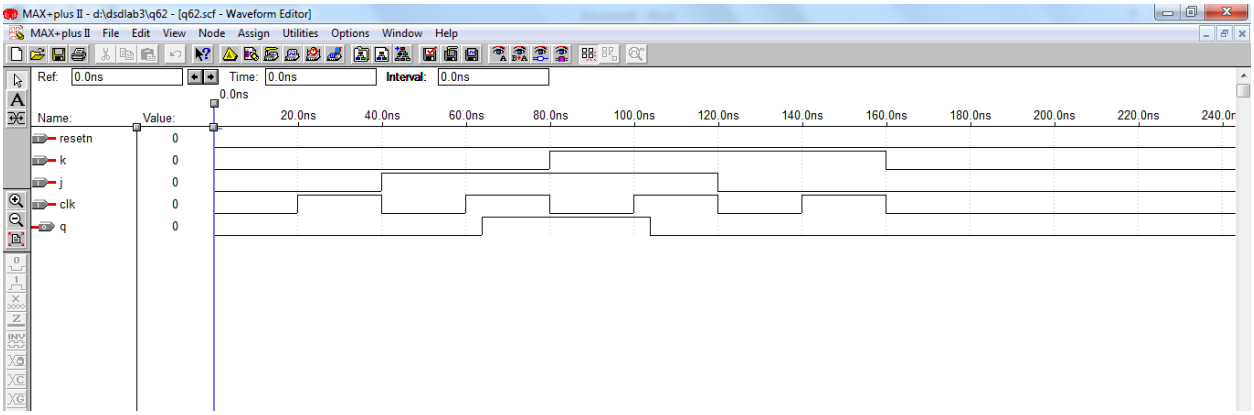


Q2) Write behavioral Verilog code for a positive edge-triggered JK FF with synchronous active high reset

Code:

```
module q62(j,k,clk,resetn,q);
        input j,k,clk,resetn;
        output q;
        reg q;
        always @(posedge clk)
        if(resetn)
        q<=0;
        else
        case({j,k})
        0:q<=q;
        1:q<=0;
        2:q<=1;
        3:q<=~q;
        endcase
endmodule
```

Output:



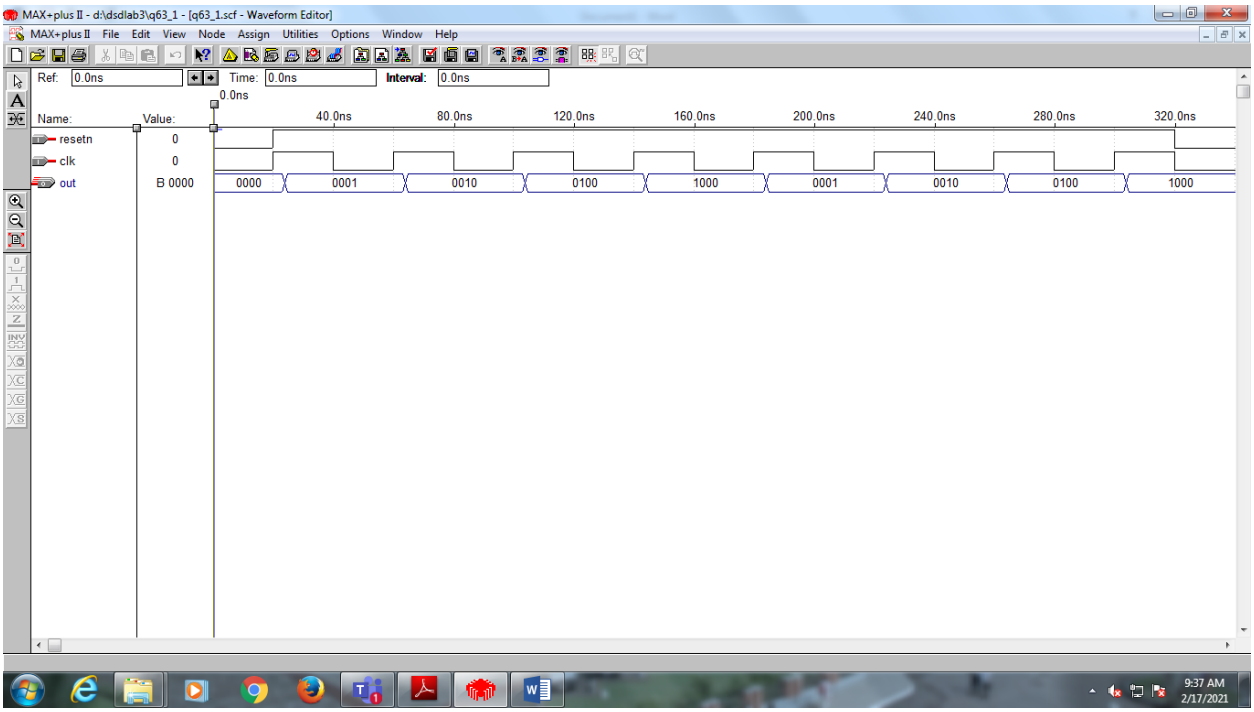
Q3) Design and simulate the following counters

a) 4-bit ring counter.

Code:

```
module q63_1(clk,resetn,out);
        input clk,resetn;
        parameter N=4;
        integer i;
        output [N-1:0]out;
        reg [N-1:0]out;
        always @(posedge clk)
        begin
        if(!resetn)
        out<=1;
        else
        begin
        out[0]<=out[N-1];
        for(i=N-1;i>0;i=i-1)
        begin
        out[i]<=out[i-1];
        end
        end
        end
endmodule
```

Output:



b) 5 bit Johnson counter.

Code:

```
module q63_2(clk,resetn,out);
        input clk,resetn;
        parameter N=5;
        integer i;
        output [N-1:0]out;
        reg [N-1:0]out;
        always @(posedge clk)
        begin
        if(!resetn)
        out<=0;
        else
        begin
        out[N-1]<=~out[0];
        for(i=0;i<N-1;i=i+1)
        begin
        out[i]<=out[i+1];
        end
        end
        end
endmodule
```

Output: