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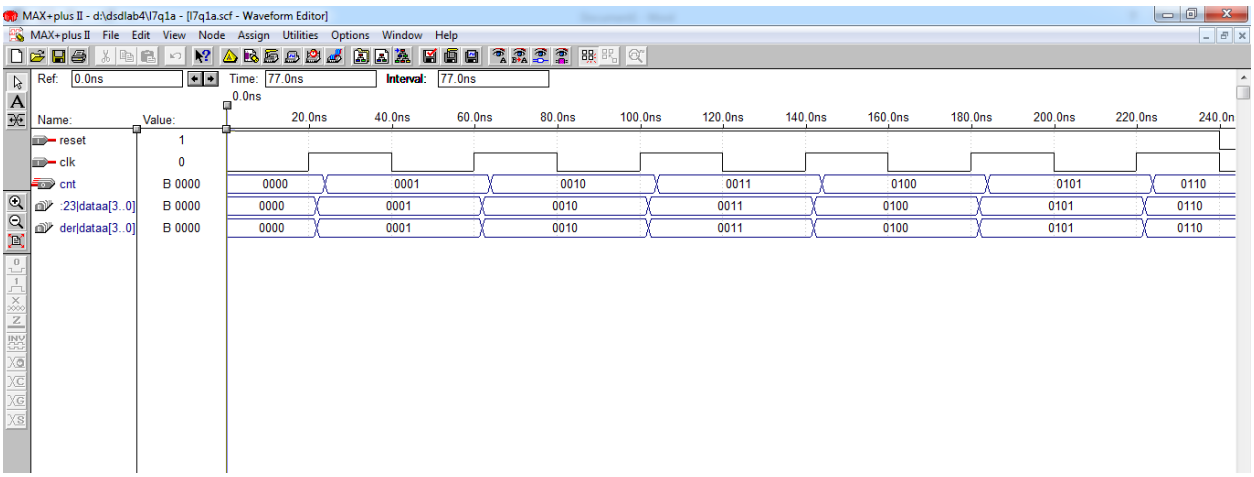
DSD Lab 7 (Session 4)

1. Design and simulate the following counters

a) 4 bit synchronous up counter

```
module l7q1a(clk, reset, cnt);
        input clk, reset;
        output [3:0]cnt;
        reg [3:0]cnt;
        always @(posedge clk) begin
        if(!reset)
        cnt<=0;
        else
        cnt<=cnt+1;
        end
endmodule
```



b) 3 bit synchronous up/down counter with a control input up/down’. If up/down’ = 1, then the circuit should behave as an up counter. If up/down’ = 0, then the circuit should behave as a down counter.

```
module l7q1b(clk, up, resetn, c);
        input clk, resetn, up;
        output [2:0]c;
        reg [2:0]c;
        always @(posedge clk)
        begin
        if(!resetn)
        c<=0;
        else
        begin
        if(up)
        c<=c+1;
        else
        c<=c-1;
        end
        end
endmodule
```