Mihir P Mehta

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Education	
Ph.D., Computer Science, University of Texas at Austin.	(2014 - present)
GPA: 3.3/4	(Spring 2018)
B.Tech., Computer Science and Engineering, Indian Institute of Technology (IIT) Delhi.	(2009 - 2013)
GPA: 7.9/10	
Exchange semester, Ecole des Mines, Saint-Etienne.	(2011)

Professional Experience

Research Intern at Oracle Corp., Belmont, CA, USA. (2018)
- Completed a code proof to certify the correctness of a highly optimised assembly language program.
- Contributed to a timing analysis of this program, to ensure the avoidance of race conditions.
- Studied the potential use of the TLAPS theorem prover for distributed systems, and created some preliminary internal documentation.

Research Intern at Apple Computer, Inc., Austin, TX, USA. (2017)
- Used model checking tools towards verifying Apple's hardware microarchitectures
- Developed proofs of correctness of hardware components with respect to specifications, with code changes where necessary.

Research Intern at Intel Corporation, Austin, TX, USA. (2015)
- Built a Pintool to dynamically analyse executables.
- Augmented the analysis with fine-grained information obtained from static analysis techniques.

Software Engineer at Samsung Research Institute, Noida, India. (2013-2014)
- Optimised the Linux kernel for Samsung's Android devices.
- Improved core components of the Linux virtual memory subsystem.

Research Experience

Filesystem modelling for FAT32 with Professor Warren A. Hunt Jr., CS department, UT Austin. (2016-present)
- Developed a model for the FAT32 file system with ACL2.
- Published a paper on this work in the proceedings of ACL2-2018.
- Currently developing specification for POSIX file operations, to be used for proving correctness of file-manipulating programs.

Program verification in object-oriented languages with Professors Isil Dillig and Thomas Dillig, CS department, UT Austin. (2014-2015)
- Developed a prototype verifier based on Hoare logic and weakest pre-conditions.
- Used the Soot compiler framework to generate verification conditions and the Z3 theorem prover to discharge them.
- Generated example inputs demonstrating bugs in several test programs.

Algorithms for bisimilarity with Professor S Arun Kumar, CSE Department, IIT Delhi (2012-2013)
- Conceptualised and implemented a toolkit for verifying bisimilarity and other properties of timed automata and labelled transition systems.
- Improved an algorithm for generating a zone graph from a timed automaton.

Coursework (selected graduate courses)	<u>UT Austin:</u> Automated Logical Reasoning, Introduction to Mathematical Logic, Formal Verification and Semantics, Automatic Verification of Software, Numerical Linear Algebra, Dependable Computing Sytems, Advanced OS, Recursion and Induction, Programming Languages (teaching assistant). <u>IIT Delhi :</u> Compiler Design, Theory of Computation, Numerical Optimisation.
Technical Skills	<u>Theorem provers:</u> ACL2, Coq, TLAPS. <u>Programming languages:</u> Functional languages (OCaml, SML), logic programming languages (Prolog), hardware description languages (VHDL, Verilog). <u>Operating systems:</u> GNU/Linux (kernel and application development). <u>Compiler frameworks:</u> Soot (Java), LLVM (C++). <u>Others:</u> Xilinx, Matlab, PostgreSQL.
Scholastic Achievements	- Awarded the UT Austin Graduate School's Recruitment Fellowship. (2014-2017) - All India Rank 138 (out of 400000), Joint Entrance Examination (IIT-JEE). (2009) - Secured All India Rank 29 in the All India Engineering Entrance Examination (AIEEE) among 1000000 candidates. (2009) - Scored 99 percentile in Verbal and Analytical Reasoning, GRE. (2012)
Others	<u>Languages:</u> English, French, Gujarati, Hindi.