# Mihir P Mehta

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**Education**

**Ph.D., Computer Science** (2014 - 2021)
University of Texas at Austin
GPA: 3.3/4

**B.Tech., Computer Science and Engineering** (2009 - 2013)
Indian Institute of Technology (IIT) Delhi
GPA: 7.9/10

**Exchange semester**, Ecole des Mines, Saint-Etienne (2011)

**Professional Experience**

**Formal Verification Engineer** at Intel Corporation, Santa Clara, CA, USA. (2021-)

- Applying diverse hardware verification tools - Forte, JasperGold, ACL2 - to solve a number of verification problems in the context of Intel's hardware chips.
- Incorporating verification into the hardware development cycle.
- Suggesting corrections to hardware designs to speed up the process of their verification.

**Research Intern** at Oracle Corp., Belmont, CA, USA. (2018)

- Completed a code proof to certify the correctness of a highly optimised assembly language program.
- Contributed to a timing analysis of this program, to ensure the avoidance of race conditions.
- Studied the potential use of the TLAPS theorem prover for distributed systems, and created some preliminary internal documentation.

**Research Intern** at Apple Computer, Inc., Austin, TX, USA. (2017)

- Used model checking tools towards verifying Apple's hardware microarchitectures
- Developed proofs of correctness of hardware components with respect to specifications, with code changes where necessary.

**Research Intern** at Intel Corporation, Austin, TX, USA. (2015)

- Built a Pintool to dynamically analyse executables.
- Augmented the analysis with fine-grained information obtained from static analysis techniques.

**Software Engineer** at Samsung Research Institute, Noida, India. (2013-2014)

- Optimised the Linux kernel for Samsung's Android devices.
- Improved core components of the Linux virtual memory subsystem.

**Research Experience**

**Filesystem modelling for FAT32** with Professor William R. Cook, CS department, UT Austin. (2016-present)

- Developed a binary-compatible executable model for the FAT32 file system.
- Used the model as a basis for separation-based reasoning about filesystems and filesystem clients with the ACL2 theorem prover.
- Used the separation logic framework as a basis for reasoning about concurrent filesystem clients under an oracle model of nondeterminism.

**Program verification in object-oriented languages** with Professors Isil Dillig and Thomas Dillig, CS department, UT Austin. (2014-2015)

- Developed a prototype verifier based on Hoare logic and weakest pre-conditions.

- Used the Soot compiler framework to generate verification conditions and the Z3 theorem prover to discharge them.
- Generated example inputs demonstrating bugs in several test programs.

**Algorithms for bisimilarity** with Professor S Arun Kumar, CSE Department, IIT Delhi (2012-2013)

- Conceptualised and implemented a toolkit for verifying bisimilarity and other properties of timed automata and labelled transition systems.
- Improved an algorithm for generating a zone graph from a timed automaton.

**Publications**

Mihir Parang Mehta. **Formalising Filesystems in the ACL2 Theorem Prover: an Application to FAT32**. In: *Proceedings of the 15th International Workshop on the ACL2 Theorem Prover and Its Applications, Austin, Texas, USA, November 5-6, 2018. Electronic Proceedings in Theoretical Computer Science.* Matt Kaufmann and Shilpi Goel, editors. Vol. 280, pp. 18-29, 2018. Full text: `https://cgi.cse.unsw.edu.au/~eptcs/paper.cgi?ACL22018.2`.

Mihir Parang Mehta, William R. Cook. **Binary-Compatible Verification of Filesystems with ACL2**. In: *10th International Conference on Interactive Theorem Proving (ITP 2019) (Leibniz International Proceedings in Informatics (LIPIcs))*, John Harrison, John O'Leary, and Andrew Tolmach (Eds.), Vol. 141. Schloss Dagstuhl-Leibniz-Zentrum fuer Informatik, Dagstuhl, Germany, 25:1-25:18. Full text: `https://doi.org/10.4230/LIPIcs.ITP.2019.25`.

Mihir Parang Mehta, William R. Cook. **Separation Logic-Based Verification atop a Binary-Compatible Filesystem Model**. In: *23rd Brazilian Symposium on Formal Methods (SBMF 2020)*. Preprint: `https://hal.archives-ouvertes.fr/hal-02956858`.

Aarti Gupta, Roope Kaivola, Mihir Parang Mehta, Vaibhav Singh. **Error Correction Code Algorithm and Implementation Verification using Symbolic Representations**. In: *Formal Methods in Computer-Aided Design 2022*. Preprint: `https://hal.archives-ouvertes.fr/hal-03769882`.

**Coursework (selected graduate courses)**

UT Austin: Automated Logical Reasoning, Introduction to Mathematical Logic, Formal Verification and Semantics, Automatic Verification of Software, Numerical Linear Algebra, Dependable Computing Sytems, Advanced Operating Systems, Recursion and Induction.
IIT Delhi: Compiler Design, Theory of Computation, Numerical Optimisation.

**Teaching assistantships (UT Austin)**

Graduate courses:
CS386L Programming Languages (Fall 2016, Spring 2020)
Convex Optimization (Fall 2019)
Undergraduate Courses:
CS439N Operating Systems (Fall 2015, Spring 2016, Fall 2020)
CS340D Debugging and Verifying Programs (Spring 2018)
CS392F Automated Software Design (Spring 2019)
CS371G Generic Programming (Summer 2020)

**Technical Skills**

Theorem provers: ACL2, Agda, Coq, TLAPS, Forte.
Other formal verification tools: JasperGold.
Programming languages: Functional languages (OCaml, SML),
logic programming languages (Prolog), hardware description languages (VHDL, Verilog).
Operating systems: GNU/Linux (kernel and application development).
Compiler frameworks: Soot (Java), LLVM (C++).
Others: Xilinx, Matlab, PostgreSQL.

**Scholastic Achievements**

- Awarded the UT Austin Graduate School's Recruitment Fellowship. (2014-2017)
- All India Rank 138 (out of 400000), Joint Entrance Examination (IIT-JEE). (2009)
- Secured All India Rank 29 in the All India Engineering Entrance Examination (AIEEE) among 1000000 candidates. (2009)
- Scored 99 percentile in Verbal and Analytical Reasoning, GRE. (2012)

**Others**

Languages: English, French, Gujarati, Hindi.