Mihir P Mehta

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Education

Ph.D. in Computer Science, University of Texas at Austin. (2014 - present)
GPA: 3.83/4 (Spring 2015)
B.Tech. in Computer Science and Engineering (CSE), Indian Institute of Technology (IIT) Delhi. (2009 - 2013)
GPA: 7.9/10
Exchange semester, Ecole des Mines, Saint-Etienne. (2011)

Professional Experience

Software Engineer at Samsung Research Institute, Noida, India. (2013-2014)

- Optimised the Linux kernel for Samsung's Android devices.
- Improved core components of the Linux virtual memory subsystem.

Software Engineering Intern at Intel Corporation, Austin, TX, USA. (2015)

- Built a Pintool to map dynamic memory accesses in executables to data structure elements in the corresponding C++ source code.
- Used several static analysis algorithms to get more fine-grained information for the purpose of dynamic analysis.

Research Experience

Program verification in compiled executables with Professors Isil Dillig and Thomas Dillig, CS department, UT Austin. (2014-2015)

- Developed a prototype verifier based on Hoare logic and weakest pre-conditions using the Soot compiler framework to generate verification conditions and the Z3 theorem prover to discharge them.
- Successfully found bugs in test programs and generated example inputs demonstrating the bug in each case.

Program verification in object-oriented languages with Professors Isil Dillig and Thomas Dillig, CS department, UT Austin. (2014-2015)

- Developed a prototype verifier based on Hoare logic and weakest pre-conditions using the Soot compiler framework to generate verification conditions and the Z3 theorem prover to discharge them.
- Successfully found bugs in test programs and generated example inputs demonstrating the bug in each case.

Algorithms for bisimilarity with Professor S Arun Kumar, CSE Department, IIT Delhi (2012-2013)

- Conceptualised and implemented a toolkit for verifying bisimilarity and other properties of timed automata and labelled transition systems.
- Leveraged UPPAAL model checker to add support for difference bound matrices.
- Improved an algorithm for generating a zone graph from a timed automaton.

Coursework

UT Austin: Automated Logical Reasoning, Introduction to Mathematical Logic, Formal Verification and Semantics, Automatic Verification of Software.
IIT Delhi (graduate courses only): Compiler Design, Theory of Computation.

Technical Skills

Programming languages: Functional languages (OCaml, SML),
logic programming languages (Prolog), hardware description languages (VHDL).
Operating systems: GNU/Linux (application development and kernel development).
Compiler frameworks: Soot (Java), LLVM (C++).
Others: Xilinx, Matlab, PostgreSQL.

Scholastic Achievements

- Awarded the UT Austin Graduate School's Recruitment Fellowship. (2014-2017)
- Secured All India Rank 138 in the Joint Entrance Examination (IIT-JEE) among 400000 candidates. (2009)
- Secured All India Rank 29 in the All India Engineering Entrance Examination (AIEEE) among 1000000 candidates. (2009)
- Scored 99 percentile in Verbal and Analytical Reasoning, GRE. (2012)

Others

Languages: English, French, Gujarati, Hindi.