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REVIEW ARTICLE

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Crystalline IGZO ceramics (crystalline oxide semiconductor)–based devices for artificial intelligence

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Abstract

In 2009, a crystalline oxide semiconductor with a layered structure, which we refer to as *c*-axis–aligned crystalline indium-gallium-zinc oxide (CAAC-IGZO), was first discovered. CAAC-IGZO has a peculiar crystal structure in which clear grain boundaries are not observed despite high *c*-axis alignment and absence of *a*-*b* plane alignment. When compared to a Si field-effect transistor (FET), a metal-oxide-semiconductor (MOS) FET, utilizing CAAC-IGZO, presents lower off-state current (on the order of yA [10^{-24} A]). These unique characteristics allow CAAC-IGZO to realize devices with low power consumption. With the emerging era of artificial intelligence, wherein power saving becomes more significant, CAAC-IGZO has attracted attention as a potential replacement for Si. This paper describes the characteristics and potentials of CAAC-IGZO for the development of memory devices with unprecedented functions.

KEYWORDS

gallium/gallium compounds, IGZO, indium/indium compounds, oxides, semiconductors, zinc oxide

1 | INTRODUCTION

Single-crystalline or polycrystalline indium-gallium-zinc oxide (IGZO) ceramics were first synthesized in 1985 by Dr. Noboru Kimizuka of the National Institute for Materials Science (formerly the National Institute for Research in Inorganic Materials).[1,2] In 2009, *c*-axis–aligned crystalline IGZO (CAAC-IGZO) was identified to show a layered structure. With the associated properties, CAAC-IGZO has a high potential to be used in various semiconductor devices. Due to the extremely low off-state current (I_{off}), metal-oxide-semiconductor field-effect transistors (MOSFETs), including a crystalline oxide semiconductor CAAC-IGZO (OSFET), can realize devices with significantly lower power consumption as compared to state-of-the-art Si-based devices. For instance, we have discovered that an OSFET with channel length (L)/channel width (W) of 0.8 μm/100 mm demonstrates an extremely low I_{off} of 6 yA/μm (10^{-24} A/μm), which had not been achieved previously.[3]

c-Axis–aligned crystalline indium-gallium-zinc oxide has been employed in various mass-produced display devices and is now anticipated to be a new material for display that would replace Si as a semiconductor material. In the large-scale integration (LSI) field, the emerging artificial intelligence (AI) era will require extremely low-power devices.

Compared with the human brain, current AI technologies cannot perform efficient processing and they consume significant power. For example, AlphaGo,[4] which has defeated a number of professional Go players, consumes 250 kW, whereas the human brain consumes only 20 W.[5,6] Enormous

power consumption is a serious limitation for AI data processing; thus, for practical application of AI, not only software but also hardware that enables more efficient processing needs to be developed.

In this paper, we describe several problems associated with the emerging AI era; the characteristics of a crystalline oxide semiconductor CAAC-IGZO; the features of an FET utilizing CAAC-IGZO; and the application of the crystalline oxide semiconductor to LSI.

2 | EMERGING AI ERA PROBLEMS

Various electronic devices employ Si LSI, and it is expected that the Si LSI market will exceed 400 billion dollars in coming years.

In AI, Si LSI is widely used for memory devices, arithmetic circuits, and peripheral circuits. However, AI powered by Si LSI faces several problems that must be addressed to assure an optimal prospect.[7–9] AI generates increasing amounts of data, that is, (a) the data explosion problem, (b) increasing latency in data transmission time, and (c) large power consumption of servers and terminals.

These are serious issues occurring with AI powered by Si LSI becoming widespread in our daily lives. In this study, we focus on the power consumption issue, which is of particular importance. It is noteworthy that South Korea, which dominates global semiconductor sales, has recently launched a large-scale project to reduce AI power consumption to 1/1000 of the current power consumption and develop a power-saving transistor.[10]

Such initiative reflects a global trend toward shifting existing semiconductors to next-generation materials to reduce energy consumption.

In this context, we propose an LSI that utilizes a crystalline oxide semiconductor (OSLSI) as a next-generation semiconductor to enable low-power AI. We propose a dynamic random access memory (DRAM) with greatly reduced refresh frequency (dynamic oxide semiconductor RAM, DOSRAM, Section 6.2) and a nonvolatile oxide semiconductor RAM with unlimited write cycles (NOSRAM, Section 7) as memory using OSLSI, which are expected to realize "universal memory" (Section 3). We believe that application of the proposed crystalline oxide memory to AI will reduce AI energy requirements, enabling a resilient AI technology in the future.

3 | UNIVERSAL MEMORY

As shown in Figure 1, various types of memory are employed in the hardware and software components of AI applications. Since such memory devices consume an enormous amount of power, universal memory that satisfies the following requirements is needed to ensure efficient processing:

Unlimited write cycles;
Nonvolatility (data retention after power off);
High-speed switching;
Extremely low power;

Figure 2 compares the characteristics of memory devices including OSLSI, existing memory devices including Si LSI, and nonvolatile memory devices including other materials.

Existing memory, such as DRAM and static RAM (SRAM), is capable of high-speed writes and demonstrates good write endurance; however, data retained in volatile memory are lost when the device's power is turned off. In contrast, NOR flash memory and NAND flash memory, which are primarily used in nonvolatile memory, have low write speed, high write voltage, and limited write cycles.

The proposed memory utilizing CAAC-IGZO exhibits the advantages of both volatile memory and nonvolatile memory.

As mentioned previously, CAAC-IGZO has an extremely low $I_{off.}$ This feature helps realize memory that utilizes OSFETs with long retention time and a logic circuit with OSFETs that performs normally off operation; that is, the power is interrupted in a standby state.[3,11]

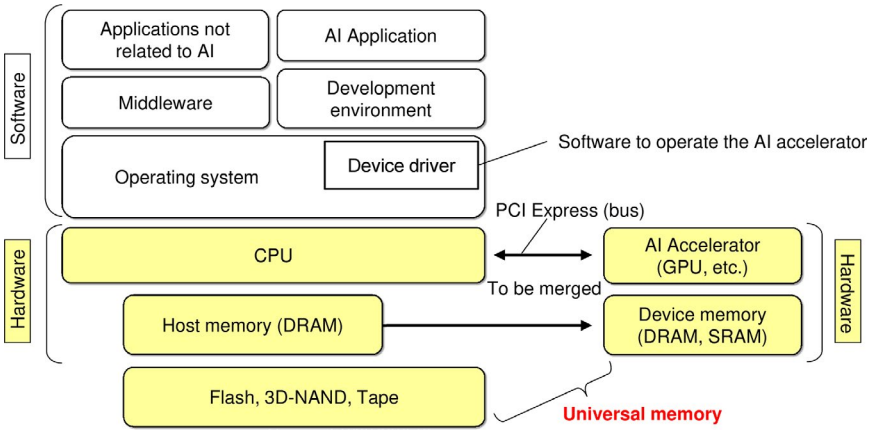


FIGURE 1 Hardware and software configuration for artificial intelligence (AI)

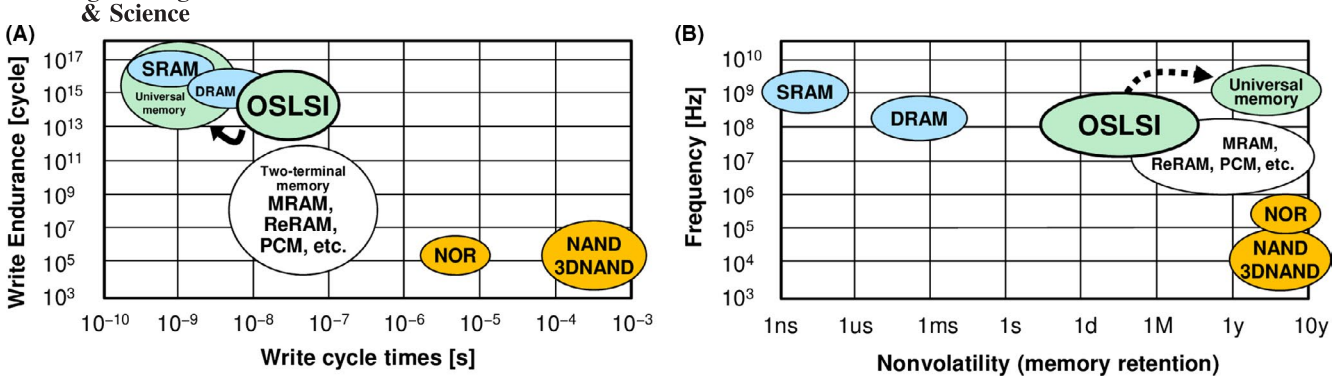


FIGURE 2 Comparison of write endurance, operating speed, and nonvolatility: (A) endurance vs. cycle time and (B) frequency vs. nonvolatility

Memory access occurs frequently in AI operations. However, nonvolatile memory including other materials, such as resistive RAM (ReRAM)[12] and magnetoresistive RAM (MRAM),[13] has poor write endurance. In principle, the proposed memory with OSFETs has excellent write endurance because data are rewritten by switching of transistors (as described in Section 7 below), implying CAAC-IGZO is a key technology to enable widespread practical applications of AI.

Such excellent characteristics of IGZO have already influenced LSI technology development efforts. For example, the Interuniversity Microelectronics Centre (IMEC), an international research institution, which is headquartered in Belgium and focuses on research, development, and innovation of VLSI, is working to move from using Si FETs in DRAM to using thin-film IGZO FETs.[14,15]

The details of technologies utilizing IGZO are described below.

4 | CAAC-IGZO

Here, the features of a crystalline oxide semiconductor CAAC-IGZO are described in terms of crystal morphology.

Figure 3 shows new classification of IGZO ceramics. IGZO ceramics are classified into three categories, amorphous, crystalline, and crystal. We have confirmed the existence of an amorphous structure[16,17] only in simulation.[18,19] CAAC-IGZO is a crystalline phase that has a structure in the boundary region between an amorphous structure and a crystal structure, including single crystal and polycrystal.[20–25]

Dr. Noboru Kimizuka, who first synthesized single-crystalline IGZO,[1,2,26] indicated that the crystal morphology of CAAC[21] and nanocrystal (nc)[22–24] should be classified as an intermediate state that is neither an amorphous structure nor a crystal structure. Similarly, Dr. Yoshio Waseda mentioned that CAAC and nc should be put in the category of a novel boundary region.[20]

Note that a single-crystalline FET is typically used in Si LSI. The single-crystalline Si FET has high mobility but requires high process temperatures, which limits available substrates.

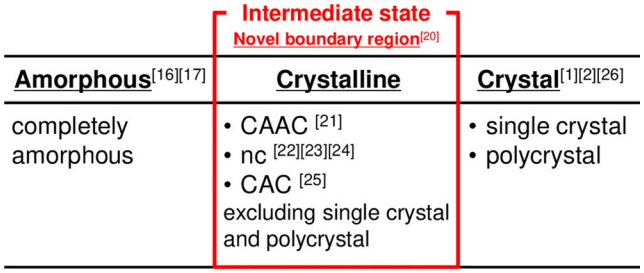


FIGURE 3 Classification of indium-gallium-zinc oxide ceramics

A polycrystalline Si FET, which can be formed with a thin film deposited over a glass substrate, is used in display and other devices. However, using a polycrystalline Si FET may reduce mobility due to grain boundary scattering and may result in characteristic variations between FETs depending on the positional relationship between an FET and the grain boundaries. The polycrystalline Si FET also has a film uniformity problem. Thus, it is difficult to use an FET with grain boundaries for LSI that requires high-speed operation and downscaling.

The crystal morphology of CAAC can address those process and grain boundary problems.

A CAAC-IGZO film does not have clear grain boundaries, and our study revealed little difference in mobility between a single-crystalline IGZO FET and an OSFET.[26] In addition, the CAAC-IGZO can be formed easily by sputtering at low costs; thus, it is highly suitable for mass production.

Figure 4 shows the crystal structure of $InGaZnO_4$. When seen from a direction perpendicular to the *c*-axis, the $InGaZnO_4$ crystal has a layered structure in which layers formed of In and O and layers formed of Ga, Zn, and O are stacked alternately.

Figure 5 shows transmission electron microscope (TEM) images of the crystal structure of CAAC-IGZO. In the cross-sectional image in Figure 5B, atoms are arranged along parallel planes as in the crystal structure of $InGaZnO_4$ in Figure 4. However, in the plan-view image (*a*-*b* plane) in Figure 5A,

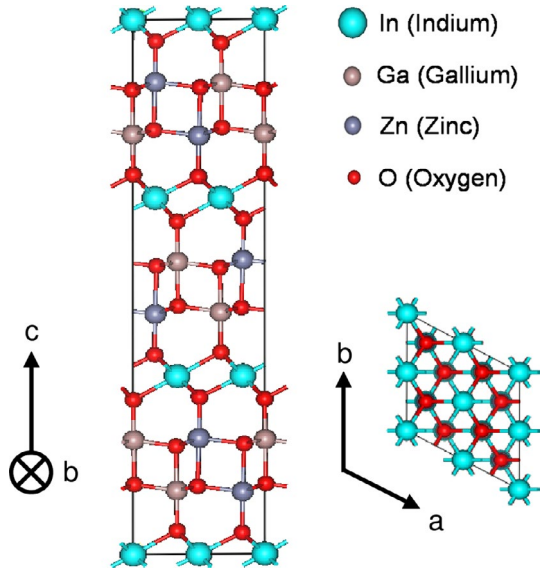


FIGURE 4 Crystal structure of $InGaZnO_4$

hexagons and other crystal structures are shown, and no clear alignment is observed.

Figure 6A,B shows the in-plane XRD spectra and the out-of-plane XRD spectra of CAAC-IGZO. According to the International Crystal Structure Database, the peak is derived from a (009) plane of an $InGaZnO_4$ crystal as shown in Figure 6B. Consequently, as shown in Figure 6A, there is no preferential orientation in the *a*-axis and *b*-axis directions, although the *c*-axis is aligned.

Figure 7 shows analysis results of the CAAC-IGZO using a Voronoi diagram, and the results indicate that the crystal grains are connected in a continuous manner.[28]

Formation of the Voronoi diagram (Figure 8) is explained. First, lattice points were extracted by analyzing the TEM image (Figure 8A), adjacent lattice points were connected with segments (Figure 8B), and a vertical bisector of each segment was drawn (Figure 8C) to obtain points where perpendicular bisectors intersect (ie, Voronoi points) (Figure 8D). Note that a polygonal region surrounded by the segments that connect the obtained Voronoi points is referred to as a Voronoi region or a Voronoi polygon.

Figure 7B reveals the fact that most Voronoi polygons are hexagons in the single-crystalline IGZO (Figure 7C), whereas some of the Voronoi polygons are pentagons and heptagons in the CAAC-IGZO. This indicates that crystal grains in the CAAC-IGZO are interconnected with an atomic arrangement that is distorted by pentagons and heptagons.

Thus, a boundary region regarded as a grain boundary of polysilicon is not seen clearly in the CAAC structure. In enlarged images of regions (1) and (2) in Figure 7D, grain boundaries are shown by broken lines, but are not clearly shown as in Figure 7A.

Figure 7E shows how the hexagons with connected lattice points in the regions (1) and (2) change in the plane, with the color mapping.

Formation of the color mapping is explained with reference to Figures 9A,B. An average value (average distance *a*) between a reference point in Figure 9A and closest six lattice points was calculated. Then, a regular hexagon with a side of the average distance *a* and with the reference point as a center was formed. The regular hexagon was rotated with the reference point as a center, and an angle ($0° \leq \theta < 60°$) was obtained such that an average of distances between vertices of the regular hexagon and the closest lattice points is minimum. This process was conducted to all of lattice points, and the angle of the mode was set to 30° and was expressed with a color shown in Figure 9B. As shown in Figure 7E, the change in colors corresponding to the angles is continuous. A drastic color change will point to the existence of grain boundaries, but

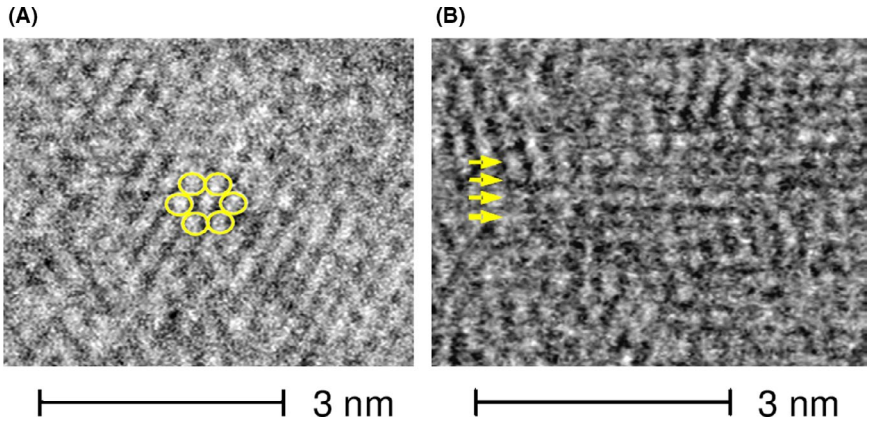


FIGURE 5 Transmission electron microscope images of *c*-axis–aligned crystalline indium-gallium-zinc oxide (CAAC-IGZO): (A) CAAC-IGZO plan-view image and (B) CAAC-IGZO cross-sectional image.[27] Reprinted from *SID Sym. Dig. Tech. Pap.*, **Vol. 46**, S. Yamazaki, J. Koyama, Y. Yamamoto and K. Okamoto, "Research, Development, and Application of Crystalline Oxide Semiconductor," pages 183-186, Copyright (2012), with permission from Wiley

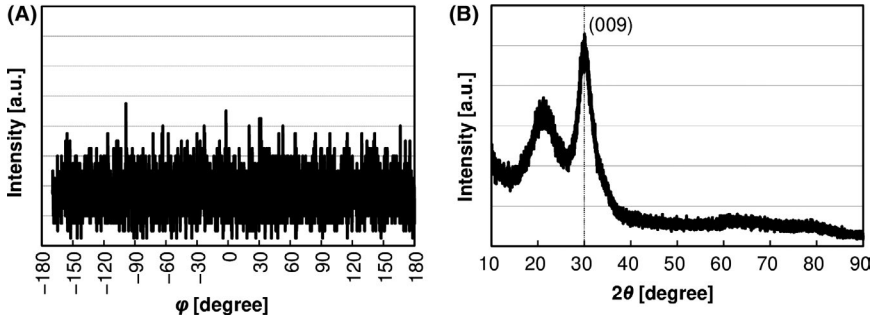


FIGURE 6 XRD measurement results for *c*-axis–aligned crystalline indium-gallium-zinc oxide: (A) in-plane (φ-scan) XRD spectra ($2\theta = 56°$) and (B) out-of-plane XRD spectra. Reprinted from Yamazaki et al,[21] Copyright (2014), with permission from Wiley

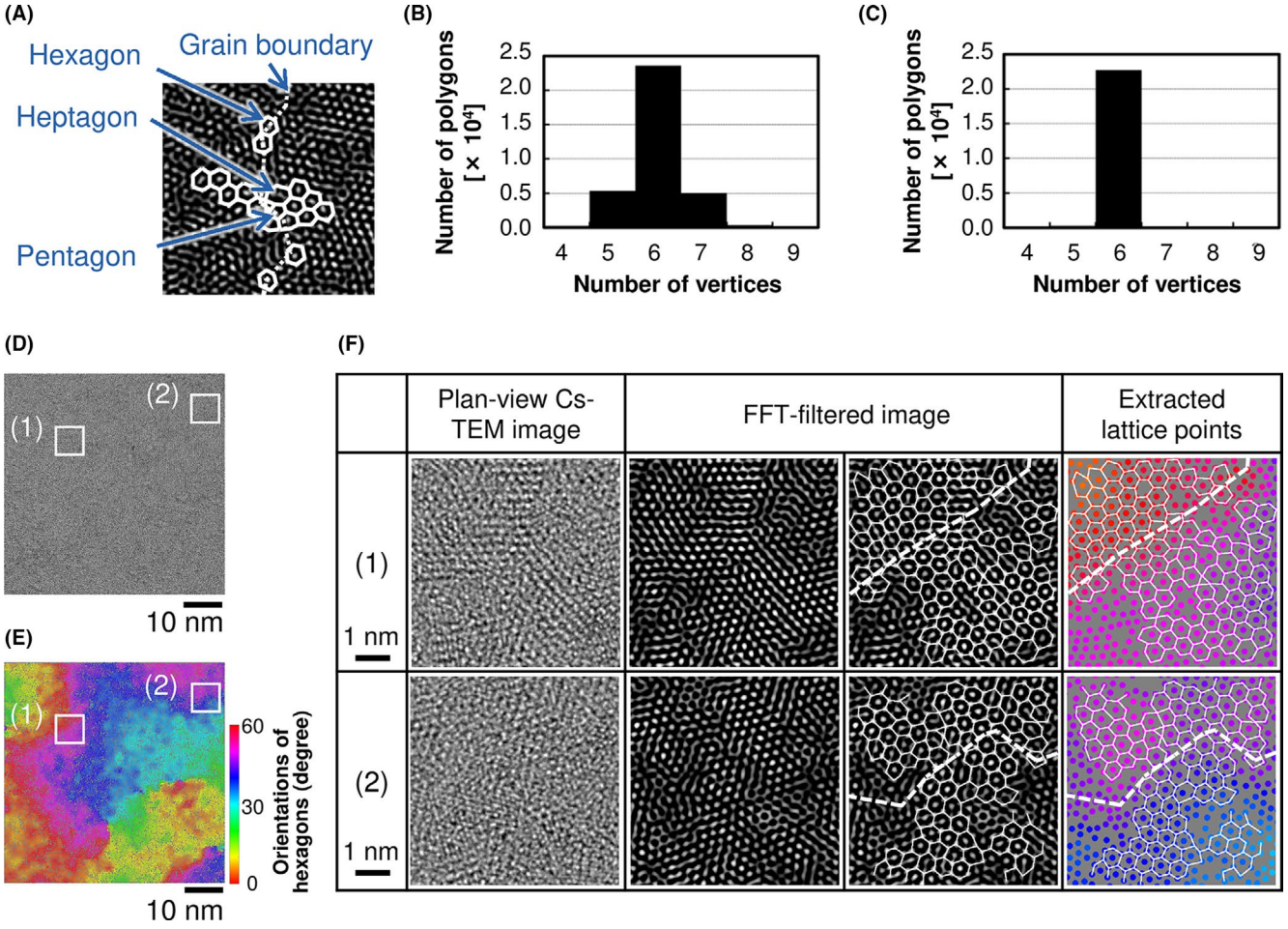


FIGURE 7 Voronoi diagram and color mapping of *c*-axis–aligned crystalline indium-gallium-zinc oxide (CAAC-IGZO): (A) FFT-filtered image of CAAC-IGZO film; (B) number of Voronoi polygons of CAAC-IGZO; (C) number of Voronoi polygons of single-crystalline IGZO; (D) high-resolution plan-view transmission electron microscope image; (E) distribution of hexagonal lattice orientation (averaged radius: 1 nm); and (F), enlarged images of regions (1) and (2) in (D) and (E)

this is not observed. Thus, unlike in a polycrystalline IGZO, clear grain boundaries are not observed in the CAAC-IGZO film. This distinctive crystal connection is considered to be attributed to the crystal structure of IGZO. The c-axis slightly deviates from a direction perpendicular to the film surface. In addition, the IGZO crystals have characteristics that oxygen atoms are positioned between In, Ga, and Zn atoms and the layered crystal structure of IGZO is stable over a wide range of compositions. The bonding strength and the equilibration distance between a metal atom and an oxygen atom vary among In, Ga, and Zn. Therefore, it is assumed that the crystal structure of the CAAC-OS is tolerant to distortion and adjacent crystals are connected with some distortion. Presumably, an adverse effect of crystal grain boundaries is not observed owing to such a feature.

The CAAC-IGZO is a crystalline oxide ceramic material that demonstrates interesting properties related to this peculiar grain boundary feature. It can be used to realize FETs

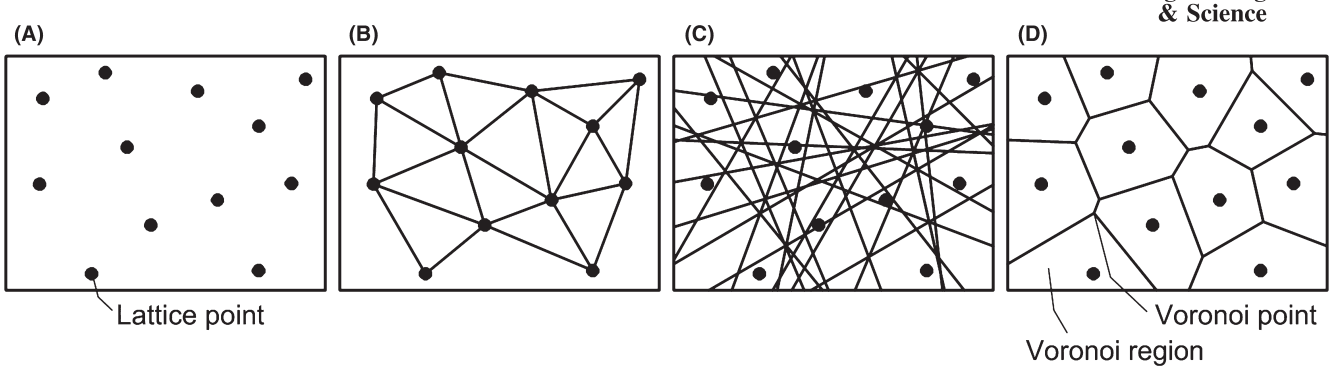
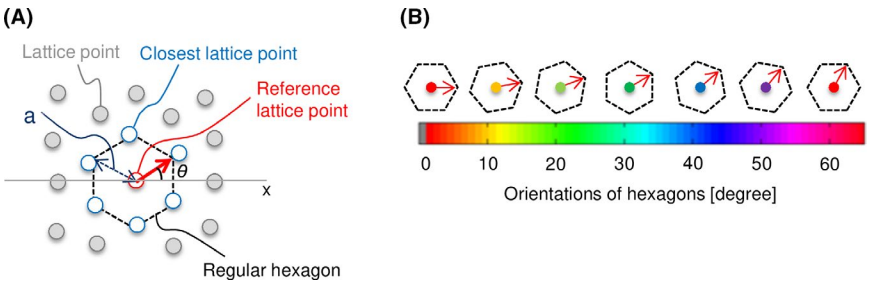


FIGURE 8 Illustration of forming Voronoi diagrams: (A) extract lattice points from FFT-filtered image, (B) connect adjacent lattice points, (C) draw a vertical bisector of each segment, and (D) obtain points where perpendicular bisectors intersect

FIGURE 9 A, Illustration of forming color mapping, B, examples of colors corresponding to angles



that are unaffected by grain boundary scattering and have no leakage via recombination centers due to defects. As a result, we estimated that the extremely low I_{off} on the order of yA/μm (10^{-24} A/μm) was obtained, which is the most remarkable feature of an OSFET.

5 | FEATURES OF CAAC-IGZO FET

5.1 | OSFET fabrication conditions

An FET using CAAC-IGZO, hereinafter referred to as OSFET, has been fabricated. Figure 10 is a perspective view of the fabricated OSFET. This OSFET is suitable for scaling down as a gate electrode can be formed in a self-aligned manner between a source electrode and a drain electrode.

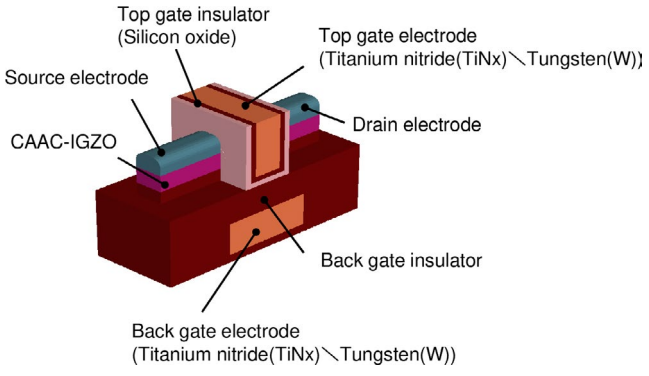


FIGURE 10 Perspective view of the OSFET

c-Axis–aligned crystalline indium-gallium-zinc oxide was deposited on a Si oxide insulating film over a single-crystal Si substrate using DC magnetron sputtering equipment. CAAC-IGZO with an In:Ga:Zn atomic ratio of 4:2:3 was formed by using a target with an In:Ga:Zn atomic ratio of 4:2:4.1 for deposition. CAAC-IGZO was deposited at a power of 0.5 kW, at a pressure of 0.7 Pa, with oxygen gas, at a substrate temperature of 200°C, and in a high-purity oxygen gas atmosphere.

The OSFET in Figure 10 has a Fin-type device structure in which a CAAC-IGZO channel is three-dimensionally surrounded by a top gate electrode through a top gate insulator. The source electrode and the drain electrode are formed over the CAAC-IGZO such that the top gate electrode is positioned between them. A back gate electrode is provided under the CAAC-IGZO, and voltage applied to the back gate electrode adjusts the threshold voltage (V_{sh}). The OSFET is fabricated at temperatures up to 400°C with the condition that the copper wiring and other components provided over or under the OSFET are not damaged.

5.2 | I_{off} characteristics

The I_{off} of an OSFET is approximately 15 digits less than that of a Si FET.

This I_{off} is therefore too low to observe, as the I_{off} of a single-device FET is below the lower measurement limit of

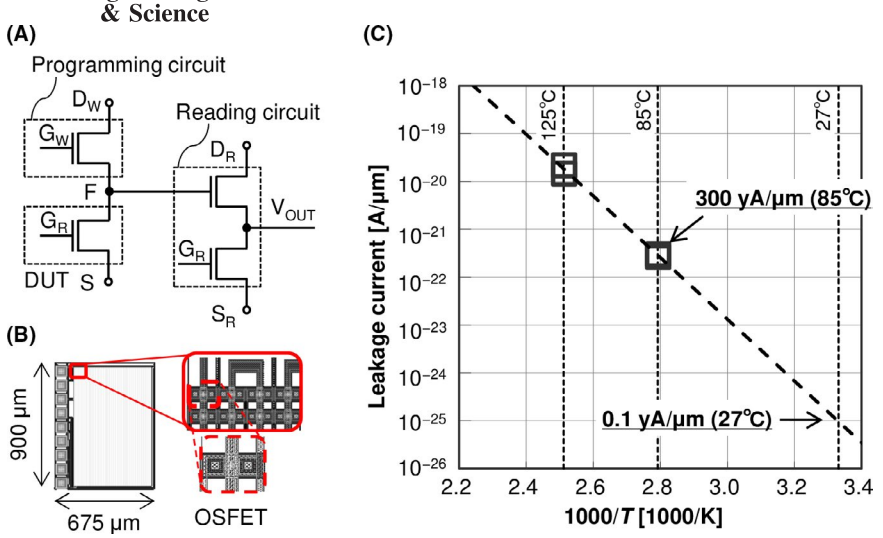


FIGURE 11 Measurement method of I_{off} and temperature dependence of leakage current in off-state of OSFET: (A) measurement concept,[29] (B) layout of test element group (DUT: L/W = 60 nm/60 nm × 20 000 FETs; W_{total} = 1.2 mm), and (C) I_{off} characteristics[34]

most accurate measurement apparatuses. Therefore, the I_{off} was measured as follows.[29]

As shown in Figure 11A, if there is minute leakage current while a device under test (DUT) is off, the voltage (V_F) of the floating node (FN) and the output voltage (V_{out}) decrease over time. The I_{off} can be estimated on the basis of the reduction in V_{out} (ΔV).

Figure 11B shows a layout of a test element group where 20 000 OSFETs with L/W of 60/60 nm are connected in parallel to make a large transistor with W of 1.2 mm. The change in V_{out} can thus be monitored, so that the V_F of the FN can be observed. As shown in the graph in Figure 11C, leakage current of 300 yA per W of 1 μm was measured at 85°C.

5.3 | Mobility comparison with Si FET

A typical guiding principle for improvement of LSI performance is downscaling of FETs.

Figure 12A shows L dependence of drift mobility of Si FET and OSFET with the same drain voltage. The drift mobility of OSFET was obtained in reference to theoretical studies.[30] Figure 12A also shows measurement results of field-effect mobility of the OSFET. The measurement results meet the theoretical studies. Figure 12B shows the mobility ratio of Si FET to OSFET.

The mobility of an OSFET is less affected by L as compared to that of a Si FET, suggesting that the mobility of an OSFET would be close to 1/5 of that of a Si FET with scaling down to L of 20 nm.

5.4 | Initial characteristics

The variations (V_{sh} and on-state current [I_{on}]) of 26 OSFETs on one substrate by the Smirnov-Grubbs test (significance level of 5%) were evaluated. Figures 13 and 14 are normal probability plots of V_{sh} and I_{on} of the OSFETs with L/W = 60/60 nm. The fabricated OSFETs were evaluated after being subjected to a thermal budget stress of N_2 treatment at 400°C for 8 hours. Here, V_{sh} is a gate voltage (V_g) at 1 pA when a drain voltage (V_{ds}) is 1.2 V. I_{on} is a drain current at V_{ds} = 1.2 V when

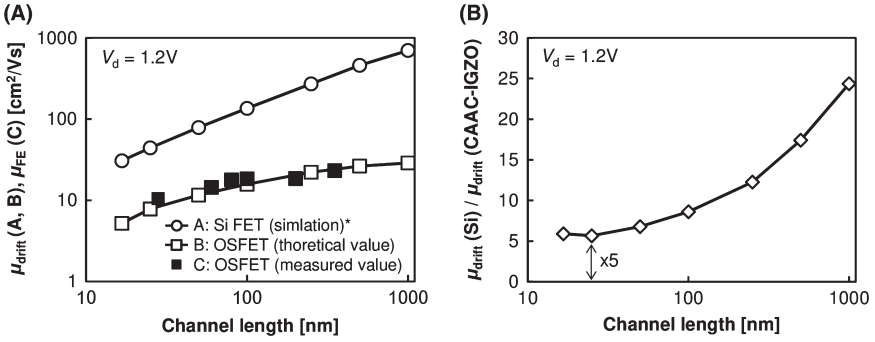


FIGURE 12 Mobility comparison between OSFET and Si FET: (A) L dependence and (B) mobility ratio of Si FET to OSFET, where ($\mu_{drift}(A, B)$) is the drift mobility derived from a calculation of electron velocity ($v = \mu E$), and $\mu_{FE}(C)$ is calculated from actual measurement data, $\mu_{FE} = \max\left[\frac{2L}{WC_{ox}}\left(\frac{\partial\sqrt{I_d}}{\partial V_g}\right)^2\right]$ *Monte Carlo simulation based on Silvaco, Inc. TCAD mcdevice ex02[34]

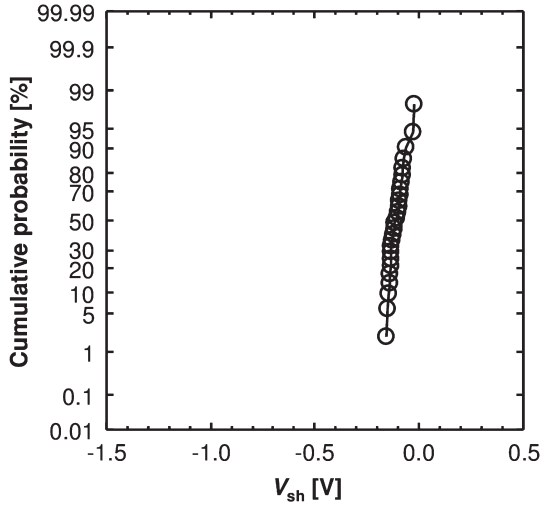


FIGURE 13 Normal probability plot of V_{sh} of OSFET with L/W = 60 nm/60 nm (sample size = 26, average = −0.11 V, σ = 35 mV, V_d = 1.2 V [obtained by the Smirnov-Grubbs test; significance level of 5%])

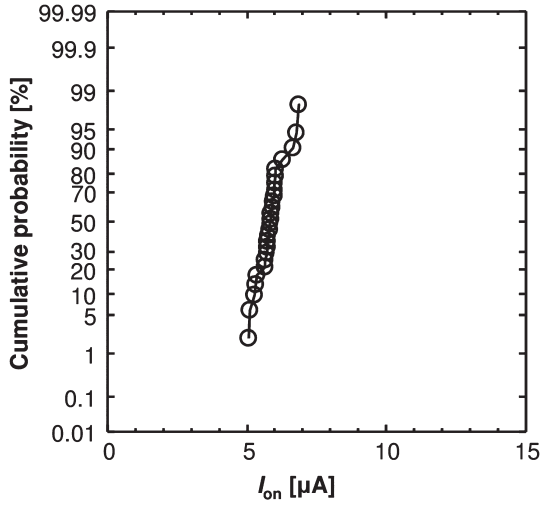


FIGURE 14 Normal probability plot of I_{on} of OSFET with L/W = 60 nm/60 nm (sample size = 26, average = 5.85 μA, σ/average = 7.7% [obtained by the Smirnov-Grubbs test; significance level of 5%])

$V_{gs} = V_{sh} + 2.5$ V. The variations of V_{sh} and I_{on} were σ = 35 mV and 7.7%, respectively. The variation of V_{sh} has achieved 35 mV, which approaches the variation values of CMOS, indicating commercial suitability.

5.5 | Reliability evaluation

The reliability of the OSFET was evaluated next. The reliability test used four elements (samples) on one substrate, and a positive gate bias temperature stress test (PGBT test) was conducted with a stress voltage condition of 10% raise of an operation voltage (nominal value). In the PGBT test, a positive bias stress was applied to the OSFET's gate electrode to check temporal variations in characteristics of the OSFET. The test was conducted at a temperature of 150°C with a stress (3.63 V) applied to the gate electrode. Figure 15 shows the PGBT test results. From the results obtained with four samples, the lifetime of the OSFET was calculated to be 1200 hours or longer, when the lifetime is defined as the period of time that the shift amount of V_{sh} (ΔV_{sh}) is within 100 mV. Variations of other parameters (*S.S.* [mV/dec], I_{on} [A], and μ_{FE} [cm^2/Vs]) were sufficiently small. The initial characteristics and reliability performance that were obtained in the tests indicate that we have reached a point where we can evaluate the OSFET's commercial viability.

5.6 | Cutoff frequency f_T

Next, the high-speed current characteristics of an OSFET were measured. The driving force (g_m) per gate load (C_g) can be estimated with cutoff frequency (f_T). Here, f_T refers to the frequency at which the current gain becomes 1, and the f_T of a bulk Si FET with a gate length of 30 nm is approximately 300 GHz.[31] Figure 16 shows the f_T measurement results for an OSFET with L/W of 25/21 nm.[32] As shown in Figure 16, the f_T value ranges from 24 to 29 GHz. This OSFET has a back gate electrode, and a change in voltage applied to the back gate electrode (V_{bg}) can adjust the V_{sh}. In general, not only V_{sh} but also C_g or mobility may vary with V_{bg}; however, the f_T of the OSFET will only change slightly with V_{bg} and 30 GHz is obtained.[32]

6 | OSFET MEMORY CHARACTERISTICS

6.1 | DOSRAM: a memory enabling high operating frequency

A memory called dynamic oxide semiconductor random access memory (DOSRAM)[33] has been fabricated. This memory's peripheral circuits are formed with Si FETs, and an OSFET is used as 1T of its 1T1C (one transistor and one capacitor) memory cell. Figure 17 shows the prototyped DOSRAM's (A) cross-sectional view of its stacked layer structure, (B) 8-kB chip micrograph,[33] and (C) memory cell circuit diagram. OSFETs can be formed on top of insulators, insulating films, or Si LSIs.

In DOSRAM, the number of cells per bit line is reduced by stacking OSFET on top of Si FET, which in turn makes the load on each bit line smaller and reduces the capacitance. Having OSFET, which enables low I_{off}, in its memory cells, DOSRAM can store data for a longer time with a smaller capacitance than DRAM with Si memory cells.

The prototype is a CPU-embedded 8-kB DOSRAM.[33] The DOSRAM has an operating frequency of 30 MHz that is applied to CPU, and its data retention time is more

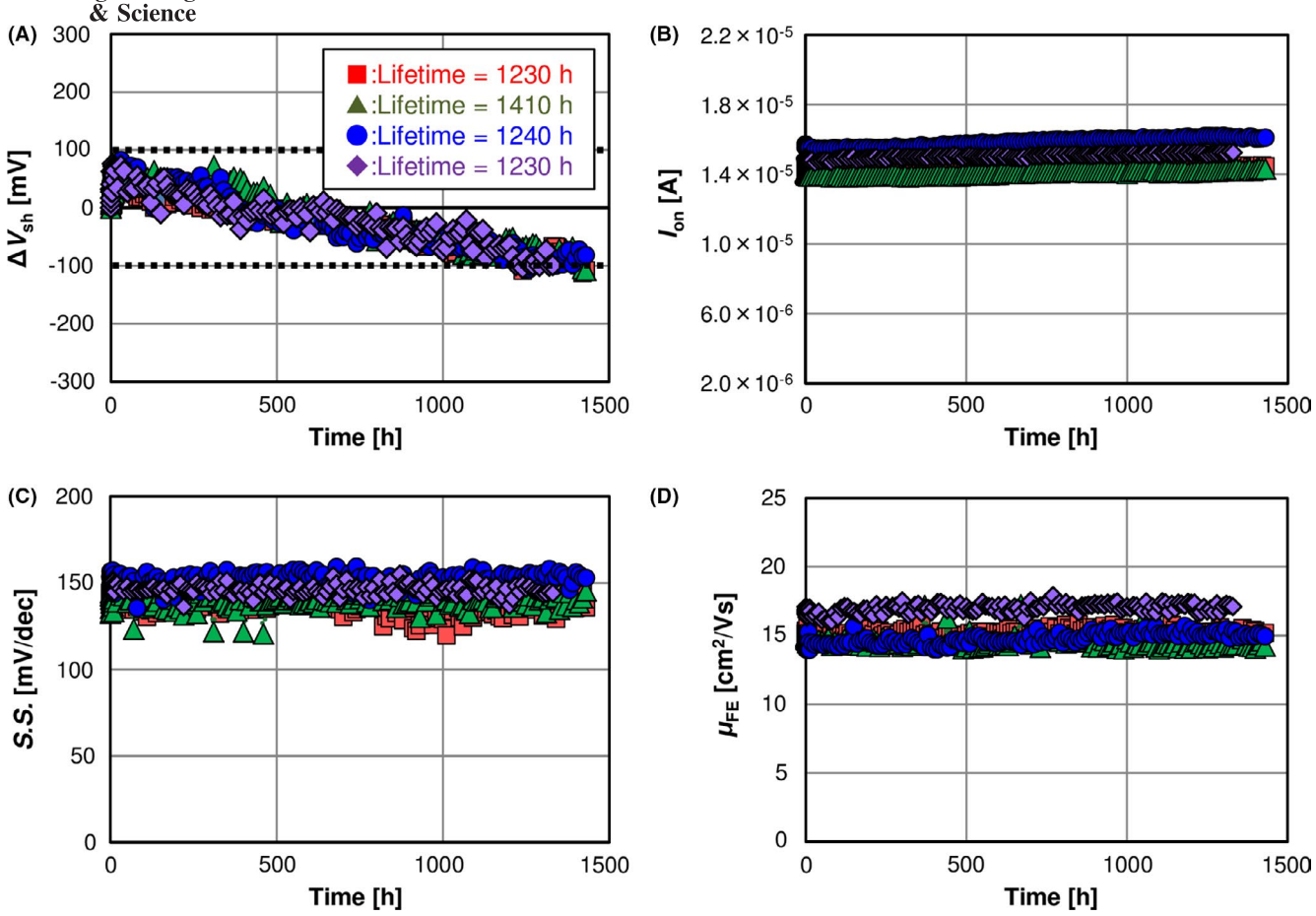


FIGURE 15 Positive gate bias temperature stress test results (stress condition: V_g = 3.63 V, 150°C) showing temporal variations of (A) ΔV_{sh}, (B) I_{on} (V_d = 1.2 V, V_g = 3.3 V), (C) *S.S.* (V_d = 1.2 V), and (D) μ_{FE}

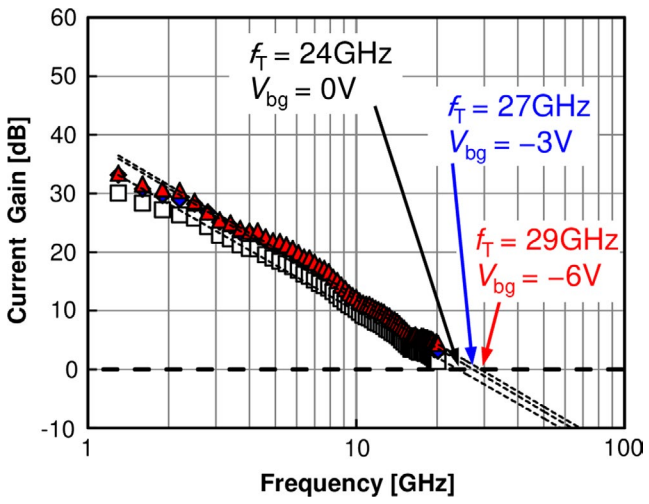


FIGURE 16 Cutoff frequency f_T of OSFET with *L*/*W* of 25 nm/21 nm[32]

than 1 hour. The CPU's operating frequency at 30 MHz is a bottleneck to the memory's performance, and a stand-alone DOSRAM is estimated to have a higher operating frequency.

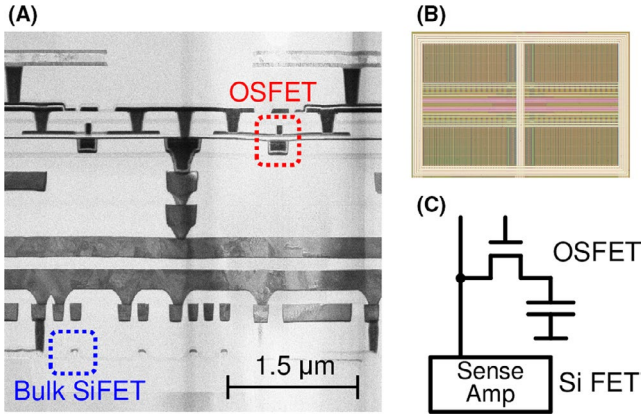


FIGURE 17 DOSRAM module with stacked Si and OSFETs: (A) cross section, (B) chip micrograph,[33] and (C) circuit diagram of memory cell

The DOSRAM module's operating frequency and retention time were estimated based on its design and characteristics of a single OSFET.

The block diagram of a 1-MB DOSRAM module used for estimation is shown in Figure 18. In the 1-MB DOSRAM module, a memory with the same configuration as the 8-kB

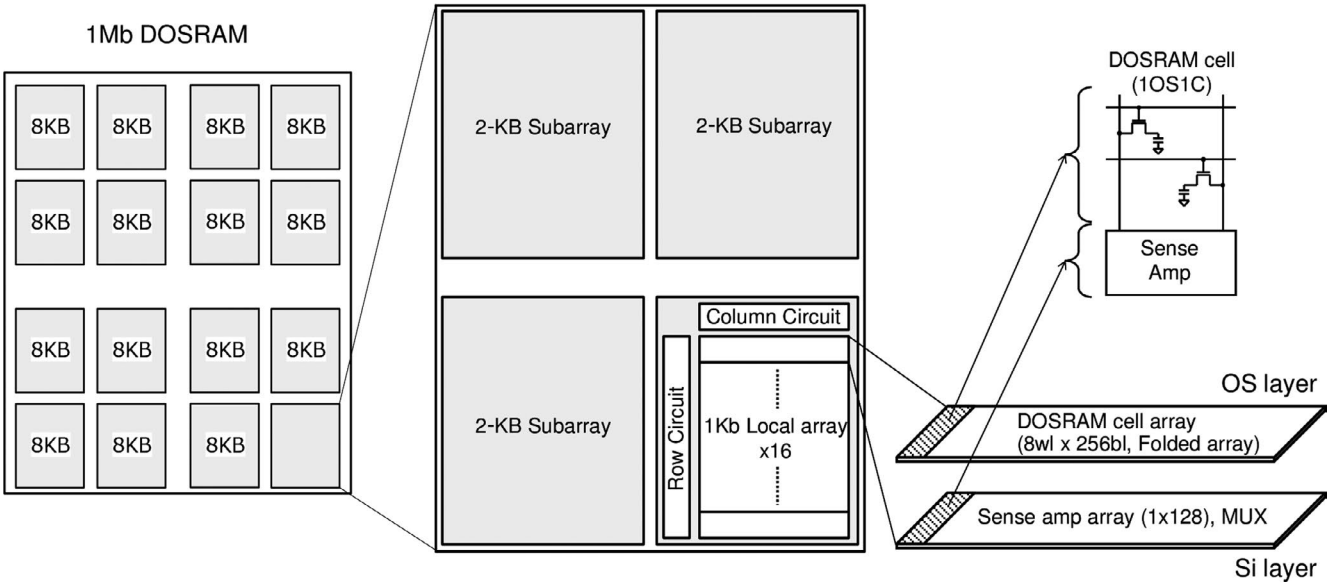
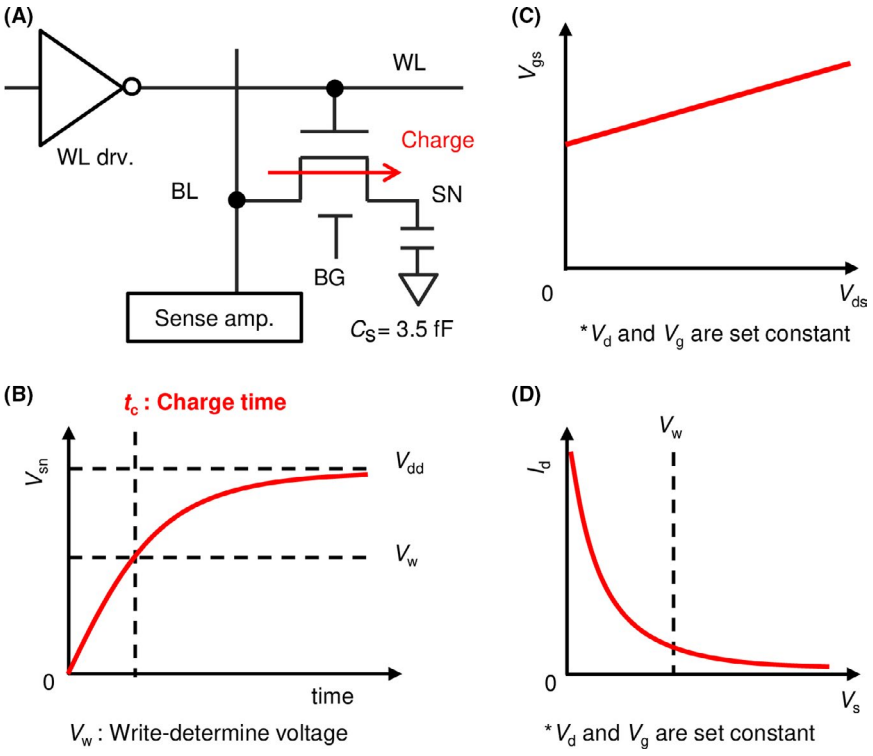


FIGURE 18 1-MB DOSRAM module (cell size: 0.56 μm^2; storage capacitor: 3D-MIM 3.5 fF; memory density: 1MB; configuration: 8 wl × 128 bl × 16 blocks × 4 subarrays × 16; data bus: 32b; array type: open array; supply voltage: VDD = 1.2 V; OS gate = −0.8 V/2.5 V; BL loading: 90 ohm; 8 fF)

FIGURE 19 Method of estimating operating frequency of 1-MB DOSRAM: (A) circuit diagram of DOSRAM memory cell, (B) relationship between retention potential and time during write operation of memory cell shown in (A), (C) the V_{gs} and V_{ds} trajectory during "High" potential writing of a memory cell, and (D) relationship between I_d and V_s when the source potential of a single OSFET is swept



DOSRAM prototype (made up of four 2-kB subarrays) constitutes 1 block, and 16 of these blocks are arranged to form a 1-MB DOSRAM. The load on the bit line is 90 Ω and 8 fF, and the storage capacitor is 3.5 fF.

The operating frequency and data retention time of the 1-MB DOSRAM shown in Figure 18 are estimated based on characteristics obtained from a single OSFET.

Figure 19 illustrates how operating frequency is estimated from a single OSFET's characteristics. Figure 19A shows the circuit diagram of the memory cell and peripheral circuits of DOSRAM. Figure 19B depicts the potential of the storage node (SN) when a word line is selected to write "High" potential so that the node potential changes from "Low" to "High" (hereinafter referred to as "High"

potential writing). Normal write operations are carried out when the potential of SN (V_{SN}) reaches the write-determine voltage (V_W). Charge time (t_c) is defined as the amount of charge time required for normal write operations.

Figure 19C shows the trajectory of the OSFET's drain-source and gate-source voltage during "High" potential writing. In the memory write operations, the "High" potential writing is the worst condition of write time.

By conducting an I_d-V_s measurement of a single FET based on the trajectory of the driving voltage shown in Figure 19C, the memory cell's current during write operations can be measured accurately. In fact, the trajectory of the driving voltage is obtained from I_d-V_s measurements (in which V_d and V_g are set constant). This current characteristic is shown in Figure 19D.

The operating frequency is estimated with the following steps:

I_d-V_s is measured based on the trajectory of the driving voltage when writing to the memory cell.

The charge curve of SN shown in Figure 19B is calculated using I_d-V_s measurement results and the Equation that is based on Coulomb's law.

$$t_c = C_s \int_0^{V_w} \frac{dV_s}{I_d(V_s)} \quad (1)$$

With Equation , t_c needed for "High" potential writing can be estimated.

3. The cycle time-to-t_c ratio is obtained from the layout-based simulation of the 1-MB DOSRAM module, and the operating frequency is then estimated from t_c.

Figure 20A illustrates the method of estimating the retention time of the 1-MB DOSRAM module. The written and stored "High" potential decreases over time due to cell leakage current. In DOSRAM, the OSFET's drain leakage current is expected to be dominant as the cell transistor does not have a body terminal and leakage current from the capacitor is minimal. The OSFET's drain current exhibits exponential behavior with respect to a wide voltage range in the subthreshold region. As shown in Figure 20B, the retention time is estimated based on the I_d-V_{gs} measurement results. The I_{off} of the OSFET is extremely low, and as described in Section 5.4, its actual value cannot be measured without a special method. Therefore, the drain current (I_{cut}) obtained from the V_s and the

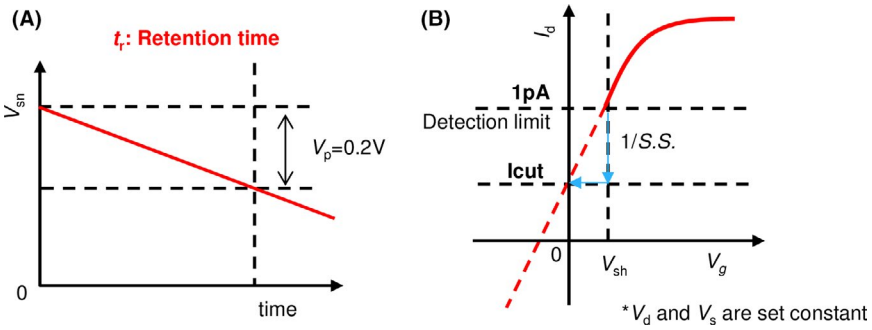


FIGURE 20 Method of estimating retention time of 1-MB DOSRAM: (A) relationship between retention potential and time of memory cell in assumed 1-MB DOSRAM after writing "High," and (B) I_d-V_{gs} measurement of a single OSFET

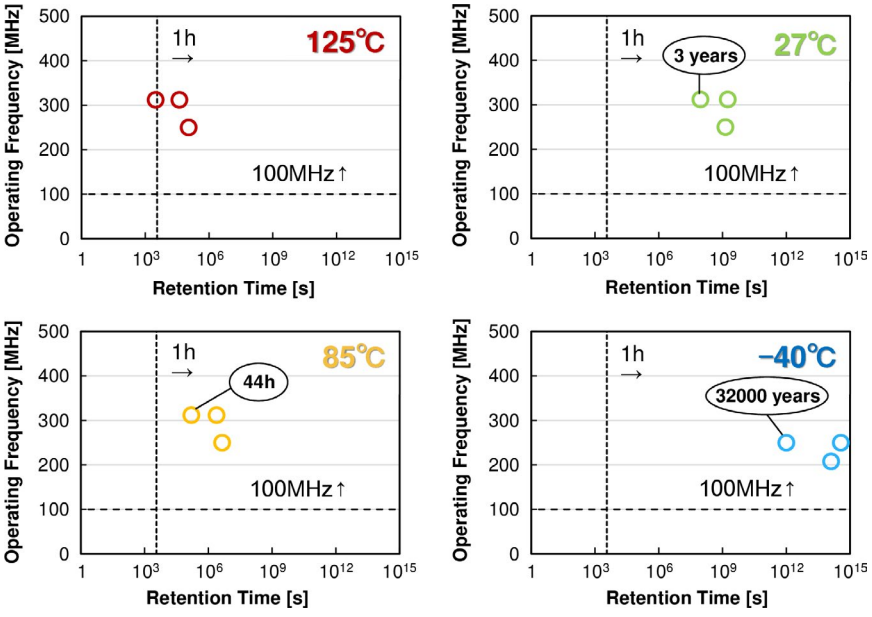


FIGURE 21 Estimation results of operating frequency and retention time of DOSRAM, which are evaluated according to the estimation methods in Figures 19 and 20 (sample: three devices, L/W = 60 nm/60 nm, V_g(off)/V_g(on) = −0.8 V/2.5 V, V_{bg} = −5.7 V)[34]

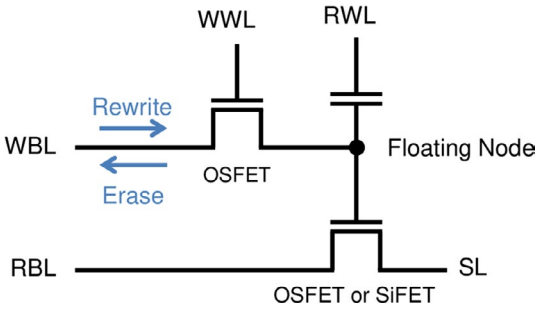


FIGURE 22 NOSRAM circuit diagram

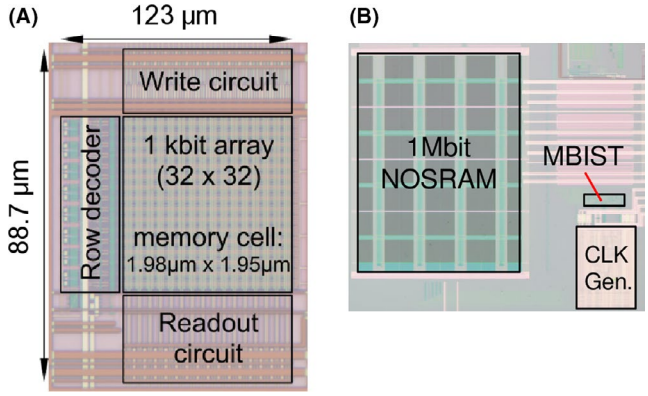


FIGURE 23 Prototype NOSRAM: (A) single-layer 1-kb NOSRAM[35] © 2018 IEEE. Reprinted, with permission, from S. Maeda et al, *ISSCC Dig. Tech. Pap*., (2018) 486 and (B) stacked layer 1 Mb NOSRAM[36] © 2017 IEEE. Reprinted, with permission, from T. Ishizu et al, *IEEE Symp. VLSI Circuits Dig. Tech. Pap*., (2017) C163

S.S. needs to be estimated as the cell leakage current when the word line is not selected. The DOSRAM module's expected retention time (t_r) can be estimated using Equation , which includes this cell leakage current (I_{cut}), the design value of allowable retention voltage variation (V_p), and the design value of capacitance (C_s).

$$t_r = C_s \frac{V_p}{I_{cut}} \tag{2}$$

Figure 21 shows the estimation results of operating frequency and retention time using the evaluation methods depicted in Figures 19 and 20. The estimation results reveal that the prototyped OSFET requires refreshing (the energy supply required to record the same value) less than once per hour in a wide range of temperature between −40°C and 125°C. In contrast, a DRAM that uses Si FET for its memory cell requires refreshing once every dozens of milliseconds. As power consumption is directly correlated to refresh frequency, DOSRAM that has low refresh frequency is more effective for usage in larger computers. In this case, to replace DRAM with DOSRAM for practical use, an operating frequency of more than 100 MHz is required for DOSRAM. The horizontal dotted line in Figure 21 shows that the prototyped OSFETs (sample: 3 devices) have achieved adequate memory characteristics of both an operating frequency of more than 100 MHz and a refresh frequency of less than once per hour.

6.2 | NOSRAM

NOSRAM is a memory with OSFETs that has unlimited write cycles in principle, which is suitable for universal memory.

Figure 22 shows a circuit diagram of a NOSRAM cell composed of two transistors and one capacitor. The NOSRAM cell can be configured with a stack of an OSFET and a Si FET (ie, a hybrid structure). The NOSRAM cell can also comprise only OSFETs. A NOSRAM module can be configured with a stack of OSFETs and Si FETs. A NOSRAM module can also be configured with a single layer of OSFETs, in which case peripheral circuits comprise only OSFETs.[35] Figure 23A shows a memory module with a single layer of OSFETs,[35] and Figure 23B shows a memory module with a stacked layer of OS and Si FETs (the hybrid structure).[36]

The write endurance of Si flash memory is generally around 10^4. Figure 24 shows the device structure of Si floating gate nonvolatile memory with a control gate, which is a basic patent[37] for current flash memory. S. Yamazaki, one of the present authors, invented this structure in 1970. After that, flash memory was mass-produced from TOSHIBA CORPORATION and is in common use even nowadays all over the world.

In the Si floating gate nonvolatile memory with a control gate, electric charge is injected into and released from the floating gate through a gate insulating film (Figure 24); thus, damage

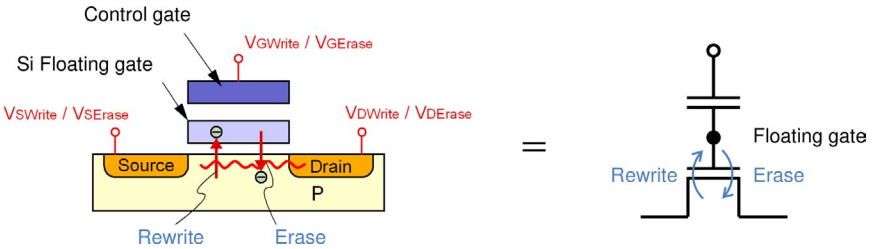


FIGURE 24 Device structure of Si floating gate nonvolatile memory

caused by the injection of the electric charge degrades the gate insulating film, which limits the number of write cycles.

NOSRAM with the circuit shown in Figure 22 does not require injection of electric charge through a gate insulating film. Here, charging and discharging of storage capacitor, which correspond to write, are performed by turning on/off the OSFET; therefore, such degradation does not occur in principle. In addition, since the I_{off} of the OSFET is on the order of yA/μm, electric charge stored on the floating node (FN) can be held in nonvolatility.

Figure 25 shows changes in voltages of the floating node at writing and erasing in the NOSRAM write cycles. The room temperature (R.T.) data show the characteristics of a device with OSFETs,[34] and the 85°C data show the characteristics of a device with a hybrid structure (OS and Si FETs). NOSRAM operates normally even after 10^{14} rewrites at R.T. and at 85°C.

In general, universal memory requires high-speed writes, erases, and reads and long retention time as shown in Figure 2. NOSRAM is expected to achieve high-speed operation at a frequency of 100 MHz and data retention of greater than 10 years at 85°C by a V_{th} control technology. The operating frequency and retention time of NOSRAM were estimated by controlling V_{th} with V_{bg} so that I_{cut} has a value low enough to achieve the retention time of 10 years at 85°C (Figure 26). The graph for 125°C (Figure 26) demonstrates that data retention of approximately over 1 year is possible. A low V_{bg} value can increase the data retention period, and assuming I_{off} to be ideal, data retention of 2.3×10^9 years (2.3 billion years) would be possible at −40°C according to the calculation. This period is half of the 4.6 billion years since the earth was formed. That is, there is a possibility that data would be retained for hundreds of thousand years, enabling an unprecedented knowledge storage platform.

7 | CONCLUSIONS

Here, we report on the discovery of CAAC-IGZO, which is a novel crystalline oxide ceramic suitable for memory technologies.

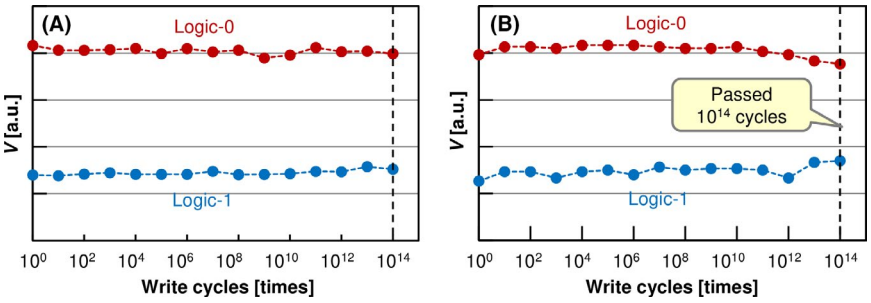


FIGURE 25 NOSRAM write characteristics: (A) R.T.[34] and (B) 85°C[34]

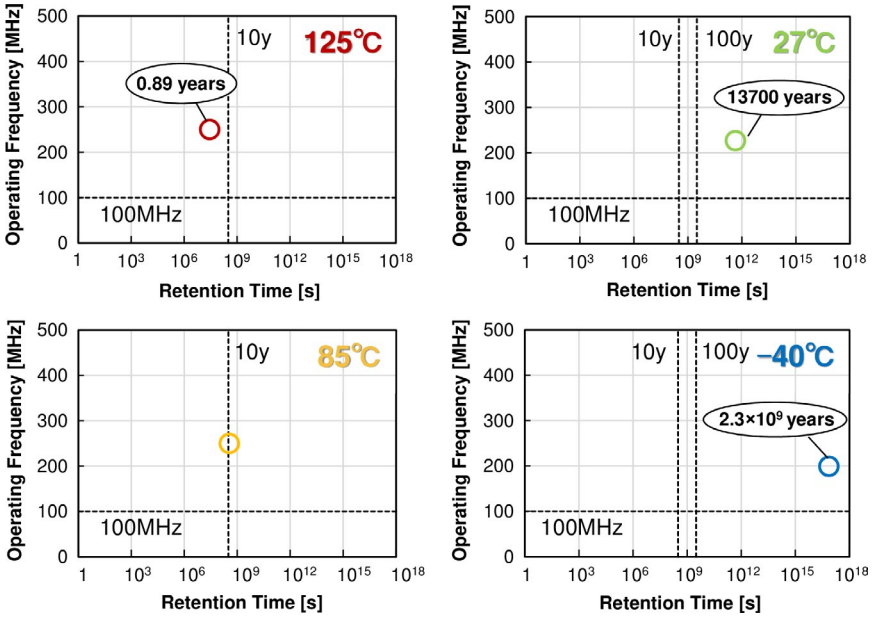


FIGURE 26 Estimation results of operating frequency and retention time of NOSRAM, which were evaluated according to the estimation method in Figures 19 and 20 (sample: one device; $L/W = 60$ nm/60 nm; $V_{g(}$off)/V_g(on) = −1.47 V/1.83 V; $V_{bg} = -3.0$ V)[34]

c-Axis–aligned crystalline indium-gallium-zinc oxide has a structure in a novel boundary region, which differs from single-crystalline, polycrystalline, and amorphous structures. The crystalline structure has not been known and demonstrates interesting properties. Clear grain boundaries are not observed in CAAC-IGZO despite high *c*-axis alignment and absence of *a*-*b* plane alignment. The crystal grains in the CAAC-IGZO were suggested to be interconnected with a distorted atomic arrangement by the analysis of the Voronoi diagram.

We propose the CAAC-IGZO as a next-generation material for LSI to replace the current mainstream Si. The CAAC-IGZO is expected to offer solutions to the significant power consumption issue for the emerging AI era.

An OSFET can be formed by sputtering and is thus suitable for mass production. The most remarkable feature of an OSFET is the extremely low I_{off} (on the order of yA/μm [10^{-24} A/μm]). The mobility of an OSFET is suggested to be close to 1/5 of that of a Si FET with scaling. Due to the unique characteristics of an OSFET, DOSRAM and NOSRAM, which are memory devices with low power consumption, have been realized. DOSRAM is a DRAM with greatly reduced refresh frequency. NOSRAM is a memory with OSFETs that can operate normally even after 10^{14} rewrites, which can be configured with an OSFET/Si FET hybrid structure. NOSRAM can also comprise only OSFETs.

The memories with OSFETs are able to operate at high frequency of 100MHz or more in a wide temperature range.

In principle, DOSRAM and NOSRAM with OSFETs have unlimited write cycles, which is expected to facilitate the realization of extremely low-power memory that does not need to be refreshed. Both memories are optimal for applications to products that require low power usage (eg, AI products).

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