DLD LAB MANUAL 3

Objectives:

- Max terms and Min terms
- To learn and study how to create and test combinational logic circuit using Logic Works

THEORY:

Logic Works 4 is a program used for designing and simulating circuits.

Start Logic Works by selecting it from the Microsoft Windows Start menu as shown in Fig. 1. Once the application is started several windows will appear on your screen:

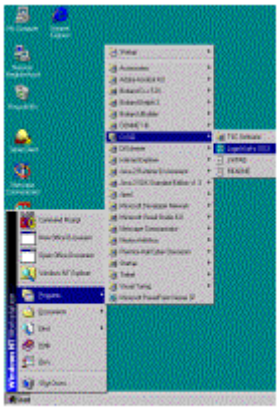


Fig. 1

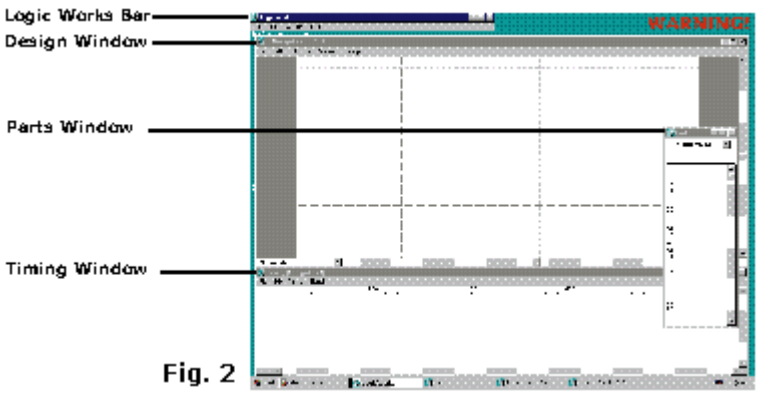


Fig. 2

We will refer to these windows by the labels associated with them in Fig. 2. *The Design Window* is the main window where circuits are drawn. Once the circuit is drawn, it is simulated and the output appears in the *Timing Window*. The *Logic Works Bar* is used to open existing designs and start useful tools. The *Parts Window* is used to select devices to place on the circuit design. Circuit designs are often referred to as schematics.

Let's Build a Circuit

In this tutorial, you will build and test a circuit that implements the following Boolean equation:

$$Z = AB + BC + AC'$$

This requires the following components:

1. Three AND gates with two inputs (AND-2)
2. Two OR gates with two inputs (OR-2)
3. A single NOT gate commonly called an inverter

4. Some wires to connect the gates
5. Three switches to provide a way to modify the input values for testing.

AND Gates:

- Find the AND-2 gate in the *Parts Window* and double click on it.
- Move the mouse pointer to the *Design Window* and place three of these gates where you want them by clicking once for each gate. See Fig. 4. ***Note:*** Spreading the gates apart a little makes it easier to connect parts to them later.
- Hit *Esc/Space* so that no more AND gates are selected.

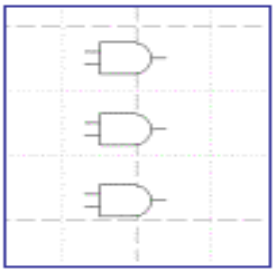


Fig. 4

OR Gates:

- Find the OR-2 gate in the *Parts Window* and double click on it.
- Move the mouse pointer to the *Design Window* and place two of these gates to the right of the AND gates. See Fig. 5
- Hit *Esc/Space* again so no more OR gates are selected.

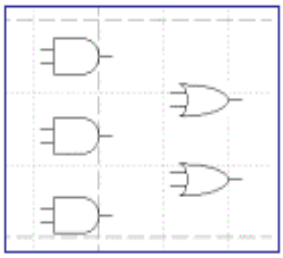


Fig. 5

NOT Gates (Inverters):

- Find the NOT gate in the *Parts Window* and double click on it.
- Move the mouse pointer to the *Design Window* and place one NOT gate to the left of the bottom AND gate.
- Remember to hit *Esc/Space* to deselect the NOT gate.

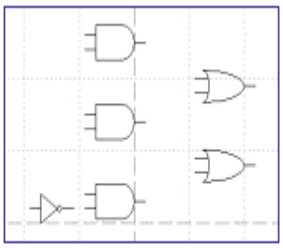


Fig. 6

Moving and deleting existing gates:

By single clicking on an item on the schematic (The *Design Window*) the device will be selected and highlighted. While the device is selected, the *Delete* key will remove the item from the schematic. To move a device, point at it and hold down the left mouse button, then move the mouse to the desired location. Release the mouse button.

Connecting the Devices:

Adding wires:

- Place the cursor on the right edge of the switch and hold down the left mouse button.
- Drag the mouse a half-inch or so to the right and release the button. A red wire should now be attached to the switch, ending in the middle of nowhere. See Fig. 8.
- Repeat this for each of the three switches.

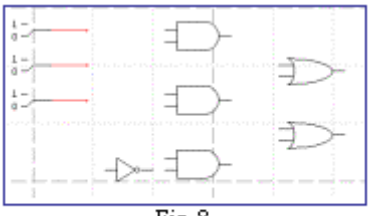


Fig. 8

Recall that we are trying to implement Z = AB + BC + AC'. To clarify your design and show its relation to the equation above, we will label the wires A, B, and C.

Labeling wires:

- Right-click on the wire you want to name.
- Select *Name* from the box that appears, as in Fig. 9.
- Type the name of the wire in the text box. Be sure to check Visible as in Fig. 10.

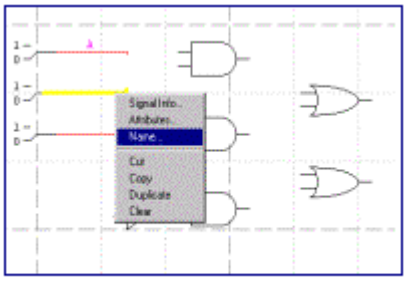


Fig. 9

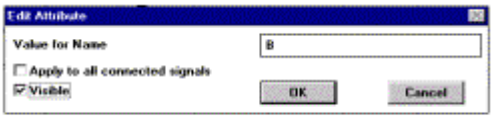


Fig. 10

When you named these wires you should have noticed that in The Timing Window the names appeared. This will later show you the values of these three variables.

Connect the devices together with wires:

- Place the pointer on the end of the wire extending from switch A and hold down the left button, then drag the mouse to an input of the first AND gate. You have now connected the switch for input A to the first input of the AND gate.
- Connect the wire from switch B to the other input of the first AND gate in a similar manner.
- Click on the first input of the second AND gate.

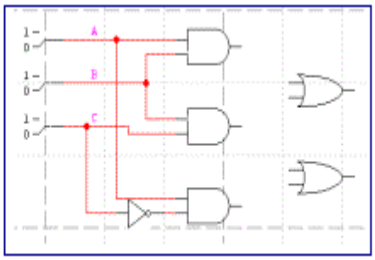


Fig. 11

- Drag a wire to any point of the wire extending from switch B. A dot will appear on the intersection if the wires were successfully connected.
- Connect the C switch wire to the input of the inverter.
- Connect the output of this inverter to one of the inputs of the last AND gate and connect the other AND gate input to switch A. Your design should now resemble the schematic in Fig. 11.

Note: The wire will go around one corner for you, but you may have to stop in the middle of the schematic with one wire and then restart to go in another direction. In addition, an intersection without a dot is simply two wires crossing without making a connection.

- Connect the outputs of two of the AND gates to the inputs of one of the OR gates.
- Finally we connect the output of the remaining AND gate and the output of the first OR gate to the input of the last OR gate.
- A short wire should be connected to the output of the final OR gate and this wire should be labeled Z. See Fig. 12. Notice that the output Z showed up in the *Timing Window*.

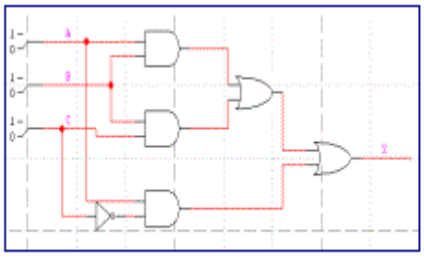


Fig. 12

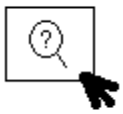
Testing your Circuit:

- Click on the handle of switch A to point to the value 1.

Notice that the A line in the *Timing Window* went up to a high level, indicating the value 1. Also, notice that the Z output went high. This is because A is high and C' is high and according to the equation Z should be high with these input values.

- Change the values of A, B, and C and observe the results in the Timing Window.

  Click on the S*ignal Probe* tool in the Tool Palette.



- Click the tip of the probe tool along any signal line. It will show the current value of the signal as the simulation progresses.

- The *Binary Probe* is a device for displaying the level present on any signal line. Any change in the signal state is shown on the probe. Possible displayed values are 0(low), 1 (high), Z (High Impedance) and X (unknown)

Max terms and min terms:

Q1

.Find Max terms from the following Min terms

(i) F(X,Y,Z) =Σm(1,3,6,7)
(ii) F(X,Y,Z) =Σm(0,1,2,4,6)
(iii) F(A,B,C) =Σm(0,3,4,5,7)

Q2:

For the Boolean function $F1(A,B,C) = \sum m(0,2,3,4,6)$ do the following:

a) Find truth table

b) Find minimal SOP expression for Boolean function $F1$

c) Fill the following table

IC type	Required No. of Gates	Gates per IC	Required No. of ICs
Total no. of ICs			

Q3:

For the Boolean function $F1(A, B, C) = \sum m(0,2,4,6,7,8,10,12,14,15)$ do the following:

a) Find truth table

b) Find minimal SOP expression for Boolean function $F1$.

c) Fill the following table

IC type	Required No. of Gates	Gates per IC	Required No. of ICs
Total no. of ICs			

Q4.For the Boolean functions implement the circuit on Logic Work 4 and make a truth table

F2 = [(A+BC')(A'C')]'+ C

<u>Submission:</u> You have to submit the circuit diagrams and truth table in hardcopy. Use only A4