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Section 2E2
DLD LAB 8

Question 1 Implement 4x1 mux using one 2x4 decoder, four ANDs and three OR gate.

$2^n = 4 = 2^2$

$n = 2$ (select lines)

truth table

S_1	S_0	F
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

1 2x4 decoder
4 ANDs
3 OR

↳ Implementation done on logic works!

Question 2

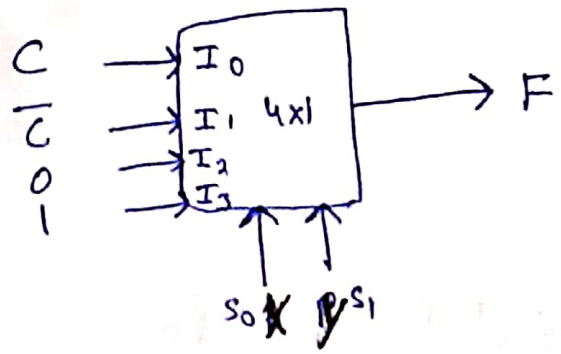
Implement the following function using 4x1 mux.

$F(x, y, z) = m1 + m2 + m6 + m7$

$2^{(2)} = 4$

X	Y	Z	F	
0	0	0	0	C
0	0	1	1	
0	1	0	1	$\overline{C}$
0	1	1	0	
1	0	0	0	0
1	0	1	0	
1	1	0	1	1
1	1	1	1	

Diagram



Question 1

$A_1 A_0$ and $B_1 B_0$ are 2 bit numbers

$A_1 \quad A_0$

$\times \quad B_1 \quad B_0$

$2^1 \qquad 2^0$

$A_1 B_0 \qquad A_0 B_0$

$A_1 B_1 \qquad A_0 B_1$

C_1

$C_2 \quad A_1 B_1 + C_1 \quad A_1 B_0 + A_0 B_1 + C_1 \quad A_0 B_0$

C_2

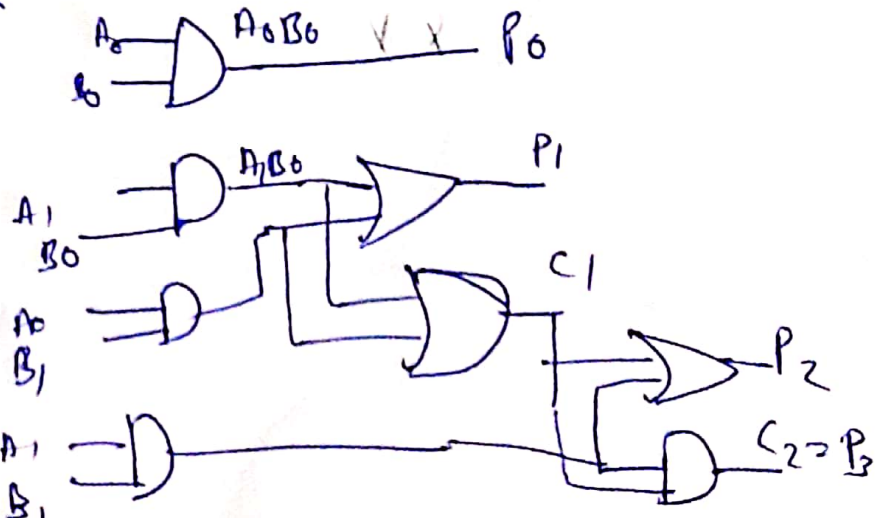
* When you multiply 2, 2 Bit number you output is 4 Bit number

$P_0 = A_0 B_0$

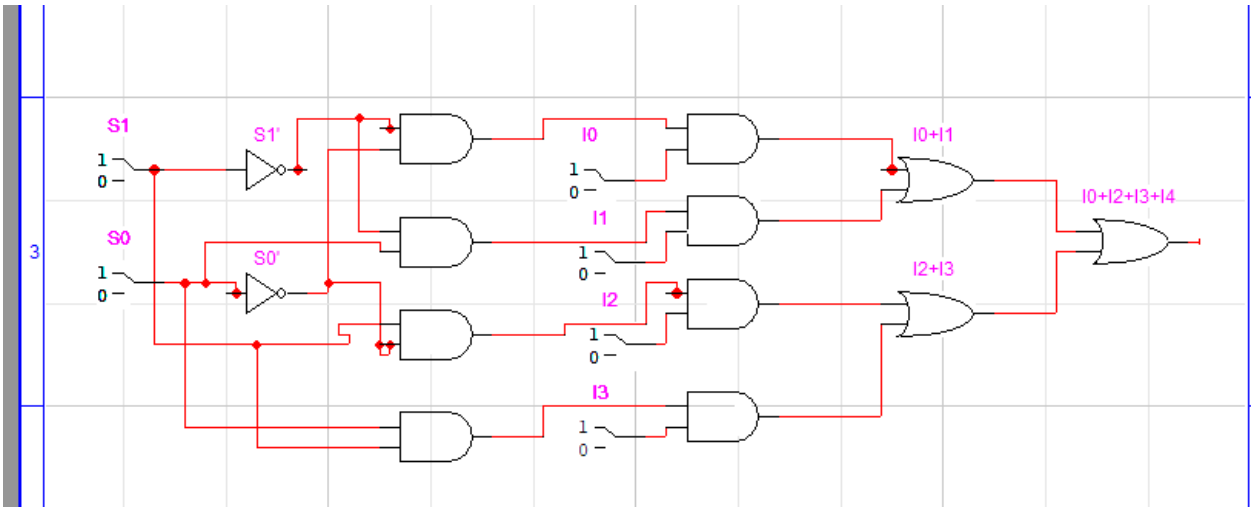
$P_1 = A_1 B_0 + A_0 B_1$

$P_2 = A_1 B_1 + C_1$

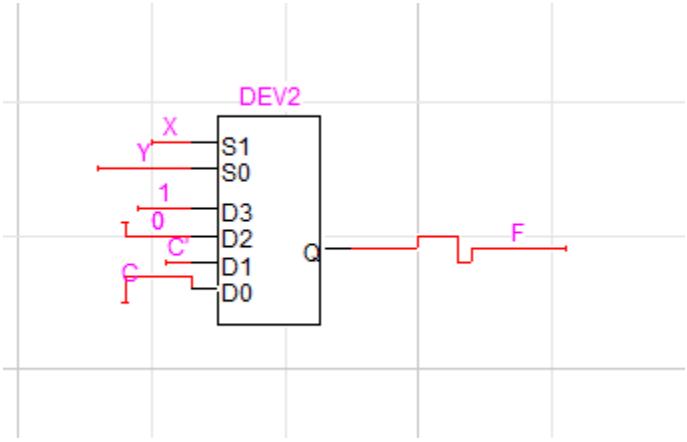
$P_3 = C_2$



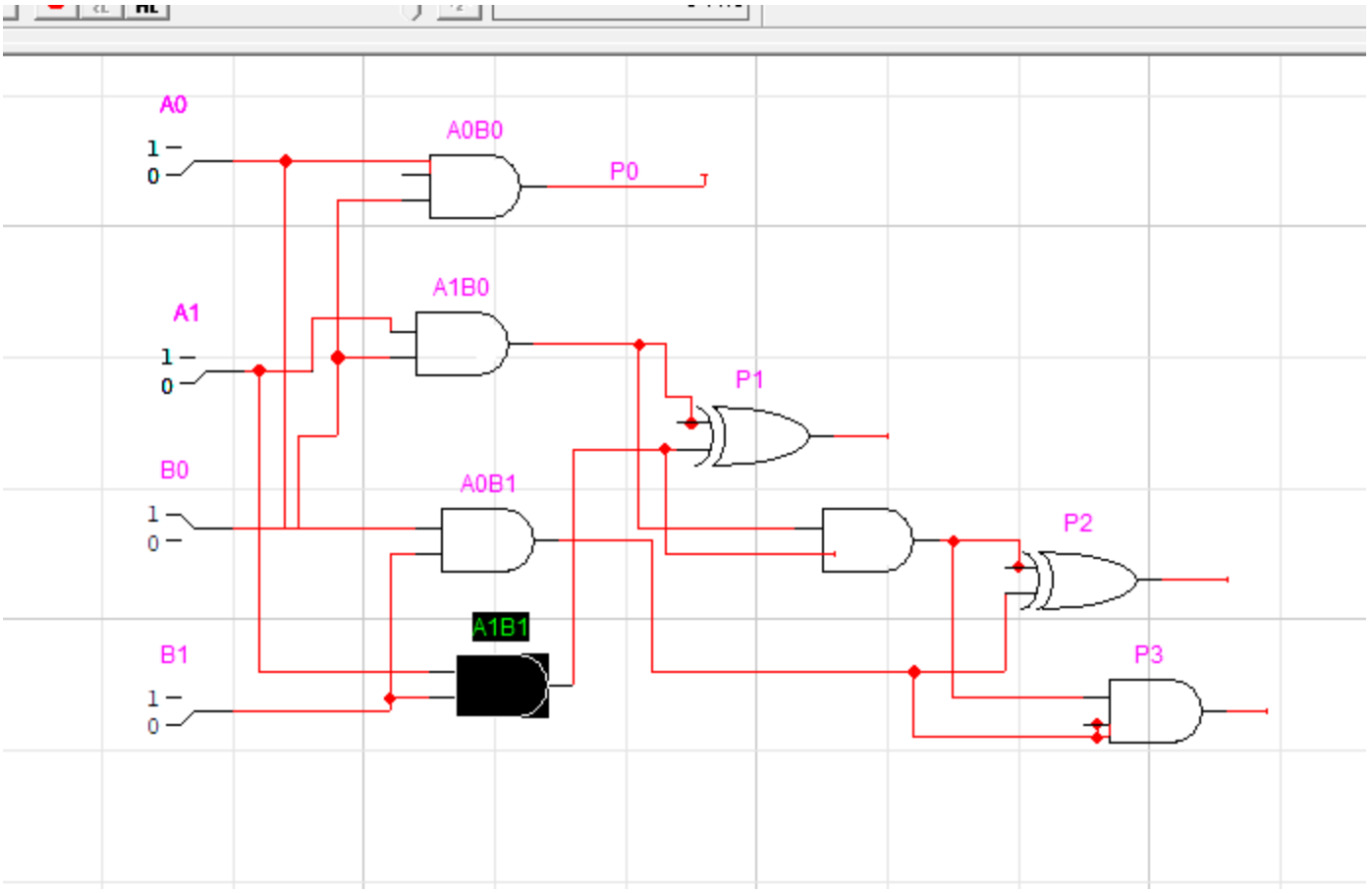
Question 1:



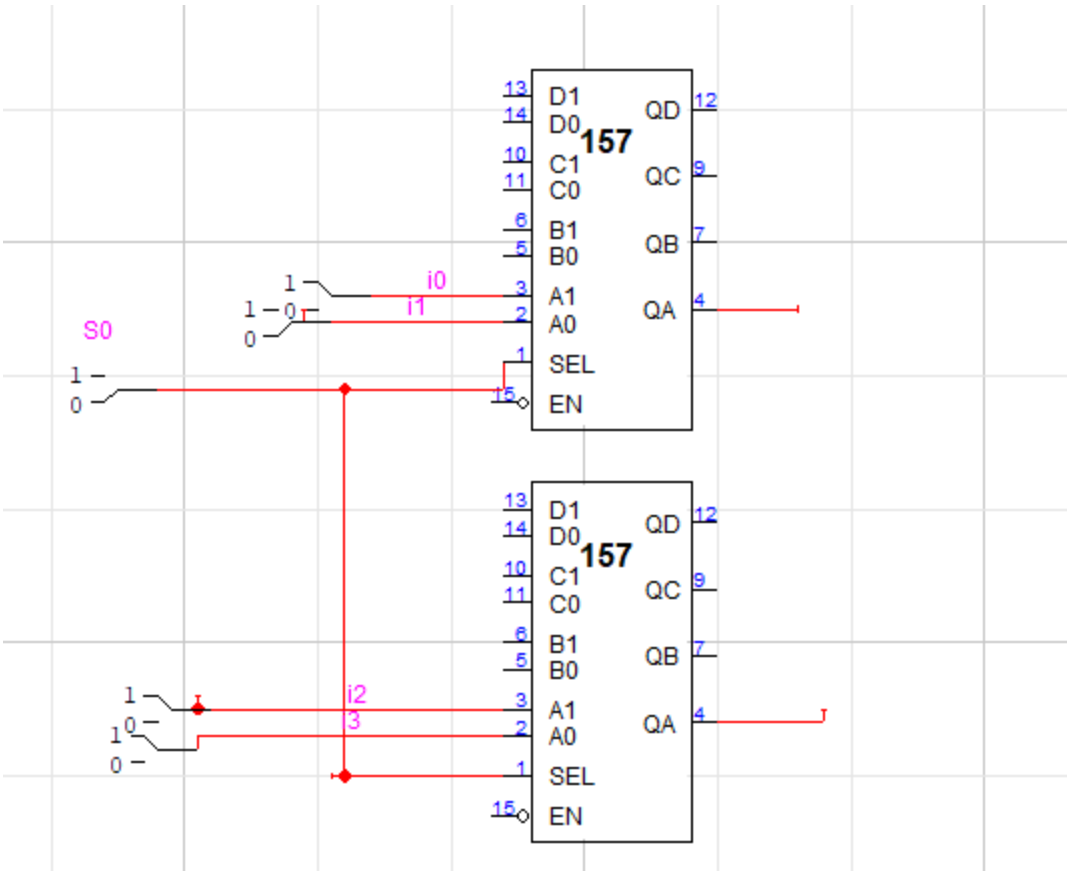
Q2:



Q3:



Q4:


157
D1
D0
C1
C0
B1
B0
A1
A0
SEL
EN
QD
QC
QB
QA
13
14
10
11
6
5
3
2
1
15
12
9
7
4
S0
i0
i1
i2
i3
1
0