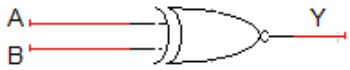
Lab Manual# 7

Objectives:

- To learn and understand how to design a multiple output combinational circuit using XOR and XNOR
- To learn and understand the working of different types of decoders
- To learn and understand how to design a multiple output combinational circuit using Decoders

Exclusive-OR & Exclusive-NOR gates:

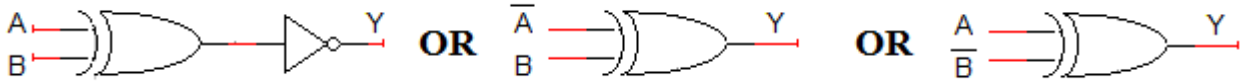
The figure given below shows the symbol of Exclusive-OR (XOR) and Exclusive-NOR (XNOR) gates.



XNOR gate

XOR gate

Boolean expression of XNOR gate is $AB + \bar{A}\bar{B}$ and Boolean expression of XOR is $\bar{A}B + A\bar{B}$. Boolean expression of XNOR gate can be implemented using XOR gate as shown in figure below:



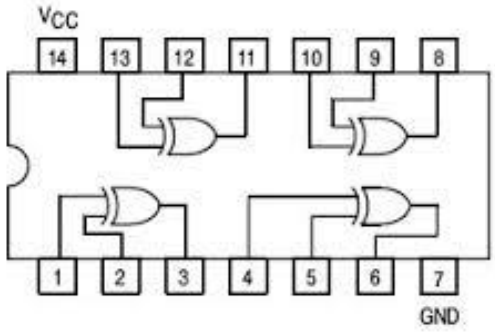
Function Table:

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	H
H	L	H
H	H	L

H= Logic High, L= Logic Low

Connection Diagram:

74LS86 IC will be used for implementation of XOR gate function. **74LS86 IC** contains four 2-input XOR gates. The function table and connection diagram for this IC are shown below:



2-to-4 line decoders:

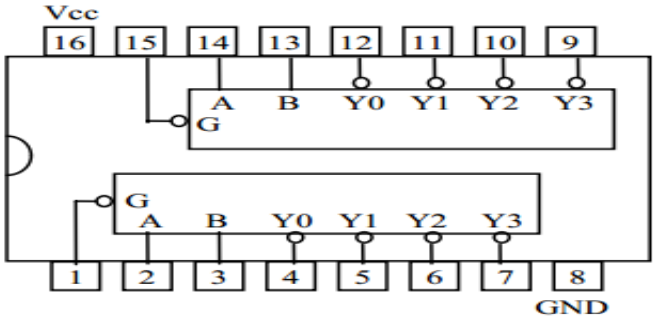
74LS139 IC contains two fully independent 2-to-4 line decoders with active low enables. The function table and connection diagram for this IC are shown below:

Function Table:

Enable	Selection Inputs		Outputs			
G	**B**	**A**	**Y0**	**Y1**	**Y2**	**Y3**
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H= Logic High, L= Logic Low, X= Don't Care

Connection Diagram:



3-to-8 line decoders:

74LS138 IC contains 3-to-8 line decoder. The function table and connection diagram for this IC are shown below:

Function Tables

DM74LS138

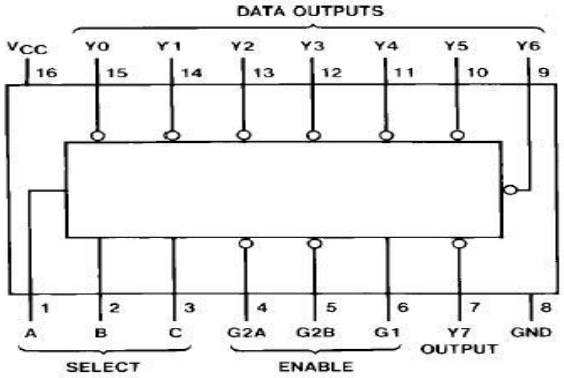
Inputs					Outputs							
Enable		Select										
G1	G2 (Note 1)	C	B	A	YO	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Level
L = LOW Level
X = Don't Care

Note 1: G2 = G2A + G2B

Connection Diagram:

Dual-in-Line Package



Lab Tasks:

Question 1:

Make a truth table and implement **2x4 Decoder with a low enable** using **8 AND gates and 3 NOT gates.**

Question 2:

Implement 3x8 decoder using two **2x4 decoders and NOT gate**

Question 3:

4 bit parity Checker

Implement a circuit that receives **4-bit message** and outputs **Error (E=1) if its parity is ODD**

(Implement it using XOR and XNOR gates)

Question 4:

Implement a doubler circuit. It takes a **3 bit input** and multiplies it by two and gives a **5 bit output.**

(Implement it using XOR and XNOR gates)