INVITED PAPER

Enabling Electronics With Physically Flexible ICs and Hybrid Manufacturing

We discuss the benefits and challenges of taking a hybrid manufacturing approach that integrates traditional, yet flexible, electronic devices with printed components to meet performance requirements.

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ABSTRACT | Printed and flexible electronic components have been used and proposed in a wide range of markets, including biomedical, environmental, computers, energy, and communication. Fully printed and flexible electronic systems promise great advantages in ease of manufacture, weight, durability, and physical conformity, but such systems have failed to achieve widespread adoption. Printed technology still seeks solutions in the areas of complex logic, analog circuitry, power usage, and light emission. First, the benefits and challenges of taking hybrid manufacturing approaches that combine printed components with either traditional integrated circuits or recently fabricated complex flexible devices are discussed. Second, a recently realized set of physically flexible integrated circuits poised to accelerate the development of flexible sensor systems is presented, enabling the combination of low cost and large format printed systems with high performance and low-power silicon-based semiconductors. The chip set addresses the three requirements of flexible sensor systems, namely, sensor readout, signal processing, and communications with three chips—an analog-to-digital converter, a microcontroller, and an RF communicator. This technology may revolutionize such things as smart, wearable consumer devices, flexible and conformal industrial applications, and smart structures for military, automotive, and aerospace.

KEYWORDS | Flexible electronics; flexible printed circuits; hybrid integrated-circuit fabrication; hybrid integrated-circuit interconnections; hybrid integrated-circuit packaging; hybrid integrated circuits; integrated-circuit manufacture; printed-circuit fabrication; printed-circuit layout; printed circuits; product development; remote sensing; structural engineering

I. INTRODUCTION

Printed and flexible electronics (PFE) have been proposed to revolutionize multiple markets—health care, environmental monitoring, displays, and human-machine interactivity, energy, communication, and wireless networks. Their concept appears to provide a likely path to truly all-embracing electronics. The potential benefits of printed and flexible electronics include thinness, lighter weight, greater durability, and the ability for conformal integration. However, printed and flexible electronics have thus far failed to achieve widespread adoption; and broad commercialization continues to be perennially "just around the corner."

Significant unresolved technical challenges are assignable to this lack of commercial success. These issues include the focus on all-printed solutions, and major gaps that exist between expectations and performance of printed electronics in the areas of logic, memory, analog circuitry, power, and light generation. The maturity and performance characteristics of proposed printed solutions and a lack of focus on manufacturability and technology integration of known solutions are particularly problematic. We hope to close those gaps with a more inclusive

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view of flexible technology. In this paper, we will consider and contrast the all-printed solution with two hybrid approaches as follows.

1) Reliable integration of conventional electronics with mature and manufacturable printed flexible materials to produce flexible subassemblies.
2) Flexible single crystalline silicon electronics as a solution for logic, memory, and analog circuitry in the absence of adequate performance in printed or partially printed electronics.

We first discuss the benefits and challenges of fully printed electronics. This is followed by a discussion of the limitations of the manufacturing approach of integrating printed electronics with established Si-based manufacturing to meet customer-driven performance requirements. This has become known as the hybrid approach.

One example of this approach is a biosensor intended to be attached directly to the skin which wirelessly communicates with a diagnostic system [1]. The approach optimizes a viable response to the unresolved technical challenges by utilizing the advantages of each approach: the high performance and low power of silicon-based semiconductors and the cost effectiveness, scalability, and large formats possible with printed systems.

Finally, we introduce the second approach with recent developments called flexible hybrid systems (FHS) where printed electronics are integrated with flexible silicon-on-polymer (SoP). A physically flexible integrated-circuit (IC) chip set based on SoP optimized for flexible hybrid integration will also be described. This chip set is intended to accelerate the development and integration of flexible sensor systems—a key application area for FHS.

Integration of the new flexible devices adds somewhat to the challenge but will bring major benefits. The integration steps under development are discussed as extensions of conventional attach processes, using a problem/solution approach to develop what are now highly reliable attachments. These are discussed in the context of available printed sensor technology.

II. PFE ADVANTAGES

By virtue of the available form factors, PFE techniques enable electronic functionality to be delivered in locations and formats that cannot be achieved with conventional electronics' packaging and assembly approaches. Printed electronics and specifically PFEs are electronic systems that are created using printing techniques to apply materials to define circuit interconnects and devices. Conductive inks include printable materials that can be composed of metal nanoparticles. Substrate and dielectric materials include materials, such as polyethylene terephthalate (PET). Active devices, such as thin-film-transistors (TFT) and sensors, can also be printed using a variety of materials. Circuits, substrates, and devices for PFE can be printed using a variety of methods that include screen printing, inkjet, and a wide variety of emerging roll-to-roll (R2R) methods. To the extent that PFE can be executed on existing printing and curing (drying) systems, the approach provides the opportunity for electronics to be manufactured at low manufacturing costs by utilizing a large installed capital equipment base. To maintain that advantage requires that the printing approach be used only where it is effective and efficient. We will return to this argument later when we describe the hybrid approaches, which maintain that efficiency with the strategy of "print what you can and add silicon where you must."

As with any technology, it is important to understand where the use of the technology allows its true value to be realized. For PFE, arguably the value resides in the form factors available, the scalability that additive manufacturing provides, and the intrinsic integration available where such a manufacturing process permits the opportunity to skip later assembly steps. These three elements are all supported by a mature and efficient manufacturing approach.

A flexible form factor and format are required to enable new low-cost manufacturing methods and to meet new application demands for conformal and flexible systems. Having been developed over centuries for use on paper, the printing process clearly supports the additive construction through selective deposition of functional materials in a thin flexible format. Because of this flexibility and the ease of building to arbitrary envelopes, printing lends itself to the construction of devices which can be used and applied in environments where previously available form factors either were a poor fit or no fit at all. Wearable devices, for example, have been met with limited success as long as they have remained in a form which can be fairly described as slab and strap—a rigid functional piece using conventional electronics and packaging attached by strap or by adhesion to the body. The conformability available through the use of materials well suited to printing can be exploited directly with the fashioning of electronic devices to be worn, with a more comfortable and conforming device format. Alternatively, formats can be made to be built in (or molded in) to other envelopes in fully conformable configurations, such as in switch assemblies or airframes. Alternately, the flexibility can be used to make circuit-based devices fit efficiently into shapes for which space utilization has previously been poor. Circuit boards rolled into cylinders, for example, can provide a more efficient use of space than stacks of flat rigid boards. Likewise, the problem of conformability to the body can be addressed now with thin flexible devices, enabling the broader acceptance of wearable electronics, whether it is for diagnostic or therapeutic purposes, or purely for convenience.

Scalability is a key consideration for manufacturing. Printing is a process which offers a high degree of flexibility in the scale of the part and the scale of the production volume. Electronic sensors have been used for biometric and other sensing for some time now. However, silicon-based systems (for example, sensor elements) are often

limited in their size or extent by the fact that ultimately the cost of the device is driven by the area of silicon used. Thus, a sensor system with a characteristic dimension of, say, 3 in is unlikely to be made from a single piece of processed silicon, or a single sensor. Rather, it will have been assembled from many separate pieces with all of the concomitant challenges in ensuring uniformity and continuity of response along with the cost of handling and assembly. In contrast, the technique and design of a printed object are in many ways independent of the scale. Consider, for example, a thumbprint sensor. Use of a silicon base for this sensor would be costly; use of a printed approach much less so, assuming that the necessary performance could be achieved with a printed approach. Scaling such a device to provide registering an infant's footprint electronically is out of the question for silicon; not so for a printing-based solution.

The intrinsic scalability of printing as a manufacturing process is also of great advantage; the process lends itself to production runs of an arbitrary size. While the economic details of run-size may favor one or other of the many particular printing processes to be used, the common feature is that once the initial set up has been achieved, it is a very simple matter to make an arbitrary number of that same design. There is no overhead associated with assembly to limit the productivity of a printing run.

A practical manifestation of these advantages is in such applications as needed for distributed sense and respond capability. For example, an array of temperature sensors using silicon thermistors would conventionally require the assembly of individual devices on a separate support and then the provision of interconnection between and amongst them and their readout electronics. In the case where many sensors are used, or where the size of the area is large, the cost of the assembly operations can be expensive, to say nothing of the sensors themselves, each of which has been individually formed and packaged. However if the entire assembly can be printed, much of that expense can be limited. The integration of the sensor units, their interconnection, and any associated processing not only leads to manufacturing efficiency but also to higher reliability in part due to the absence of solder joints. Arrays of sensors not only have application in wearable systems, but also in structural health monitoring for building or airframes. Not only sensing, but control and response can also be distributed with the use of inexpensive printed arrays, assuming that signal conversion, data processing, and communications are feasible.

Traditional microelectronic technology is ill-suited to applications that require dimensions greater than 1 cm. Traditionally, this has been resolved with rigid printed-circuit boards (PCB) bridging the area required between high-performance integrated circuits (ICs). PFE can go beyond the large-area multilayer interconnects of printed-circuit boards (PCBs) and support system sizes of almost limitless proportions. Printed electronics offer several benefits based on flexibility, large formats, and mass production manufacturing processes. Printed electronics inherently lend themselves to flexible applications and can be fabricated on roll-to-roll production equipment. This enables specialized sensors and sensor networks to be fabricated, potentially of almost any size and on a wide variety of materials, including elastics and textiles. The use of printing technology enables a cost-effective production process by virtue of using a mature and reliable manufacturing process and through selective deposition by allowing the minimum quantities of costly materials to be used. However, printed transistors cannot meet the requirements for high-performance memory and logic functions due to low electron mobility, large feature sizes, and relatively high-power consumption.

III. PFE CHALLENGES

Printed active devices today have very limited performance. A significant limitation of the printing processes and materials available today is the inability to print active electronic devices entirely. Instability in materials, low electron mobility, the small scales necessary, and the extremely tight registration requirements all limit the utility of transistors which can be printed readily. The results are transistors with high threshold voltages, low switching frequency, and poor lifetime. Consequently, while it is possible to make transistors of some utility for switching or digital applications, in general, it has not yet been possible to make transistors of sufficient quality and uniformity to be used in precision analog circuits that would be useful for instrumentation and signal conditioning purposes.

For example, while printing can produce reliable and versatile sensing probes (either singly or in arrays), these do not offer much without a suitably formatted processing capability to read the sensors, condition the data, communicate it, and perhaps display it. These tasks are beyond the present abilities of purely printed electronics. This is true if for no other reasons than that of the number of transistors required and the required speed, both for display driving and for digital conversion and power.

Many other aspects of the needed electronics capability are also absent in what can be printed today. The absence of well-matched transistor pairs is a significant factor because it limits the ability to print instrumentation class amplifiers. An additional problem, which works against printing, is the ability to support extremely fine-pitched devices. This limits even some aspects of developing hybrid solutions with conventional ICs. The rheology of conductive inks limits the metal content of very fine lines. Thus, even if they are of limited length, the resistance they present may be too great for practical use.

A final impediment to the fully integrated use of printed electronics is the absence of standardized design rules. The printed industry's design methods are derived from approaches common to print, graphics, and illustrations. Electronic and microelectronic design methods are

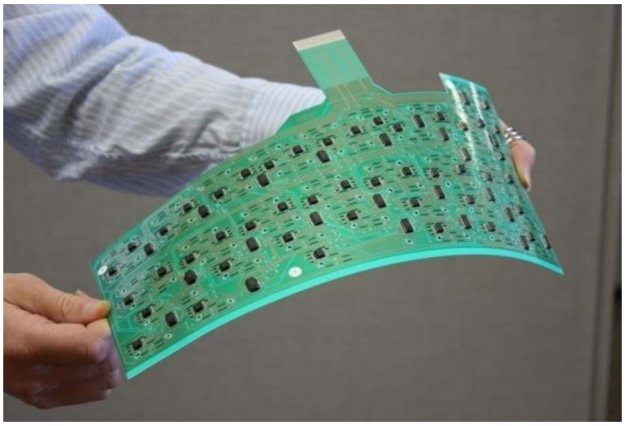

Fig. 1. ***Five-layer hybrid flexible circuit board.***

based on physics and circuit design. The integration of these two disparate approaches into a cohesive hybrid design flow is a major challenge that PFE manufacturers are currently working to resolve.

The example shown in Fig. 1 illustrates how printed elements in combination with conventionally packaged active elements have been used together to help solve these performance limitations.[1]

IV. HYBRID APPROACH

The convergence of the use of PFE, with its advantages in available envelope and format, with the performance of conventional electronics has become known as the hybrid approach. It adopts the philosophy of printing what has value in printed form, and attaching integrated devices that cannot be printed. A PFE hybrid is created when non-printed technologies, such as single crystalline silicon ICs, are integrated with PFE. Flexible hybrid integration of printed electronics and conventional silicon ICs has become an accepted near-term solution for flexible system commercialization. Hybrid systems were suggested as early as 2009 as an approach that could provide the necessary performance for fully flexible systems [2].

While this approach has many appealing properties, it also presents significant challenges and limitations. The absence of well-matched adhesive and conductive ink combinations makes attaching rigid packages to flexible substrates very difficult. In addition, maintaining that attachment while flex and band stresses are applied, elevates the mechanical integrity challenge to levels not usually encountered in electronics. Finally, package design, especially for complicated ICs, is seldom compatible with an overall flexible assembly. These challenges have, to date, limited the success of hybrid systems and lead us to seek a more fully flexible system construction.

[1]Image courtesy of Soligie Print Electronics, www.soligie.com

A. Mature Silicon Technology Performance

Conventional silicon ICs provide the best performance and the most mature technology for high-performance microelectronics. This is most relevant for complex logic, memory, and communications ICs as well as precision passive devices, such as capacitors and resistors. Modern complementary metal–oxide semiconductor (CMOS) ICs are unparalleled in performance. This extreme capability is derived from the high-mobility single crystalline materials and high density circuits that cannot be replicated with printed components. Mainstream low-cost 8-b microcontrollers, considered relatively simple in the IC industry, operate below 1.5 V and that can include more than 2 million transistors—orders of magnitude higher performance than the best printed transistor circuits. The low operational voltages result in very low power consumption which today's higher voltage printed circuits cannot match. The examples below illustrate the use of printed elements in combination with some conventionally packaged active elements.

B. Attachment Concerns

The attachment of IC packages to thin flexible substrates is challenging. Several factors combine against a highly reliable union. Metallization of the package itself as well as incompatibilities of the adhesive and conductive materials in use raise particular problems. These are exacerbated by the need to maintain attachment while the circuit is flexed.

Recent work has shown attachments which resist shear forces of some 10–15 kg and survive bending of the substrate under loads over radii of curvature which are comparable to the characteristic dimension of the IC packages. Not only is there high mechanical integrity, but the electrical continuity is well maintained in these circumstances also. It is not yet clear, however, what the manufacturing readiness level of the technique is. However, since the failure modes of this approach can either fracture the IC or rupture the substrate, there is cause for optimism. The practical limits to implementing the hybrid approach are being reduced.

In addition, the need to use noneutectic methods for making connections to the die/IC when it is attached brings additional challenges and, at best, is unfamiliar to many manufacturers of conventional electronics. Because of the use of inexpensive polymer substrates and of polymer inks, attachment in most cases has to be achieved using conductive and other epoxy adhesives. These methods also add to the effective resistance in the circuit. A fully printed solution can build ways around this restriction, but a hybrid using conventionally packaged ICs and printed interconnects does not provide the best solutions. Conventional rigid packages fail to meet reliability requirements when bent or flexed. A further consideration is the limited power handling capability of purely printed electronics. On the one hand, the required

power is sufficiently high in order to make these unattractive for lower power solutions, while on the other, the current carrying capacity of typical printed transistors is small. Thus, while the speeds may be adequate for some power switching applications, the power handling capacity is not.

C. Design Reuse

Beyond the issue of overcoming the limits of PFE, a key advantage of using silicon in hybrid systems is the reuse of mature designs. Microcontroller and application-specific integrated-circuit (ASIC) designs at 130 nm, a prime technology node for hybrid systems, can cost in excess of U.S.$1 000 000 to develop per design. This cost does not include the development of software associated with operating and using the devices. Decades have been spent designing and perfecting a wide variety of semiconductor intellectual property (IP). Reuse of this IP provides immediate support for the modern features required in hybrid systems.

Conventional bare silicon die are broadly available at this time. However, conventional die, even the ultra-thin versions, provide significant challenges for integration and reliability in hybrid applications. The difference in mechanical deformation when bent can result in serious reliability problems.

Unfortunately, the reality of combining conventional microelectronics and printed technology is that purely printed electronics, even when combined with conventional packaged silicon, fails to provide a good flexible or conformal solution. For hybrid systems to overcome the limits of conventional microelectronics, an alternative form of silicon is required.

D. Example Hybrid Assemblies

Minimizing assembly steps is always a significant consideration. As indicated before, the ability to print objects of limited size uniformly over large areas is an essential feature of printing. In addition, printing lends itself to the integration of devices in the same process as a base circuit is printed so that further assembly is not necessary. In Fig. 1, we show a five-layer "circuit board" formed by selective deposition on a 10-mil PET substrate.

The printed-circuit board (PCB) of Fig. 1 has five conduction layers representing the ground plane, dielectric, circuit traces, dielectric, and top layer circuit traces, in addition to a set of some 400 resistor elements that have been printed during manufacture as an integral part of the structure. Thus, not only are later (slow and costly) assembly operations such as "pick and place" reduced or eliminated, but the reliability of the device has been enhanced by the avoidance of solder joints. The overall thickness of the printed circuit is approximately 12 mil (300 μm) and the low weight of the passive components so formed also enhances the reliability against shock and acceleration forces for the final device.

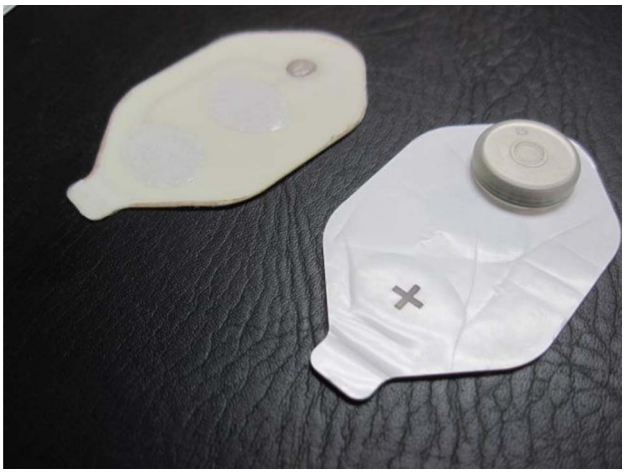

Fig. 2. *Iontophoretic drug delivery patch.*

Utilization of this general printing approach has produced a number of good examples of PFE-enabled flexible systems. Dharma Therapeutics introduced an iontophoretic drug delivery patch some years ago which overcame many of the disadvantages of the previously available wearable devices (Fig. 2). In this case, the particular circumstances of the device pointed the way to what was essentially a hybrid device, although perhaps it was not conceived that way.

The product was a single-use drug delivery patch, for which the iontophoretic circuit was powered by a removable electronic assembly. The drug-containing element was soft and flexible, and when manufactured efficiently as a two-sided circuit, was economical to use in its disposable format. The electronics assembly contained a precision current-controlled power source to enable very precise drug delivery rates. The capabilities of that circuit were very much more advanced than anything printable at the time (or now) but the patch itself was ideally suited to the capabilities of printing. Together, the power source and the patch were a well-matched hybrid solution to the challenge

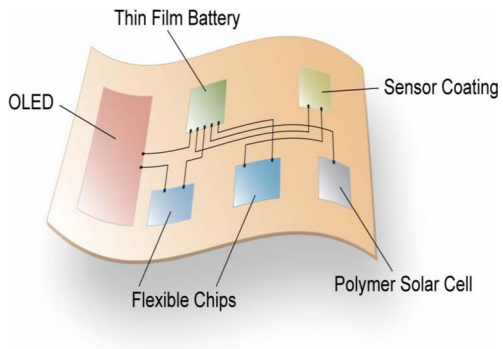

Fig. 3. *Hybrid systems-in-foil (2009).*

of a comfortably wearable, precisely driven medical application.

Another well-known application with similar characteristics is the ubiquitous glucose strip. Here, the strip itself is the printed object, essentially a sampling volume embedded within a probing circuit. The electronics are entirely conventional and contained within the hard-cased control system. Once again, the distinction between printable and not-printable is recognized and, in this case again, matches the demands of a disposable and reusable component.

V. FLEXIBLE HYBRID SYSTEMS (FHS)

The development of hybrid concepts has resulted in the emergence of FHS. FHS is a flexible electronics hybrid that is differentiated by the utilization of flexible silicon-on-polymer (SoP) ICs rather than conventional packaged ICs or bulk silicon bare die for the single crystalline silicon devices. SoP is a single crystalline IC technology that results from the conversion of conventional silicon wafers to SoP by replacing the majority of the silicon wafer with a polymer. SoP ICs retain the functionality of conventional devices, but are fully flexible and ultra thin.

FHS is a hybrid technology that utilizes SoP to provide the performance that PFE needs and the format that conventional packaged ICs or bare die cannot reliably provide. SoP has the capability to mitigate the reliability issue by having deformation characteristics much closer to PFE than bulk silicon. The simplest understanding of this is that SoP, like PFE, is a material that is engineered to bend. This approach addresses the full technology solution necessary for modern electronic products in the desired flexible format. FHS can include power sources and displays as part of the hybrid integration.

A roadmap for FHS has been derived from the synergistic convergence of PFE technology and ultra-thin silicon technology. PFE includes a variety of new materials, sensors, thin-film transistors, and interconnects that can be printed in a variety of cost-effective methods in a variety of formats. Ultra-thin silicon technology has evolved beyond conventional bare die and now includes SoP that can provide the high-performance electronics features that modern systems rely on. The proposed roadmap to hybrid integration, shown in Fig. 4, represents a feasible mid to longer term approach for manufacturing thin flexible electronic systems.

Today, the industry is establishing the PFE and SoP silicon manufacturing capability necessary to support the emerging FHS approach. Near-term development is planned for FHS development kits that product designers can use to implement and demonstrate new products based on flexible and conformal formats. New products will emerge once the FHS technology is proven, demonstrated, and capable of meeting new-product market requirements.

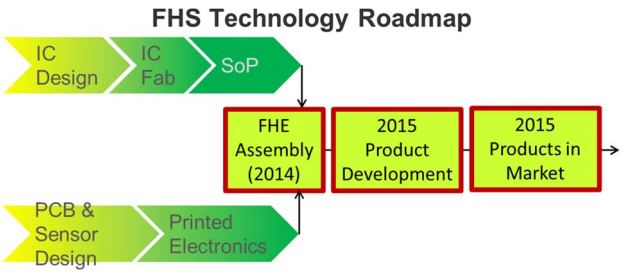

Fig. 4. *Planned FHS development.*

VI. SOP ENABLING FHS

SOP ICs are the key to FHS success. FleX is a SoP process that converts standard silicon-on-insulator (SOI) wafers into flexible SoP wafers. The process has been demonstrated by fabricating flexible, ultra-thin, single-crystalline CMOS with multilayer metal interconnect [9]. SoP technology provides IC functionality that is essentially the same as conventional ICs, with orders of magnitude faster performance than printed transistors [10]. SoP wafers are derived from conventional semiconductor foundry wafers. CMOS is first fabricated using a standard SOI process on 200-mm wafers and then the silicon handle substrate is removed and replaced with a polymer. FleX SoP processing removes all of the rigid handle silicon to create ultra-thin, high-performance flexible wafers in 130-nm CMOS.

The hybrid integration of conventional electronics with flexible materials has faced the challenge of incompatibility and unconventional materials and, thus, the inability to evaluate the resulting products by means of widely accepted reliability criteria. Newly emerging SoP technology for CMOS shown in Fig. 5 transforms high-performance, single-crystalline silicon wafers into flexible wafers for

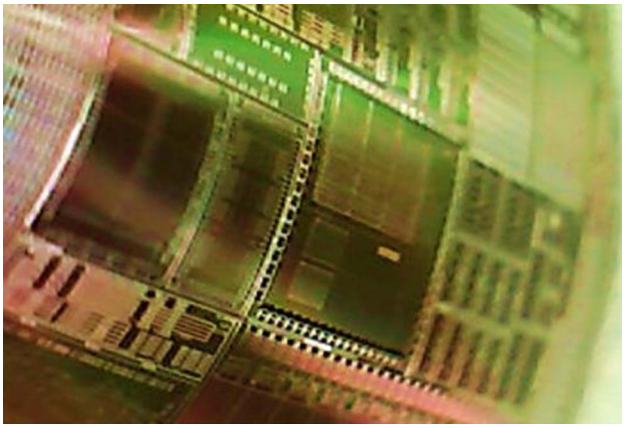

Fig. 5. *Silicon-on-polymer (SoP) thin flexible wafer.*

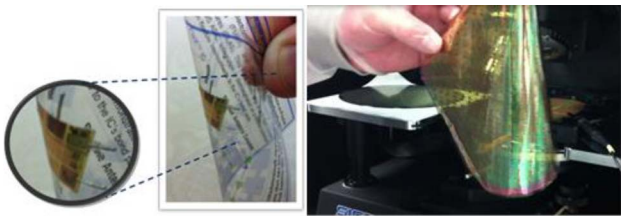

Fig. 6. ***FleX: Flexible, ultra-thin, and high-performance CMOS.***

flexible ICs designed explicitly for flexible hybrid integration [2]–[4].

The FleX SoP postfabrication process can be applied to any SOI CMOS wafer and has been demonstrated on three different CMOS processes from two different CMOS wafer foundries. FleX delivers fully functional, flexible wafers with a final silicon thickness of less than 200 nm [6], [7]. This process has been verified with functional CMOS wafers, which in June 2012 were successfully launched into space under the NASA RockSat[2] program. The RockSat program exposed the ICs to an environment known to produce high loads under both vibration and shock, thus providing validation that the intrinsic lightweight structure of the IC effectively reduces the stress loads it experiences.

A particular advantage of this approach to flexible IC construction is that few additional design rules are required. The porting of tried and true designs from the Jazz process maintains their original validity and introduces only minor changes in parasitic capacitance.

Research into the requirements for a wide variety of biomedical, commercial, and defense sensor applications identified general electronics requirements that are common to almost all applications. A three chip set addresses the requirements of many flexible sensor systems: sensor readout, signal processing, and communications. All three chips have been fabricated in a common high-volume commercial wafer fabrication foundry. The three integrated circuits (ICs) described in Fig. 7 demonstrate the migration of a known CMOS process, in this case, the CS18 (0.18-μm design rules) SOI CMOS from TowerJazz,[3] into the SoP format. The ICs benefit from the reuse of standard semiconductor design rules for fully established commercial manufacturing. These ICs may be used as a complete system or individually to address specific needs. The technology enabled by this IC chipset can easily migrate into smart, wearable consumer devices, flexible and conformal industrial applications, and smart structures for military, automotive, and aerospace [5].

Recently demonstrated functional devices of all three members of the chip set have been completed

[2]http://www.nnu.edu/news/2013/08/12/nnu-engineering-team-to-launch-electronics-on-nasa-rocket/

[3]Tower Semiconductor Ltd., and Jazz Semiconductor, Inc.

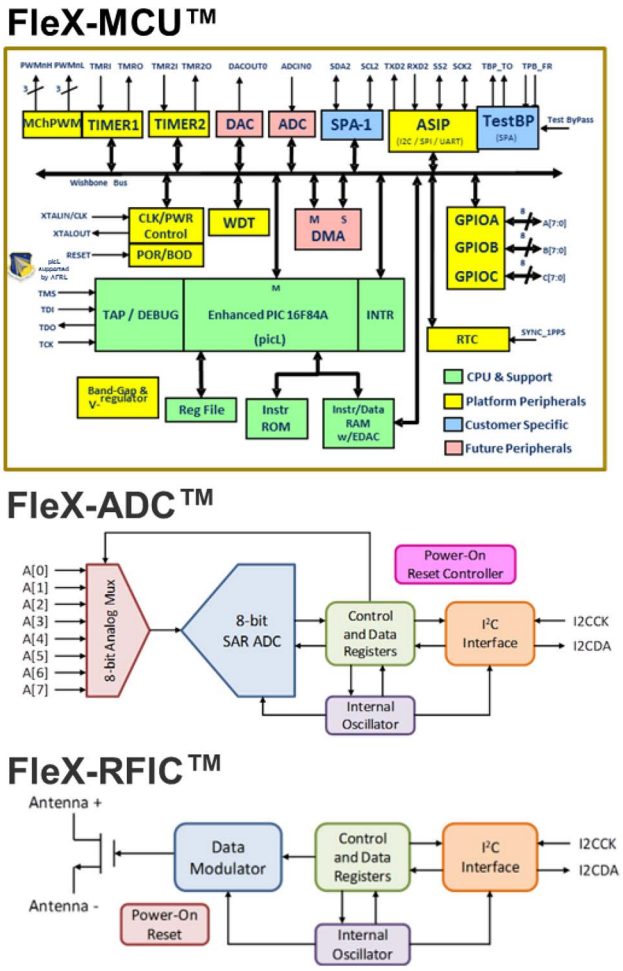

Fig. 7. ***FleX chip-set description.***

with laboratory tests on wafers before and after SoP processing.

- FleX-MCU is functional for most tests up to 8 MHz. Power requirements for low-core voltage and current are 1.5 V and 0.84 mA, respectively, while running at 1 MHz. Input/output (I/O) voltage is 2.5 V with an I/O current of 10 mA and up depending on the number of pins driving, signal frequencies, and loads driven.
- FleX-ADC has shown both I2C communication and data-conversion capability. Fig. 8 graphs the prototype linearity. Some noticeable nonlinearities are evident which are not believed to be caused by the flexing process. Corrections have been made for the next fabrication.
- FleX-RFIC is also functional at data rates of 64 and 256 kb/s.

Detailed characterizations are ongoing. Test results for these prototypes illustrate the ability of SoP technology to retain the performance of the conventional IC technology and they are derived from [5].

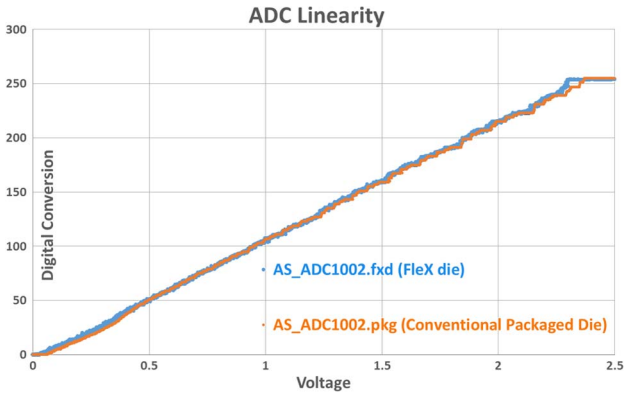

Fig. 8. *AS_ADC1002 8-bit ADC performance comparison.*

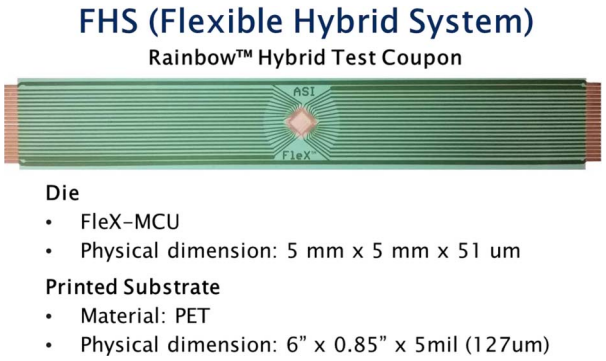

Fig. 9. *FHS development test coupon.*

VII. STATE-OF-THE-ART FHS MANUFACTURING

FHS, as illustrated in Fig. 9, has become a flexible electronics industry strategy due to the technology's capability for combining conventional electronics with printed materials to provide the features and performance that are required for modern systems.

Leading flexible electronics suppliers and researchers are currently engaged in frontier research to integrate silicon and PFE technologies. In 2014, at the LOPEC Conference in Munich, Karl Ronka,[4] Mike Clausen,[5] and Marc Koetse[6] each presented their advances in the development of hybrid die-attach and interconnect approaches [6]–[8]. Most recently, Heitzinger[7] and Hackler[8] completed the initial demonstration of a fully capable integration method that can be supported with high-volume industry-standard equipment. This new method was demonstrated with a mechanical test die that mimics the material characteristics of flexible SoP CMOS ICs and provides on-chip test circuits for opens and shorts verification. The mounting and the connection of the mechanical die on the printed flexible substrate was facilitated using an anisotropic conductive material. While formal testing continues and will ultimately be reported quantitatively, the demonstration device illustrated in Fig. 9 permits the user to flex and twist the assembly over a mandrel with as small a radius as 5 mm with no loss of continuity or functions. Fig. 10 shows a typical flexure of the assembled FHS system mounted to a demonstration board.

Fig. 10. *Demonstration of the FHS attachment showing continuity under flexure.*

The ability to provide functional silicon in the thin flexible format, which matches that of PFE, provides a fortunate complementarity in performance. Where printing alone cannot reach the performance levels expected and needed in modern sensing and communications devices, the addition of SoP in a hybrid solution with printed electronics achieves a satisfactory combination of the attractive aspects of both worlds.

The current state of FHS availability and development is rapidly evolving. The hybrid approach to flexible electronics systems is not entirely new; it is, however, entering a new phase of higher maturity with performance and characteristics which will encourage wider use. In the last year, researchers have developed perhaps the best example of a truly hybrid solution to a modern sensing problem. A device has been built where the partition between a reusable and replaceable system has been exploited. Here, the value of interchangeability of sensing functions has been recognized while making use of a single (more expensive) central control and readout device. The application shown schematically in Fig. 11 has printed electronics on the control and readout module and on the sensor modules. The device has been demonstrated with both printed temperature sensors[9] and with printed pressure sensors.[10] The

[4]VTT, Finland, www.vtt.fi
[5]CPI, UK, www.uk-cpi.com
[6]Holst Centre, Netherlands, www.holstcentre.com
[7]Soligie Print Electronics, USA, www.soligie.com
[8]American Semiconductor, USA, www.americansemi.com

[9]Printed Silicon Technology, www.pstsensors.com
[10]Soligie Print Electronics, www.soligie.com

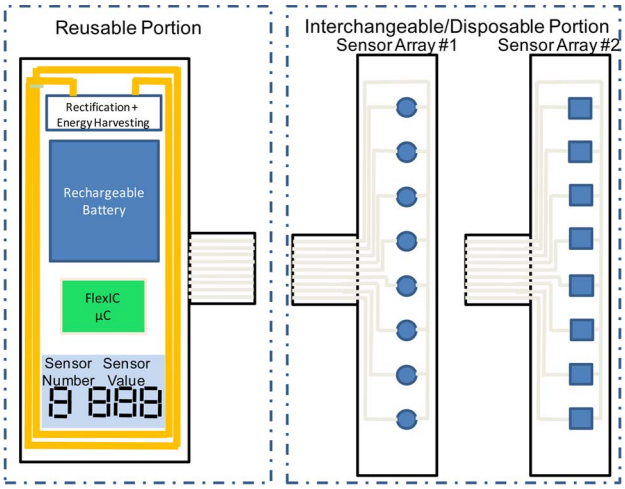

Fig. 11. *FHS consisting of a reusable power and control/readout module and replaceable sensor arrays.*

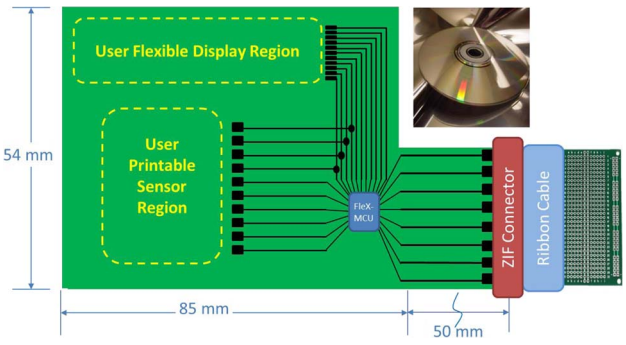

Fig. 12. *FleXform development kit.*

performance of these sensors is well suited to common (consumer and technical environment) uses. Temperatures between about −40 and +120 °C and forces of as little as 2.10–4N can be sensed and displayed. For both of these options, a single control and readout module is used and has been made with an FHS approach. In this case, a circuit with a contactless charging capability as well as control and readout was included along with a thin flexible display. Each interchangeable sensor array is recognizable by the FHS when attached. The system is designed to use the FleX microcontroller unit (MCU) with the FleX analog-to-digital converter (ADC) and/or FleX radio-frequency integrated circuit (RFIC) to demonstrate functional attachment and integration of these SoP devices. The further ability to sample and interpret printed sensors and display meaningful data on a flexible display will be a clear step forward for flexible systems.

VIII. DEVELOPERS' KITS

Prospects and projected hybrid capabilities provide a bright future for the flexible electronics industry. High utility hybrid products are emerging to support printed sensor systems with integrated processing. For example, FleXform, shown in Fig. 12, is a developer's kit intended for use by product developers and engineers during early prototyping of new products. The FleXform kit is a fully functional FHS composed of a printed flexible multilayer substrate and FleX ICs including MCU, ADC, and RFIC. FleXform will be supported with hardware and software interfaces that will allow the developer easy access for programming and debugging each chip as needed for the specific application being demonstrated.

An example of one approach to flexible product development describes how a flexible product can be realized. First, viable and demonstrated technology must be available. Commercial companies provide the necessary building blocks, such as printed sensors, printed substrates, and ultra-thin silicon ICs—including SoP devices. A product developer that seeks to build a flexible product must consider which of these technologies provides the capabilities for the necessary product features. A newly suggested method to meet this requirement is the offering of flexible development kits, such as FleXform, that a product designer can use as a basic development platform. Some product designers will have the ability to assemble the necessary printed capability and development kits. Others will utilize organizations offering integration services to realize the product designers' vision.

IX. FHS APPLICATIONS

An FHS approach allows the ability to deliver a spatially distributed response to signals from spatially distributed sensing. As a result, many applications once too cumbersome or costly to realize become accessible in an appealing format. With the ability to deploy sensors integrated with adequate processing and communication comes the opportunity for truly ubiquitous applications—smart surfaces, closed-loop diagnostics and therapeutics, and real-time monitoring of individuals or structures. Once a controller with response or communication capability is integrated in compatible formats, many options become available.

As indicated in the detailed examples, the option for disposable devices or even simply the sensing aspects of a device open many medical applications where either the sensing system is customized for an individual or situation or where disposability is desired for infection control. Reusable controller modules may offer advantages because that is where much of the value is presently located in the device. However as the processors become easier and more economical to build, the entire device may become disposable. In particular, it is now practical to make easily fitted and comfortable elements of the much-vaunted body-area network (BAN) concepts discussed some years ago [11].

The use of the FHS approach addresses many of the challenges which seemed to impede the progress of the BAN idea. Now with flexible rechargeable batteries and the ability to make reasonably efficient contactless recharging systems, a long-term wearable patch is closer to reality.

Beyond human health applications, health surveillance, and stress monitoring, many other valuable applications can be targeted with FHS solutions. Targets for sensing, including labeling, packaging, mechanical, and civil engineering structures, airframe components, remote weight and performance monitoring in commerce, were all enabled with the minimally intrusive format that FHS provides.

Additional opportunities include a broader application of display and other communication modes. These are all generally computing intensive, either for interpreting signals or for the simple control of even a low information content display. The impediment has been the need to accommodate and power a conventional IC with all of its incompatibilities. Very often, the additional bulk of accommodating a display and its driver has limited the realization of many otherwise compact devices. With the FHS approach, these spatial limitations can be overcome.

Applications in the packaging industry have been slow to be realized because again, there is the perceived need to accommodate thick and heavy rigid conventional components for sufficient computing power to provide an appealing smart package suitable for tamper resistance and detection. Likewise, food chain security has rested on discrete, large, and cumbersome devices often not truly integrated with the packaging and, thus, vulnerable to misinterpretation. The integration of sense and control with an FHS is an avenue of great promise in smart packaging.

X. SUMMARY

Hybrid electronics are now becoming feasible. The integration of PFE and conventional Si with the "print what you can and add silicon where you must" establishes a viable manufacturing approach for flexible and conformal electronic applications. The welcome news is that FHS technology, using SoP, has the benefits of printed and flexible electronics, enabling integrated systems, which are thinner, lighter weight, and more durable. Better conformance may have finally arrived—and is no longer "just around the corner." ■

REFERENCES

[1] W. Christiaens, T. Torfs, W. Huwel, C. Van Hoof, and J. Vanfleteren, "3D integration of ultra-thin functional devices inside standard multilayer flex laminates," presented at the Eur. Microelectron. Packag. Conf., Rimini, Italy, Jun. 15–18, 2009.

[2] Burghartz, "Ultra-thin chips and related applications, A new paradigm in silicon technology *Proc. Eur. Solid State Device Res. Conf.*, 2009, pp. 29–36.

[3] R. Chaney and D. Hackler, "Performance electronics integration in flexible technology," presented at the GOMAC, Reno, NV, Mar. 22–25, 2010. [Online]. Available: http://www.americansemi.com/GOMAC2010_28-18.pdf

[4] D. Hackler, "High performance electronics integration in flexible technology," presented at the 2011FLEX Flexible Electron. Displays Conf., Phoenix, AZ, USA, Feb. 2011. [Online]. Available: http://www.americansemi.com/AmericanSemiconductor_2011FLEX.pdf

[5] D. Hackler, "Flexible hybrid system integration: Combining printed sensors with flexible ICs," presented at the IDTechEX, Printed Electronics USA, Santa Clara, CA, USA, 2014.

[6] D. Hackler, "FleX silicon-on-polymer flexible single crystalline ICs from commercial foundry processes for flexible hybrid systems," presented at the LOPEC 6th Int. Exhibit. Conf., Munich, Germany, 2014.

[7] D. Hackler, "FleX silicon-on-polymer technology," presented at the American Semiconductor Inc., Phoenix, AZ, Canada. [Online]. Available: http://www.americansemi.com/FleX.html.

[8] K. Ronka, "Assembly and in-mould-integration process development for flexible systems based on chips-on-roll," presented at the LOPEC 6th Int. Exhibi. Conf., Munich, Germany, 2014.

[9] M. Clausen, "Developing the supply-chain for NFC enabled flexible electronics," presented at the LOPEC 6th Int. Exhibit. Conf., Munich, Germany, 2014.

[10] M. Koetse, "Stretching the limits of electronics," presented at the LOPEC 6th Int. Exhibit. Conf., Munich, Germany, 2014.

[11] S. Ullah, H. Higgins, B. Braem, B. Latre, C. Blondia, I. Moerman, S. Saleem, Z. Rahman, and K. Kwak, "A comprehensive survey of wireless body area networks," *J. Med. Syst.*, vol. 36, no. 3, pp. 1065–1094, Jun. 2012.

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