FACULTY OF INFORMATION TECHNOLOGY AND ELECTRICAL ENGINEERING

521402S Telecommunications Circuit Design

Simulation exercise #02

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7 May 2023

1 BEHAVIORAL MODEL

In this part, the NMOS is represented by a behavioral model, Figure 1, and results are analyzed.

From the previous exercise, a bias voltage (Vgs) of 0.7V to 1V is good to get a high and stable gm. In this exercise, Vgs was selected to be 0.9 V. This resulted in g_{m0} and C_{gs0} of 500 µS and 0.57 fF. Thus, the multiplier number required to get total g_m of 5 mS is 10 (.i.e 10 NMOS devices in parallel) which results in a total C_{gs} of 5.7 fF.

Simulating the schematic and with few trails, the required excess capacitance to set Zin to 50 Ω is C_{ex} = 0.3 pF. To cancel the imaginary part of Z_{in}, L_g is set to 17.7 nH.

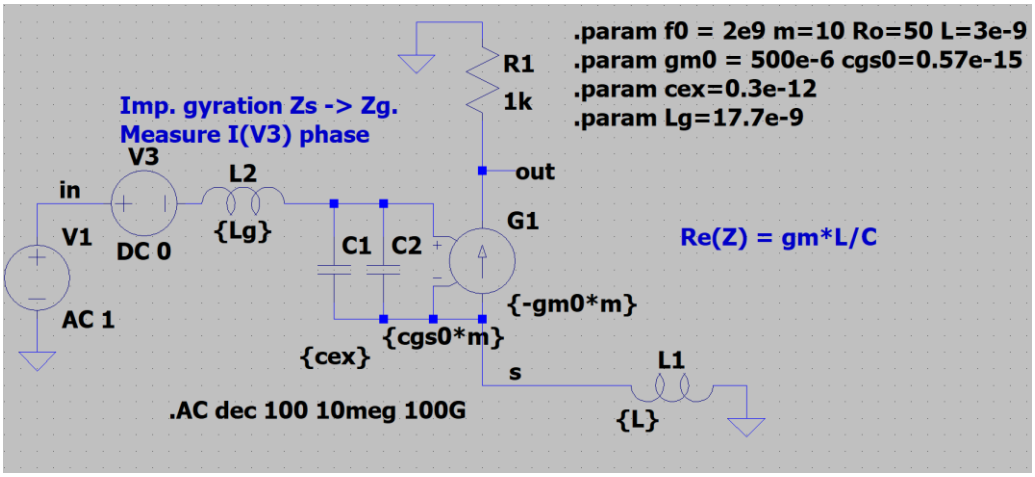

Figure 1. The dimensioned "e2_lna_behav.asc" schematic file

The resulting Z_{in} and Y_{in} are shown in Figure 2 below.

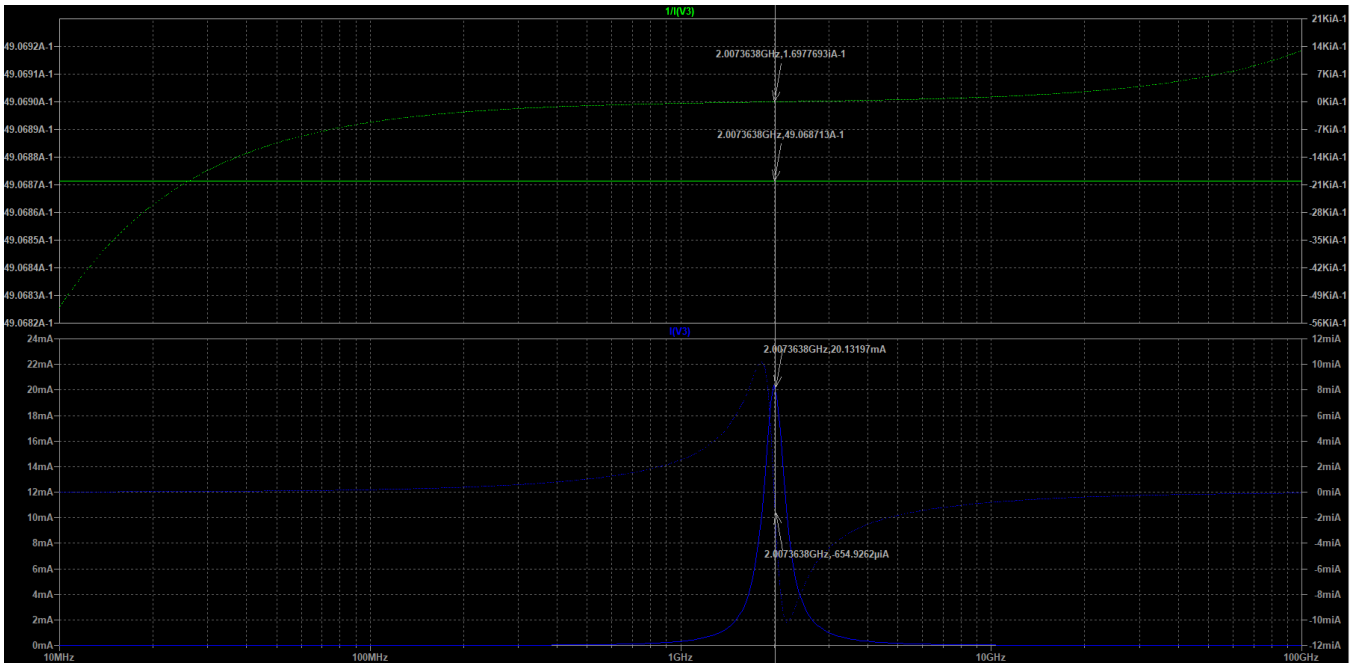

Figure 2. Z_{in} and Y_{in} of the behavioral model

2 REAL NMOS MODEL

In this part, a real NMOS device is used with the provided 45nm library.

The schematic with the NMOS device, Figure 3, was dimensioned to replicate the performance of the behavioral model. Figure 4 shows the S11 and S21 plots. No tuning was needed to set the minimum S11 to the frequency range. At 2GHz, S11 is -13.52 dB and considering -8dB the level to set the bandwidth, we have about 232 MHz of bandwidth.

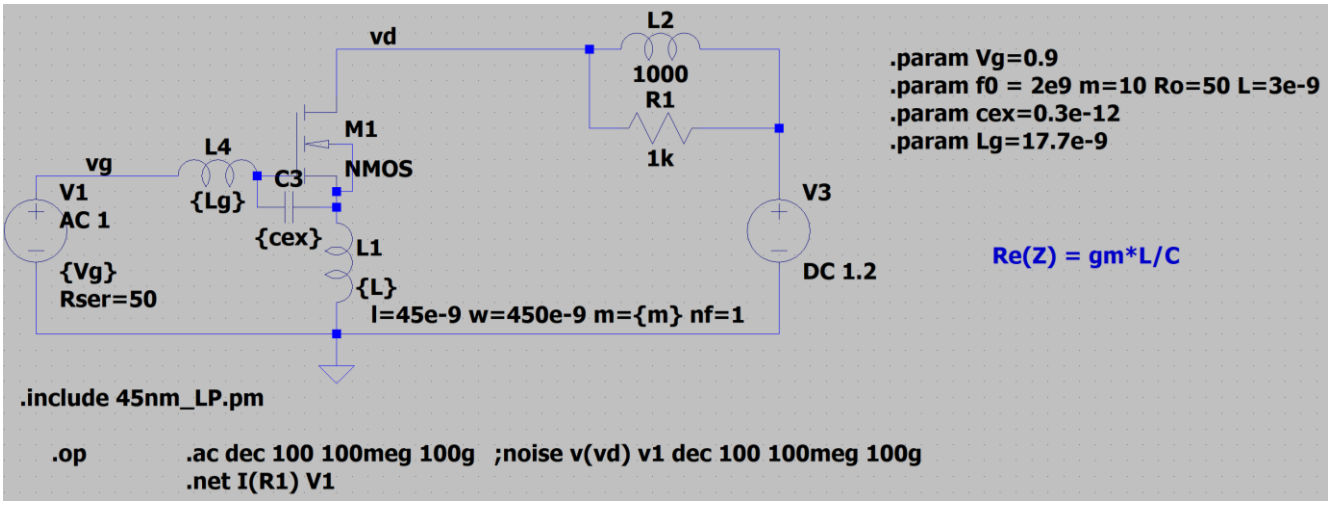

Figure 3. The dimensioned “e2_lna_mos.asc” file

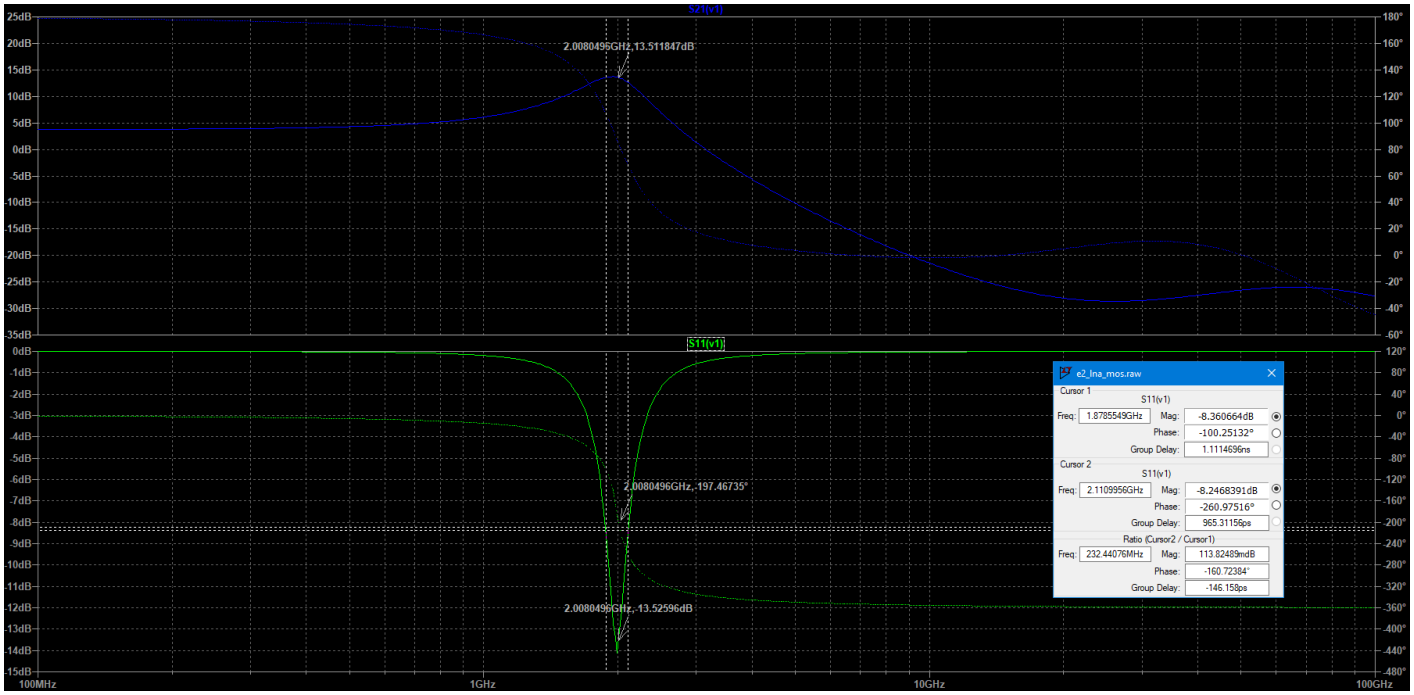

Figure 4. S11 and S21 results of the AC analysis

3 NOISE ANALYSIS

With noise analysis enabled and the source resistor replaced with an actual resistor, Figure 5, and the different noise contributions are shown in Figure 6. At lower frequencies, the transistor's 1/f noise dominates the output noise. Around the operating band (1.5 GHz – 3 GHz), the source termination resistor Rs drastically dominates the output noise especially around 2GHz where the transistor contribution reduces a bit. At higher frequencies, the output noise is dominated by the output termination resistor R1.

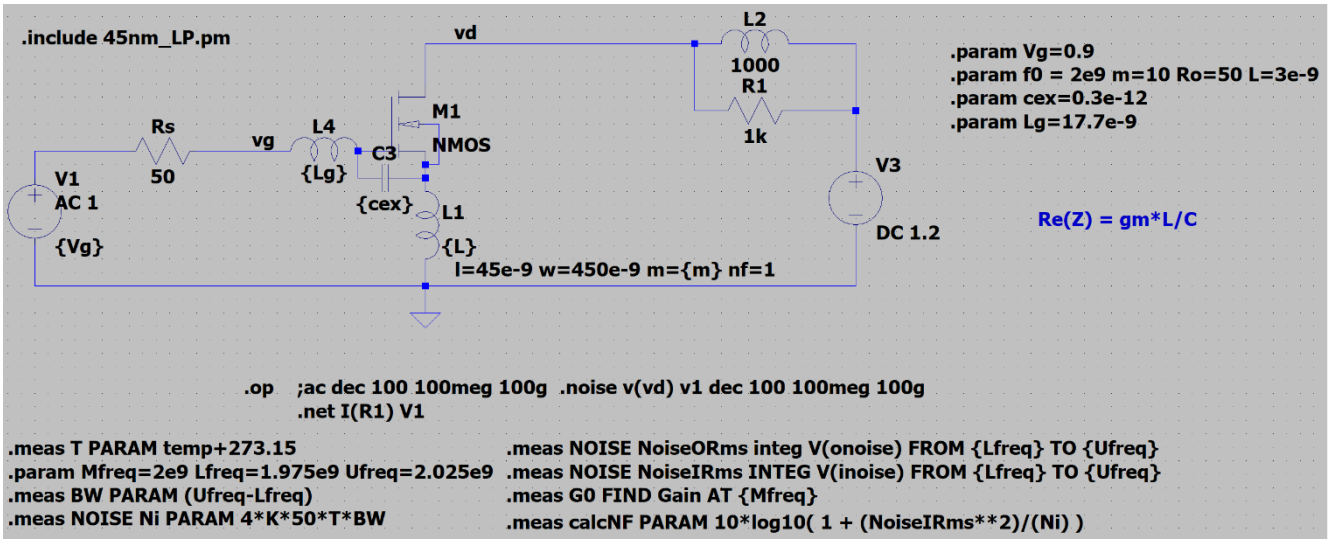

Figure 5. The modified "e2_lna_mos.asc" schematic for noise analysis

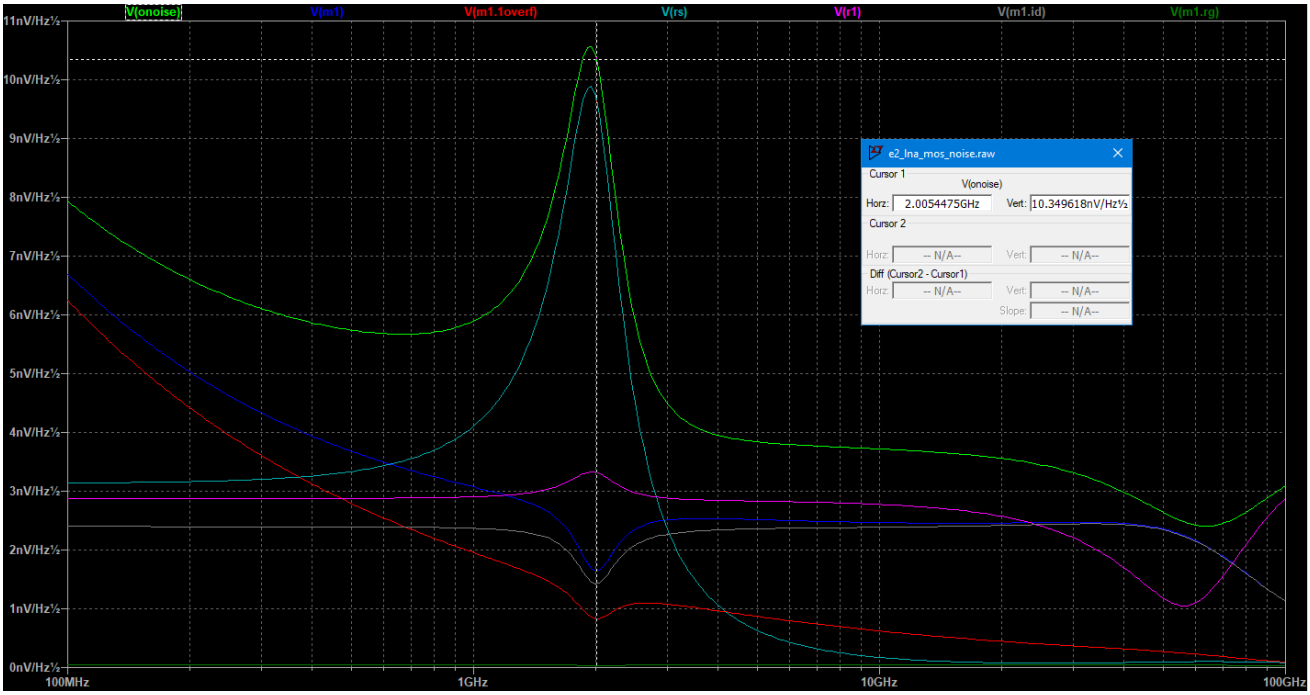

Figure 6. Noise contributions

The achieved noise Figure is high due to the lossy and noisy termination at the input of the LNA (source resistance). Using the measurement function, the noise figure could be calculated over the band of interest (50 MHz around 2 GHz). The NF is calculated by integrating the input referred noise V(inoise) over the band and using the following equations.

$$F = 1 + \frac{N_i}{N_{amp}} \; ; N_{amp} = KTB \; ; NF = 10\log_{10}(F)$$

Using the spice log, the achieved NF is 3.31742 dB which a bit high for an LNA (usually for LNAs, NF < 2 dB). The design could be improved by increasing the value of the degeneration inductor L and reducing the excess capacitance to maintain the input matching.