FACULTY OF INFORMATION TECHNOLOGY AND ELECTRICAL ENGINEERING
MASTER'S PROGRAMME IN WIRELESS COMMUNICATIONS ENGINEERING

521326S Radio Engineering 1
Design Exercise Report

Group 15

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LIST of FIGURES

LIST of SYMBOLS and ABBREVIATIONS

βl	Electrical length
Γ	Reflection coefficient
f_T	Transit frequency
Q	Quiescent point
S	Scattering parameter
ADS	Advanced Design System
dB	Decibels (relative to a 1 Watt)
dBm	Decibels (relative to a 1 mWatt)
NF	Noise Figure
OC	Open Circuit
SC	Short Circuit
TL	Transmission Line

1 Biasing parameters

In the real amplifier, the nonlinear model is used. This model includes the different effects of the transistor and in order to simplify the design and use the s-parameters model, we have to make sure that the operating point of both models match.

The s-parameters model is valid when the transistor is operating at the quiescent point of Q ($V_{CE} = 8V; I_C = 2mA$). Thus, the nonlinear model has to be biased to operate at the same point. Figure 1.1 shows the circuit used in the *BiasSetup* schematic file to determine the base voltage and current used to reach the same operating point. The base current I_{BB} is swept linearly and the *BiasSetup.dds* file presents the results as shown in.

As highlighted in Figure 1.2, sweeping I_{BB} with $V_{CE} = 8V$ shows the nonlinear model needs $I_{BB} = 19.5\mu A$ for $I_{CE} \approx 2\mu A$, which corresponds to $V_{BE} = 774.6mVV$ as presented also in the current and voltage annotations of Figure 1.1.

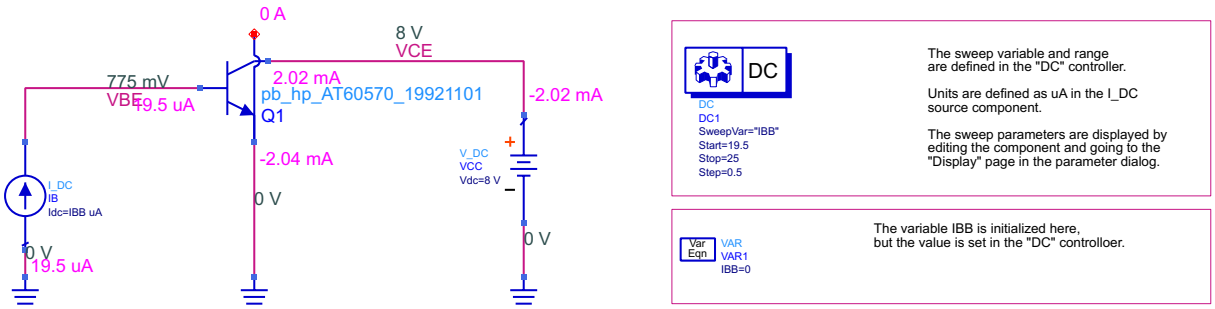


Figure 1.1: Biasing circuitry with voltages and currents annotation

IBB	VBE	VCC.i
15.000	767.0 mV	-1.563 mA
15.500	767.9 mV	-1.615 mA
16.000	768.8 mV	-1.666 mA
16.500	769.7 mV	-1.718 mA
17.000	770.6 mV	-1.769 mA
17.500	771.4 mV	-1.820 mA
18.000	772.2 mV	-1.871 mA
18.500	773.0 mV	-1.923 mA
19.000	773.8 mV	-1.974 mA
19.500	774.6 mV	-2.025 mA
20.000	775.3 mV	-2.076 mA
20.500	776.0 mV	-2.126 mA
21.000	776.7 mV	-2.177 mA
21.500	777.4 mV	-2.228 mA
22.000	778.1 mV	-2.279 mA
22.500	778.8 mV	-2.329 mA
23.000	779.4 mV	-2.380 mA
23.500	780.1 mV	-2.430 mA
24.000	780.7 mV	-2.481 mA
24.500	781.3 mV	-2.531 mA
25.000	781.9 mV	-2.581 mA

Sweeping IBB with VCE=8V shows the model needs IBB=19.5uA for ICE=2mA, corresponding to VBE=774.6mV.

Figure 1.2: Base current I_{BB} sweeping results

2 Model verification

After determining the bias requirements to ensure the same operating point, we shall verify that the two models match each other and there's no mismatches between their responses. Figure 2.1 shows the circuit used in the *ModelVerif* schematic files to determine the s-parameters responses of each model after changing the operating point of the nonlinear model to the proper point found previously of Q ($V_{BE} = 774.6mV; V_{CE} = 8V; I_C = 2mA$).

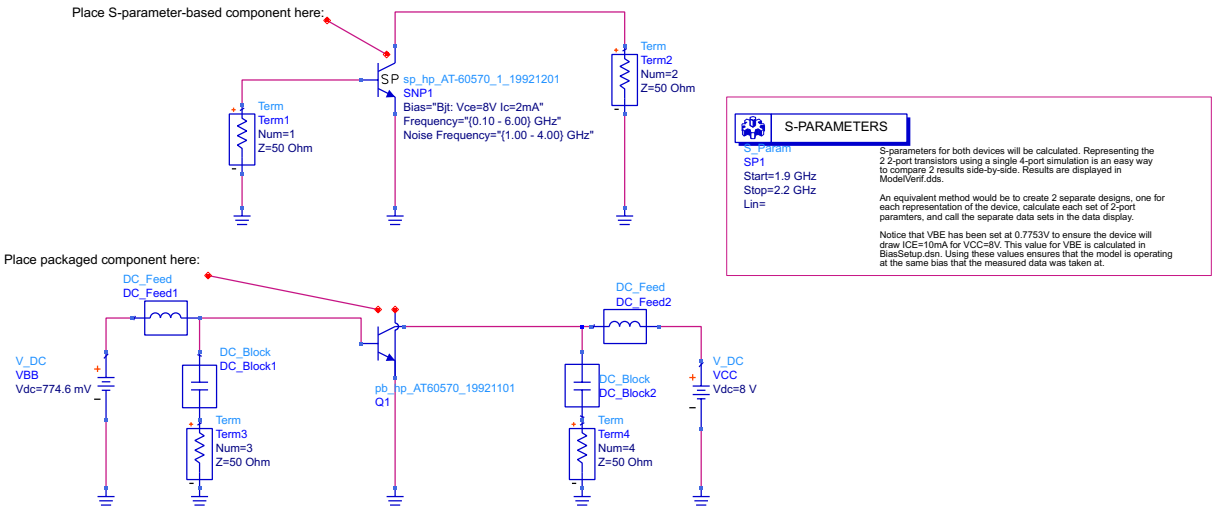


Figure 2.1: Model verification circuits

The results of the simulation are presented in the *ModelVerif.dds* file and they are shown in Figure 2.2. The comparison has been performed over the band [1.9 GHz - 2.2 GHz] which covers the intended operation bandwidth of the amplifier. There is a slight difference between the S-parameters of this difference can be neglected as it's very small (less than 1.5 dB in S_{21})

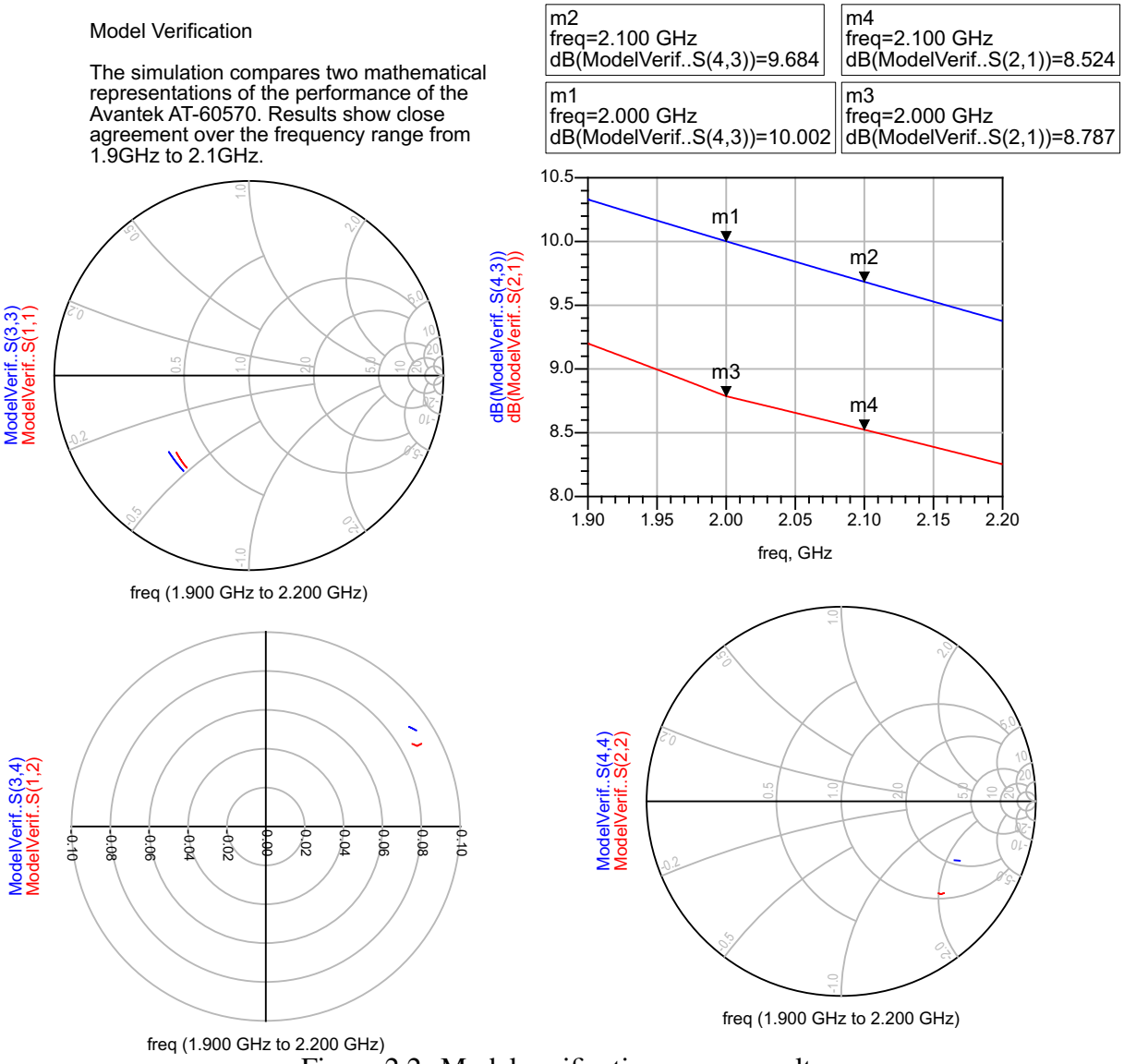


Figure 2.2: Model verification sweep results

3 Biasing Circuit

After verifying that the nonlinear model matches the s-parameters one, we design the biasing circuit. Here, the *Bias_Network* schematic file has been used and Figure 3.1 shows the circuit used in the file. The file is used with OPTIM and GOAL blocks in which ADS tries to optimizes the values of bias resistors RB1 and RB2 along with collector resistor RC1 to reach the targets set in Goal blocks within the defined margins on V_{CE} and I_{CE}. The 10V supply is used to ensure 8V across the transistor and leave headroom for the voltage drop across the drain resistor. Figure 3.1 shows the targets set in Goal block and their perspective margin. Figure 3.2 shows the ADS optimizer results and the number of iterations performed to converge to values used in Figure 3.1. Also, Figure 3.3 shows the results of the optimizer presented in the *Bias_Network.dds* file.

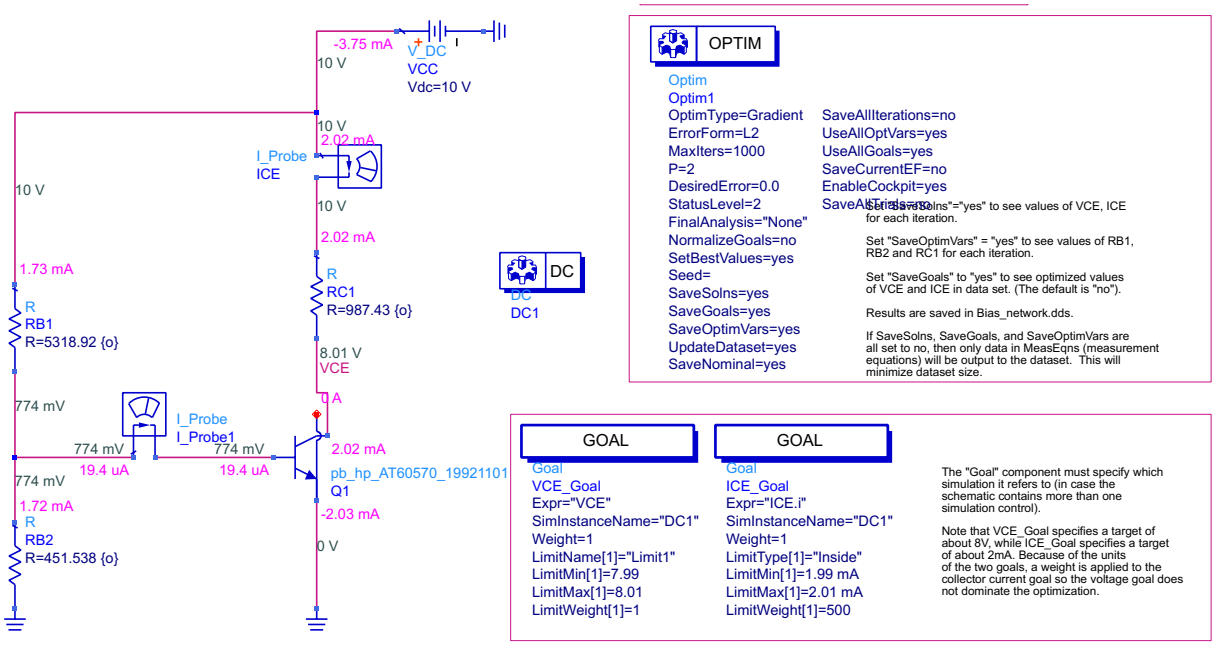


Figure 3.1: Bias network simulation circuit

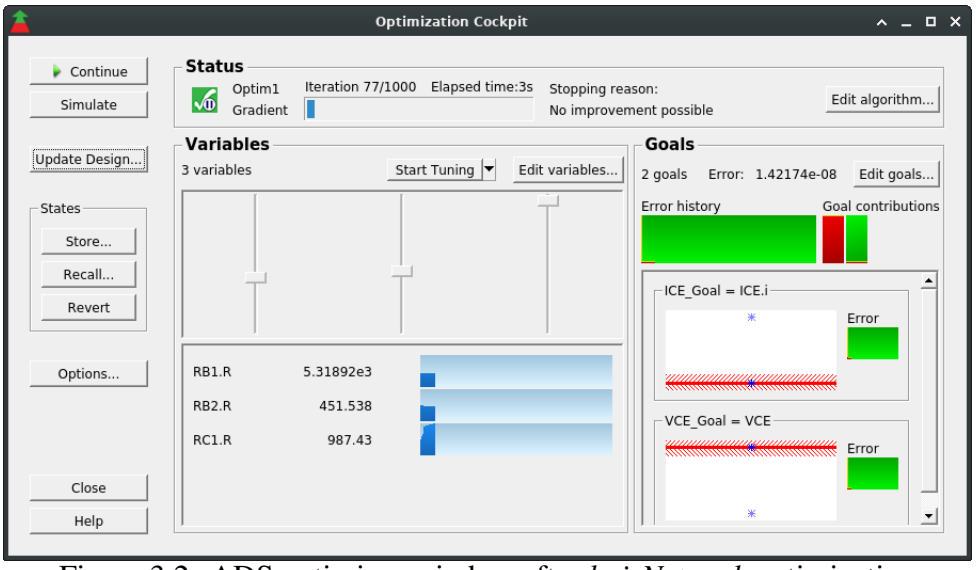


Figure 3.2: ADS optimizer window after *baisNetwork* optimization

optIter	VCE[0]	ICE.i[0]
0	3.922	0.012
77	8.010	0.002

Setting "SaveGoals=yes" means the expression in each goal is written to the dataset.

optIter	VCE_Goal[0]	ICE_Goal[0]
0	3.922	0.012
77	8.010	0.002

Setting "SaveSolns=yes" means results are written to the dataset.

optIter	OPTIM.RB1.R	OPTIM.RC1.R	OPTIM.RB2.R
0	5000.000	500.000	500.000
77	5318.925	987.430	451.538

Setting "SaveOptimVars=yes" means values for RB1, RB2 and RC1 are written to the dataset for each iteration.

OPTSOLNVALS.RC1.R	OPTSOLNVALS.RB2.R	OPTSOLNVALS.RB1.R
987.430	451.538	5318.925

Check "Set best values for parent optimization" to pass best optimized resistor values to next optimization.

Figure 3.3: ADS optimizer results

4 Noise performance

After verifying that the nonlinear and s-parameters model match each other and determining the bias circuit for the non linear model, we shall move on to use the s-parameters model in the design. The amplifier is intended to be a low noise amplifier in the required band thus the noise performance and characteristics of the transistor are examined here.

The noise performance of the transistor is examined over the noise frequency available in the s-parameters model over [1 GHz - 4 GHz]. Figure 4.1 shows the circuit used in the *SparamNoise* schematic file to study the noise performance of the transistor.

The noise circles for the used transistor are plotted for the values of 1.5 dB, 2 dB, 2.5 dB, 3 dB, and 3.5 dB, as shown in Figure 4.2, at the frequency of 2 GHz (configured by the marker m1). The reflections coefficients of the transistor $S11$ and $S22$ along with the optimum reflection coefficients at the input S_{opt} are shown in Figure 4.3, and from the marker m2, for minimum noise figure, the source reflection coefficient that should be presented to the transistor is $\Gamma_s = S_{opt}(f = 2GHz) = 0.44\angle 98.00°$. The forward gain $S21[dB]$ and minimum noise figure $NFmin[dB]$ and effective noise resistance R_n are shown in Figure 4.4.

At 2 GHz, the transistor has a minimum noise figure of $NF_{min} = 1.8dB$ (lowest NF that can be achieved), thus the input matching should provide minimum deterioration of the noise figure in order to meet the requirements on the noise figure of the hole amplifier. The maximum available gain of $G_a = |S_{21}| = 8.787dB$ and hence the output matching should provide at least 0.213 dB to achieve the 10 dB targeted gain.

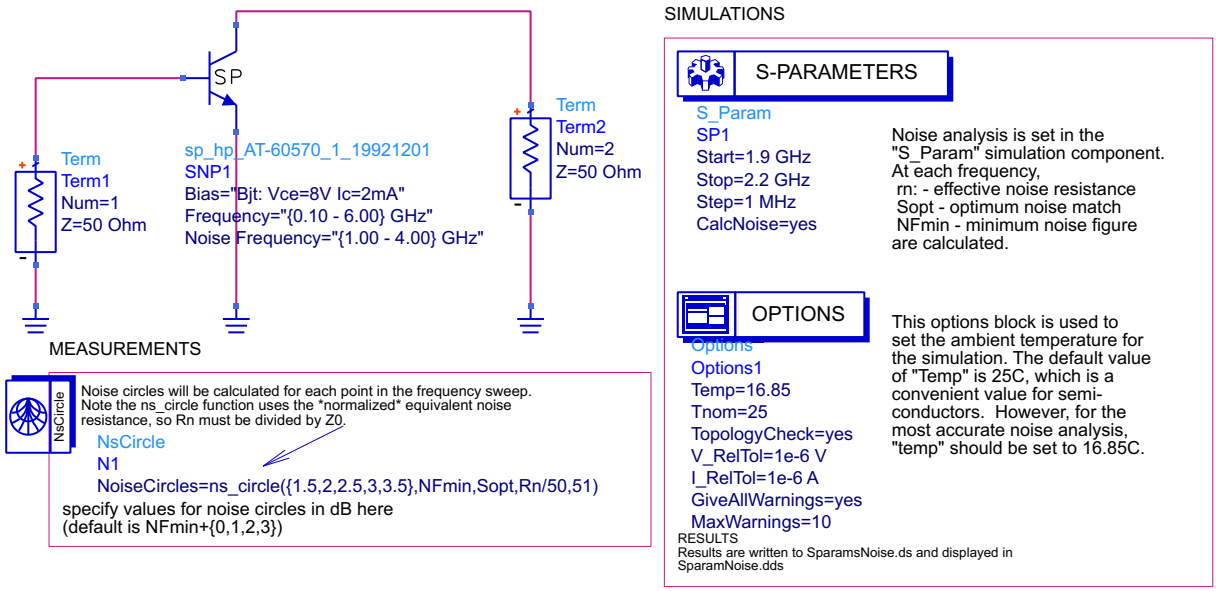


Figure 4.1: Noise performance simulation circuit

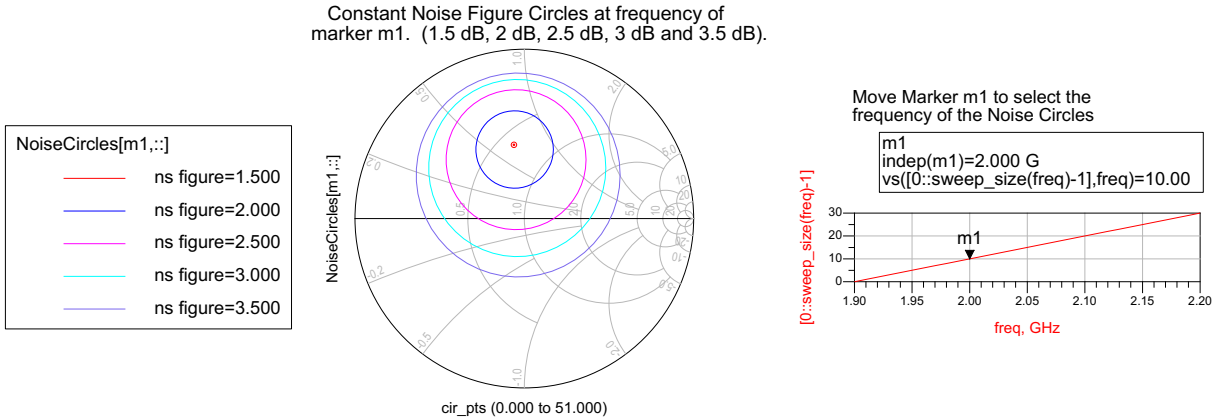


Figure 4.2: Noise figure circles

S11, S22 and Sopt (optimum source match needed to achieve minimum noise figure).

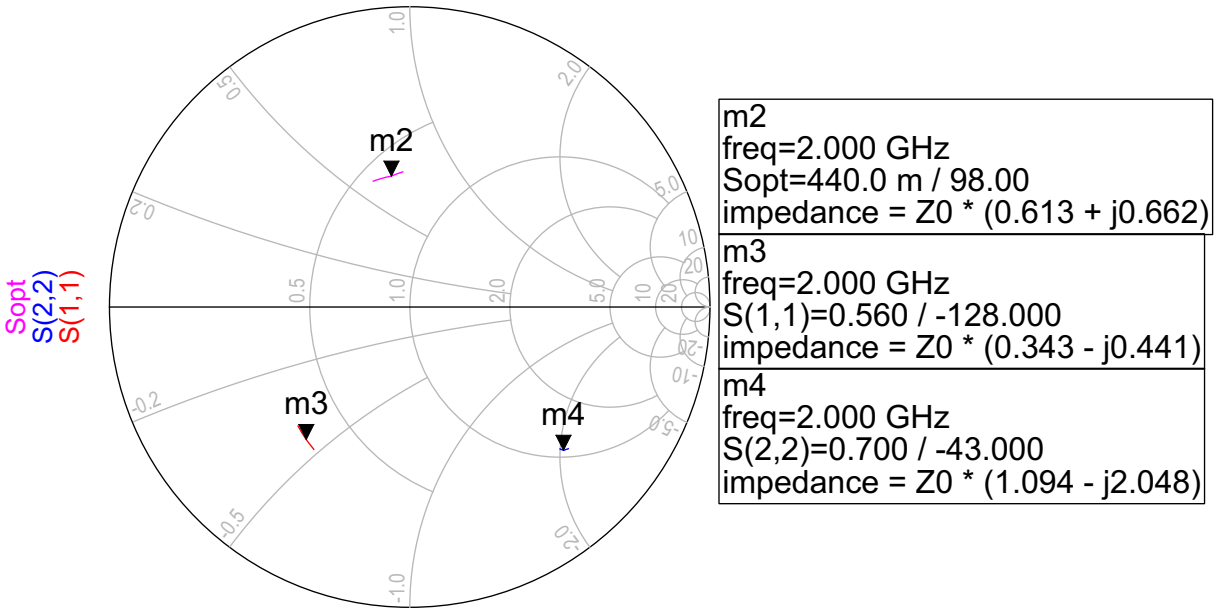


Figure 4.3: S_{11}, S_{22}, and S_{opt} reflection coefficients

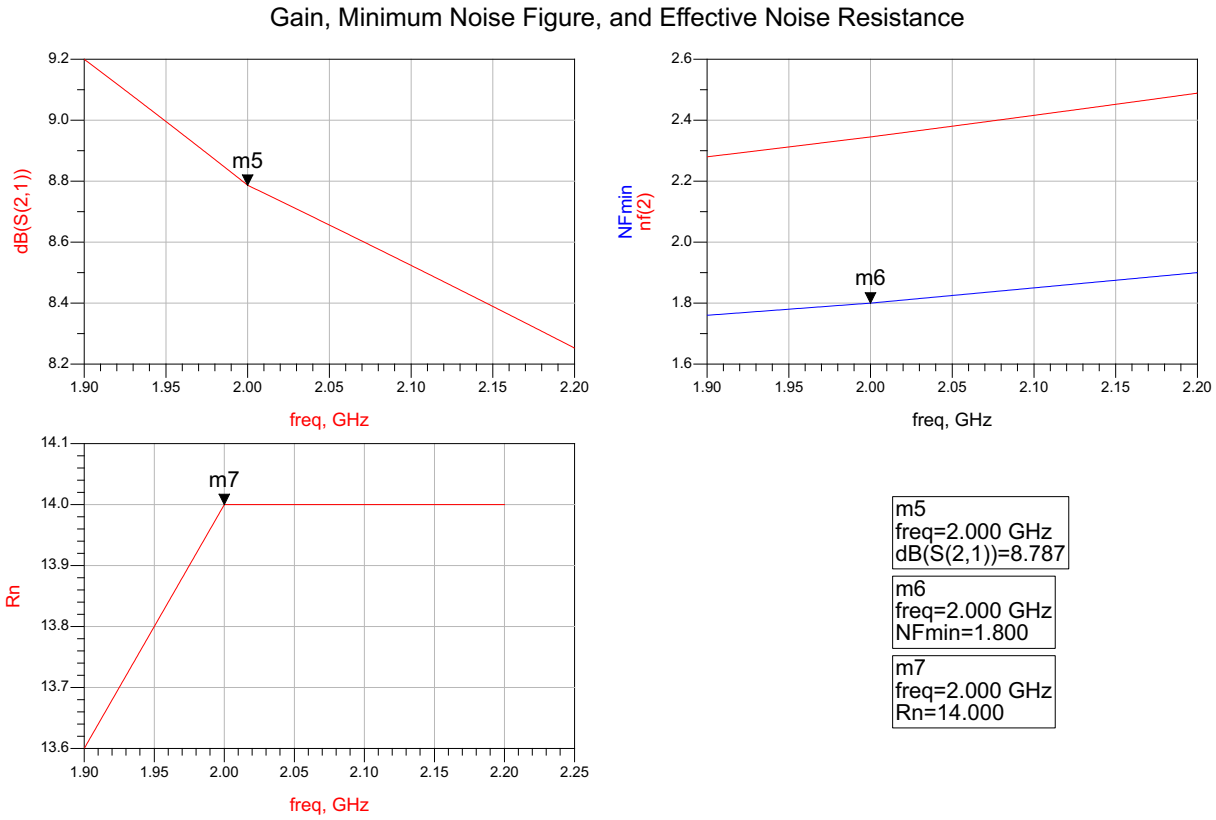


Figure 4.4: Gain, Minimum Noise Figure, and Effective Noise Resistance

5 Stability metrics

5.1 Studying the stability of the transistor

The *Stability* schematic file is used to study the stability of the transistor. It contains the circuit shown in Figure 5.1 in which the stability circuit, consisting of R1 and L1, is deactivated.

The stability circle of the output is shown in Figure 5.2 along with the stability metrics μ, K, and B_1. Since $\mu < 1$, $B_1 > 0$, and $K < 1$, the transistor is conditionally stable over the band of operation.

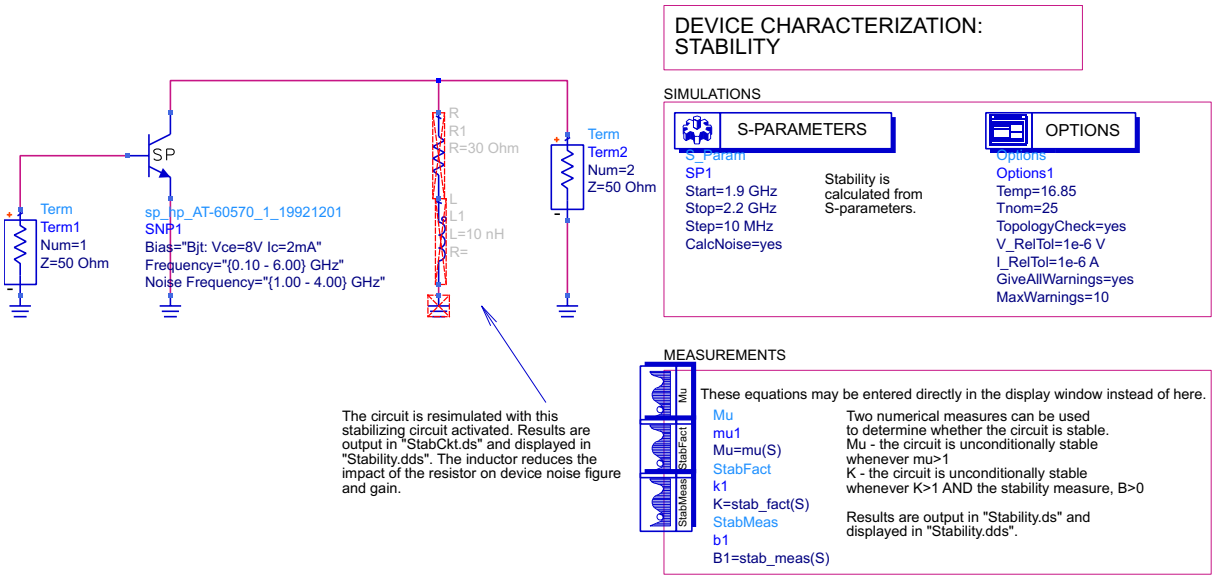
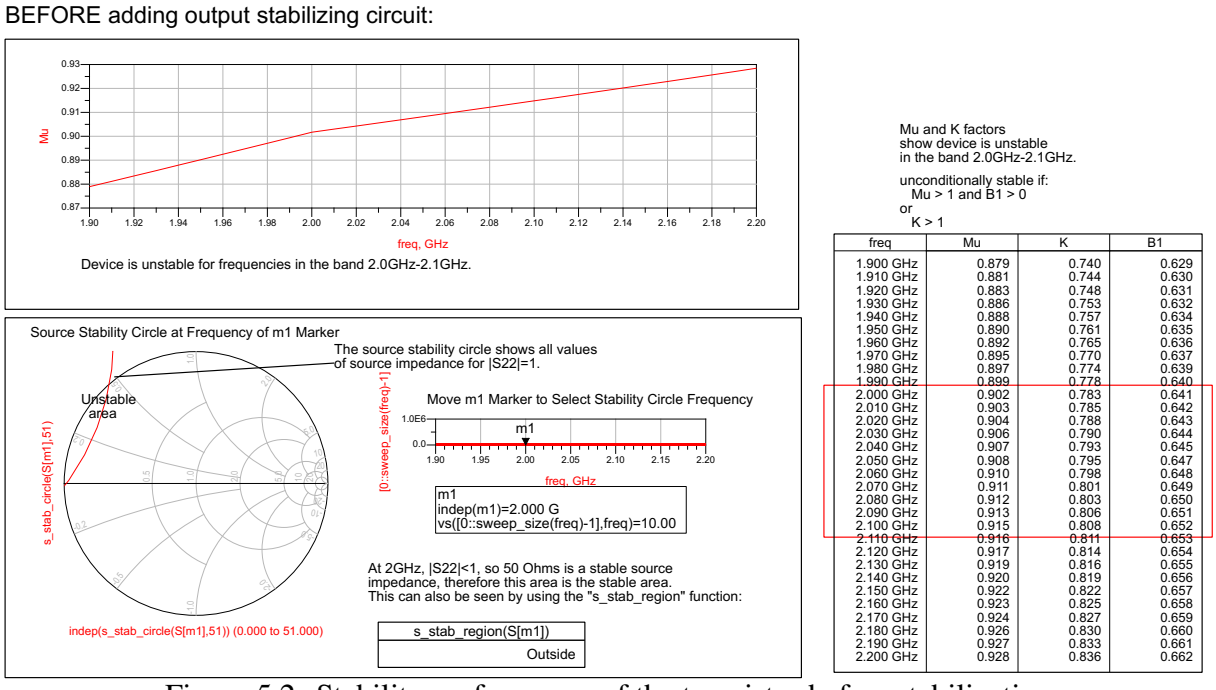


Figure 5.1: Circuit to study the stability of the transistor

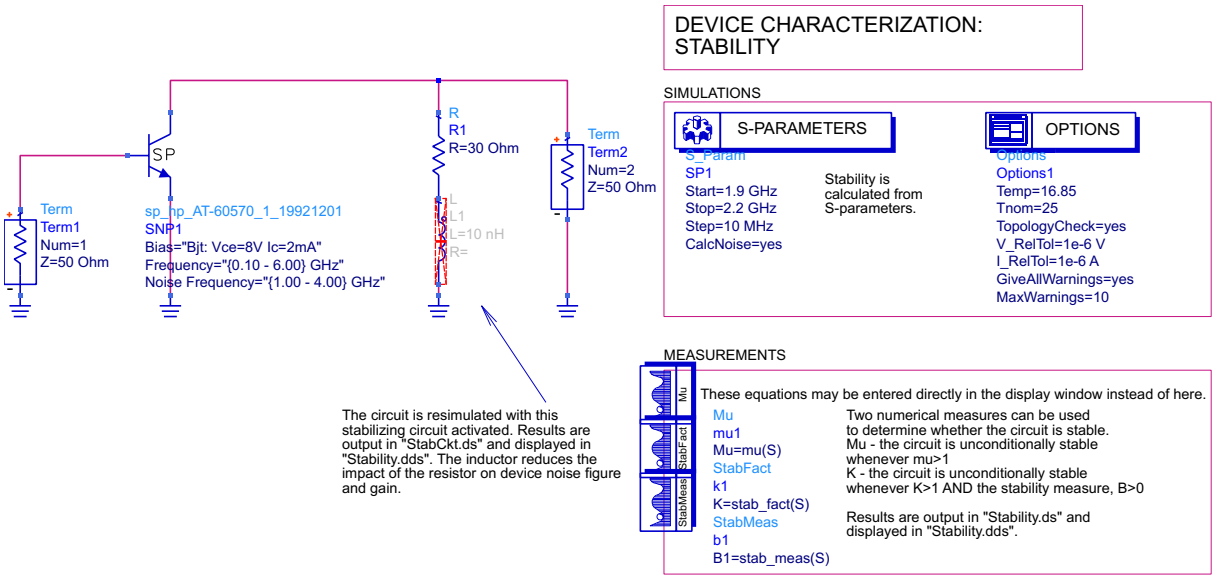


freq	Mu	K	B1
1.900 GHz	0.879	0.740	0.629
1.910 GHz	0.881	0.744	0.630
1.920 GHz	0.883	0.748	0.631
1.930 GHz	0.886	0.753	0.632
1.940 GHz	0.888	0.757	0.634
1.950 GHz	0.890	0.761	0.635
1.960 GHz	0.892	0.765	0.636
1.970 GHz	0.895	0.770	0.637
1.980 GHz	0.897	0.774	0.639
1.990 GHz	0.899	0.778	0.640
2.000 GHz	0.902	0.783	0.641
2.010 GHz	0.903	0.785	0.642
2.020 GHz	0.904	0.788	0.643
2.030 GHz	0.906	0.790	0.644
2.040 GHz	0.907	0.793	0.645
2.050 GHz	0.908	0.795	0.647
2.060 GHz	0.910	0.798	0.648
2.070 GHz	0.911	0.801	0.649
2.080 GHz	0.912	0.803	0.650
2.090 GHz	0.913	0.806	0.651
2.100 GHz	0.915	0.808	0.652
2.110 GHz	0.916	0.811	0.653
2.120 GHz	0.917	0.814	0.654
2.130 GHz	0.919	0.816	0.655
2.140 GHz	0.920	0.819	0.656
2.150 GHz	0.922	0.822	0.657
2.160 GHz	0.923	0.825	0.658
2.170 GHz	0.924	0.827	0.659
2.180 GHz	0.926	0.830	0.660
2.190 GHz	0.927	0.833	0.661
2.200 GHz	0.928	0.836	0.662

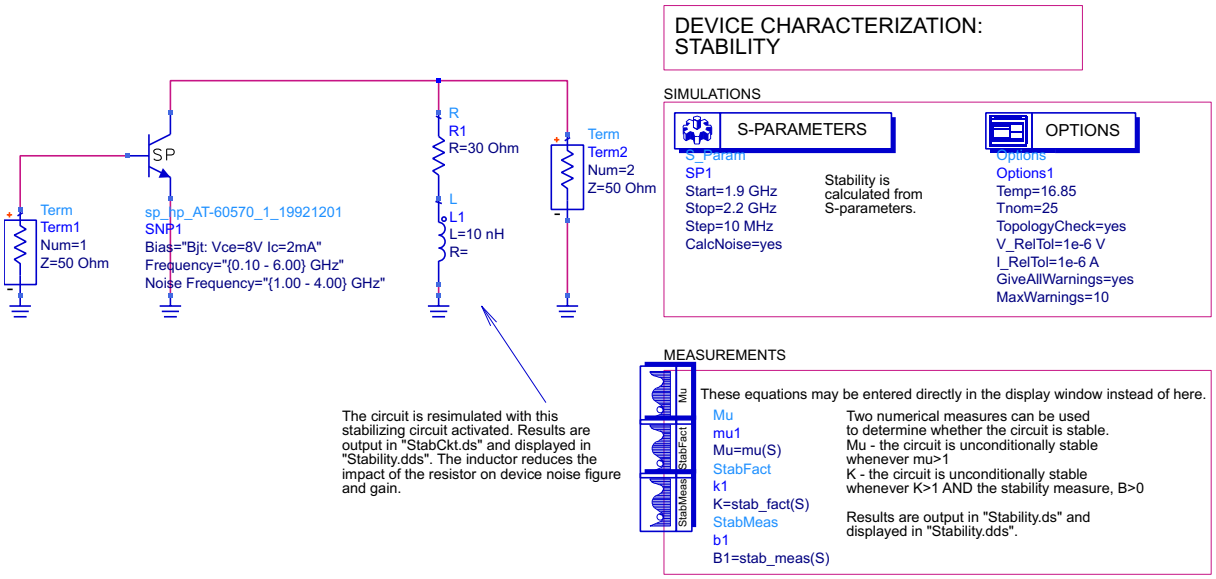
Figure 5.2: Stability performance of the transistor before stabilization

5.2 Stabilizing the transistor

To stabilize the transistor, the stabilization circuit is activated by enabling the resistor R1 and shorting the inductor L1, as shown in Figure 5.3a. Since R1 is a shunt resistor at the output, its value could be determined based on the conductance circle that is tangent to output stability circle[1, p226]. After testing a couple of values for R1, we choose the value to be 30Ω, which resulted in the stability circuit that is out of the smith chart, as shown in Figure 5.4. In addition, unshorting the inductor L1, as shown in Figure 5.3b, reduces the noise figure deterioration due to the resistor R1 and results in a noise figure that is closer to the transistor's one as shown in Figure 5.4.



(a) L1 shorted



(b) L1 unshorted

Figure 5.3: Stabilizing the transistor with the resistor R1

The stability circuit is considered part of the transistor when designing the amplifier. Thus, the optimum reflection coefficient of the source is changed and with the values used previously in the stability circuit, it becomes $\Gamma_s = S_{opt}(f = 2GHz) = 0.444\angle 98.626°$, as presented in Figure 5.4.

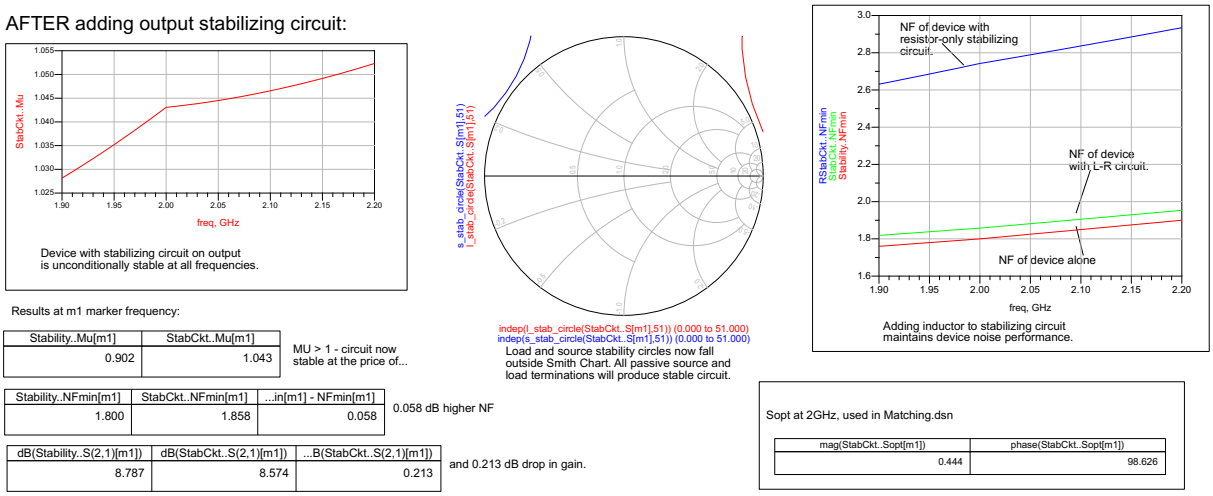


Figure 5.4: Stability performance of the transistor after stabilization

6 Input and Output matching

6.1 Input matching

The input is matched to obtain minimum noise figure. Thus, $\Gamma_{in} = S^*_{opt} = 0.444\angle{-98.626°}$. The input matching calculations and Simth chart are presented in Appendix A.1.

The *Match1* schematic file is used to determine the value of L_{in}, as shown in Figure 6.1. The simulation results, Figure 6.2, shows that the approximate suitable value for the inductor to lie in the unity resistance circle is $L_{in} = 3.2nH$.

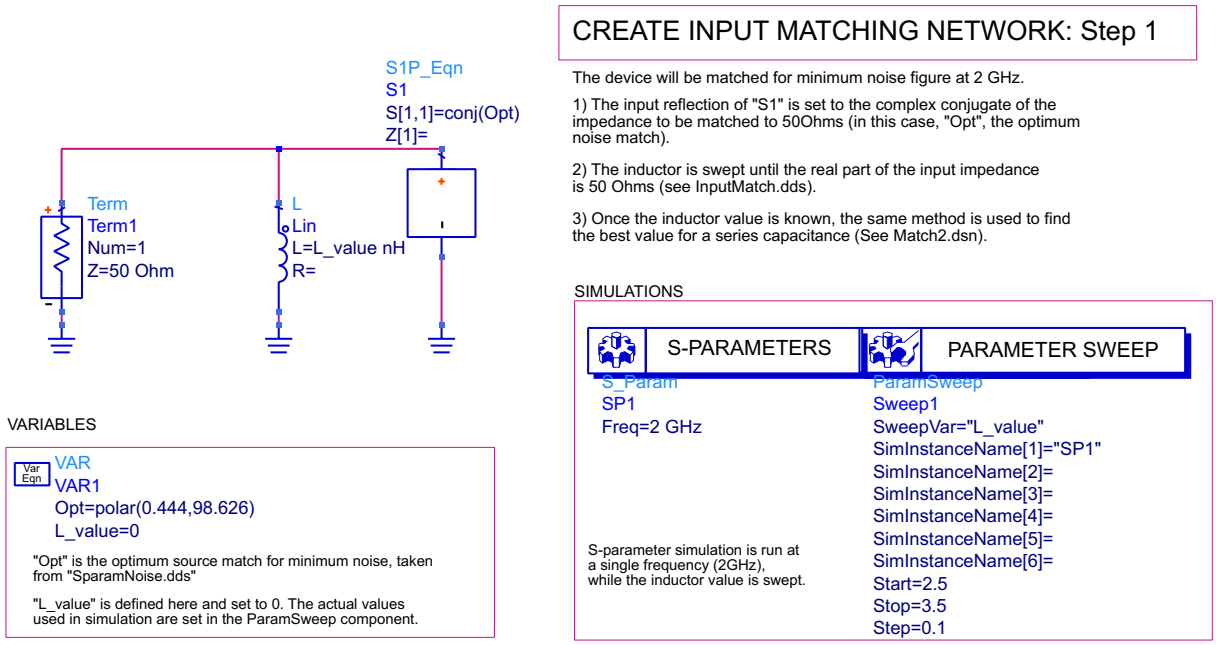


Figure 6.1: Simulation circuit for finding the value of the input matching inductor

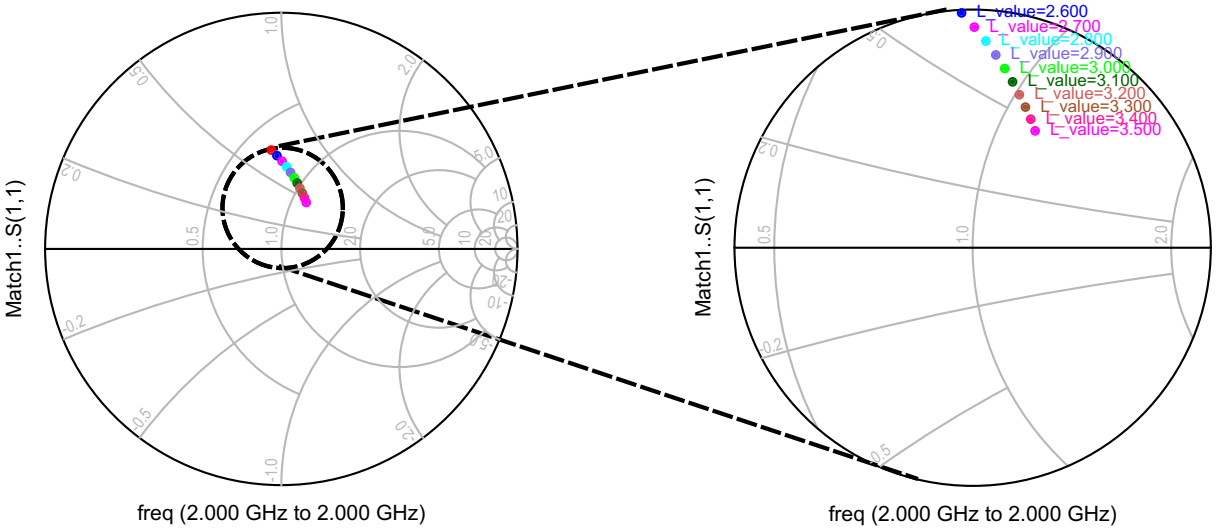


Figure 6.2: The value of the input matching inductor

The *Match2* schematic file is used to determine the value of C_{in}, as shown in Figure 6.3. The simulation results, Figure 6.4, shows that the approximate suitable value for the capacitor to lie in the origin of the smith chart is $C_{in} = 2.8pF$.

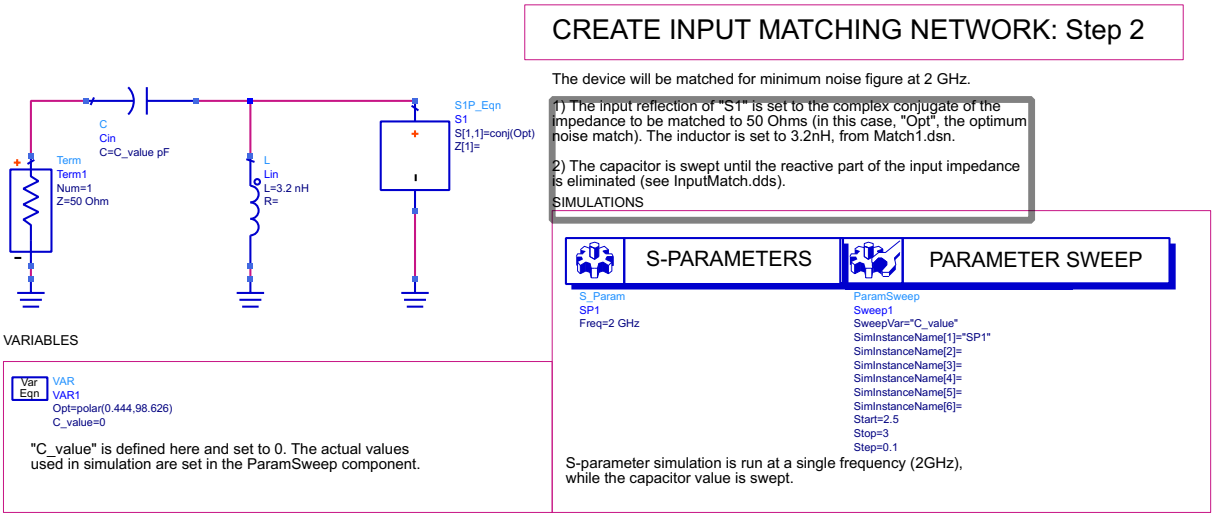


Figure 6.3: Simulation circuit for finding the value of the input matching capacitor

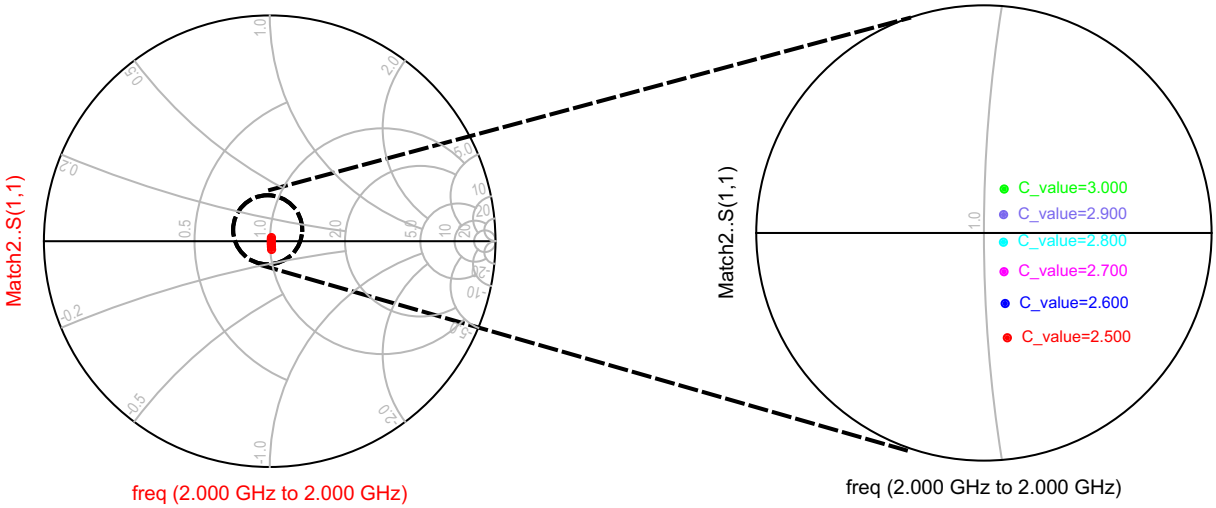


Figure 6.4: The value of the input matching capacitor

6.2 Output matching

The output is matched to obtain maximum gain. Thus, $\Gamma_L = \Gamma^*_{out}$. The output matching calculations and Smith chart are presented in Appendix A.2.

The *Match3* schematic file is used to determine the value of L_{out}, as shown in Figure 6.5. The simulation results, Figure 6.6, shows that the approximate suitable value for the inductor to lie in the unity resistance circle is $L_{out} = 6.9nH$.

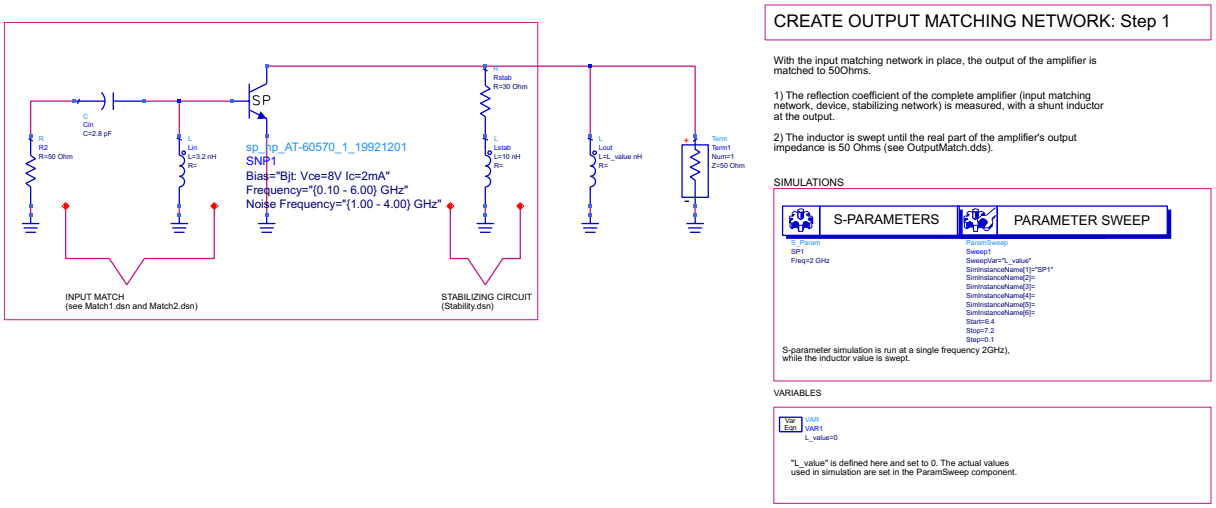


Figure 6.5: Simulation circuit for finding the value of the outputmatching inductor

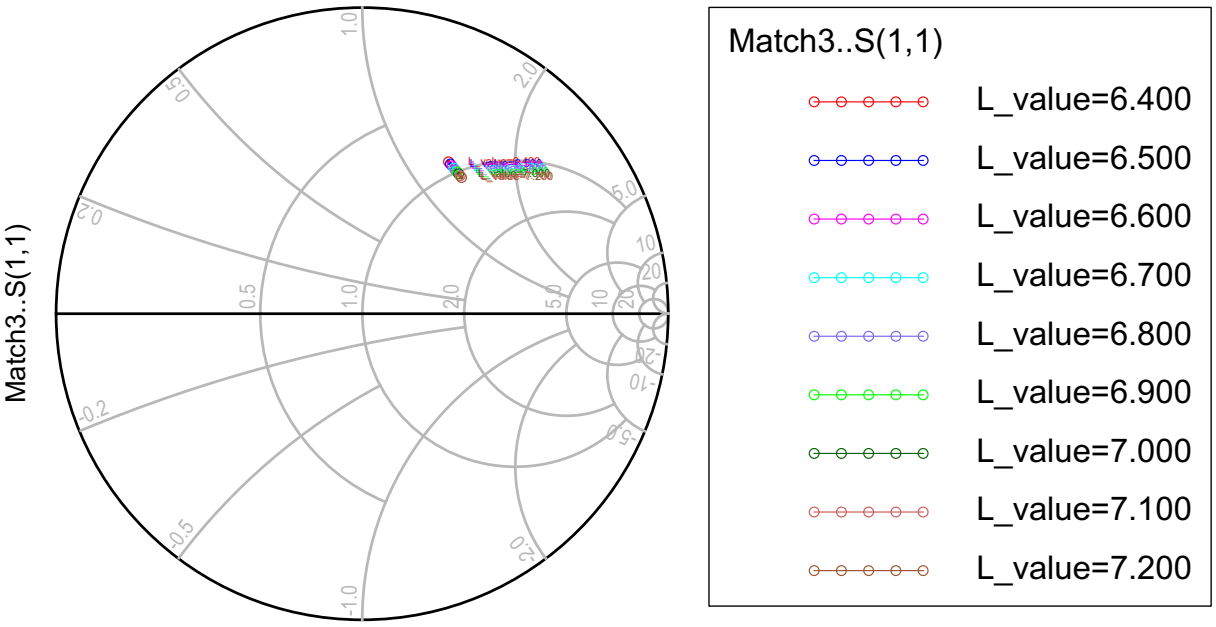


Figure 6.6: The value of the output matching inductor

The *Match4* schematic file is used to determine the value of C_{out}, as shown in Figure 6.7. The simulation results, Figure 6.8, shows that the approximate suitable value for the capacitor to lie in the origin of the smith chart is $C_{out} = 1.1pF$.

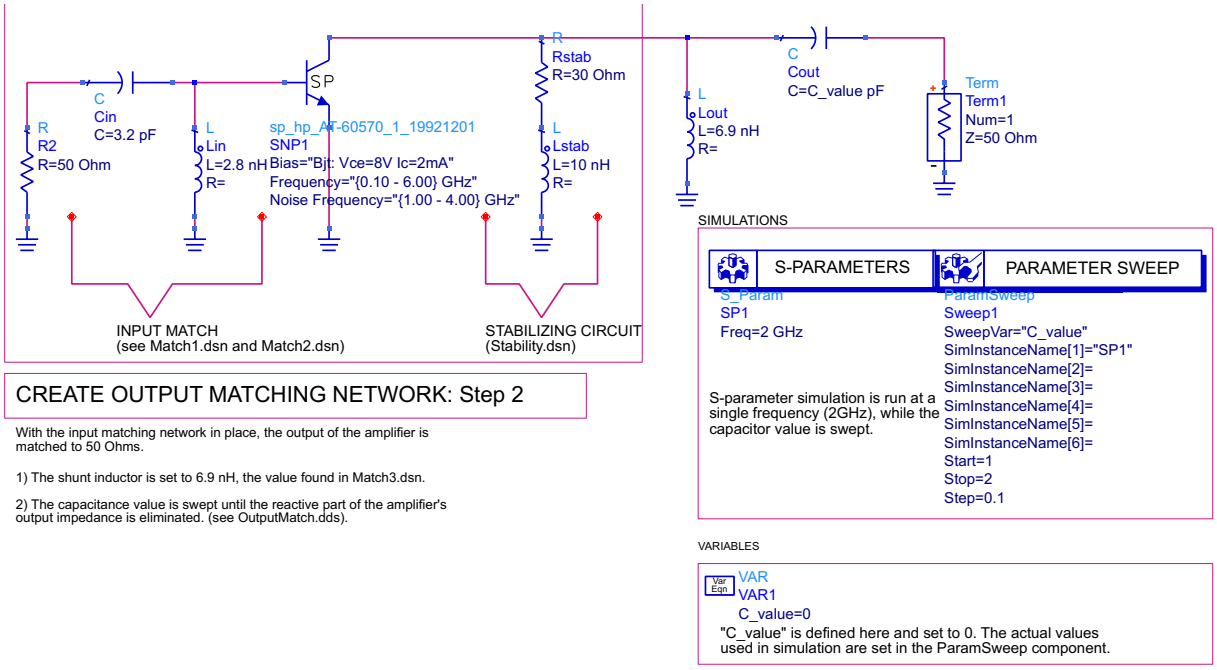


Figure 6.7: Simulation circuit for finding the value of the output matching capacitor

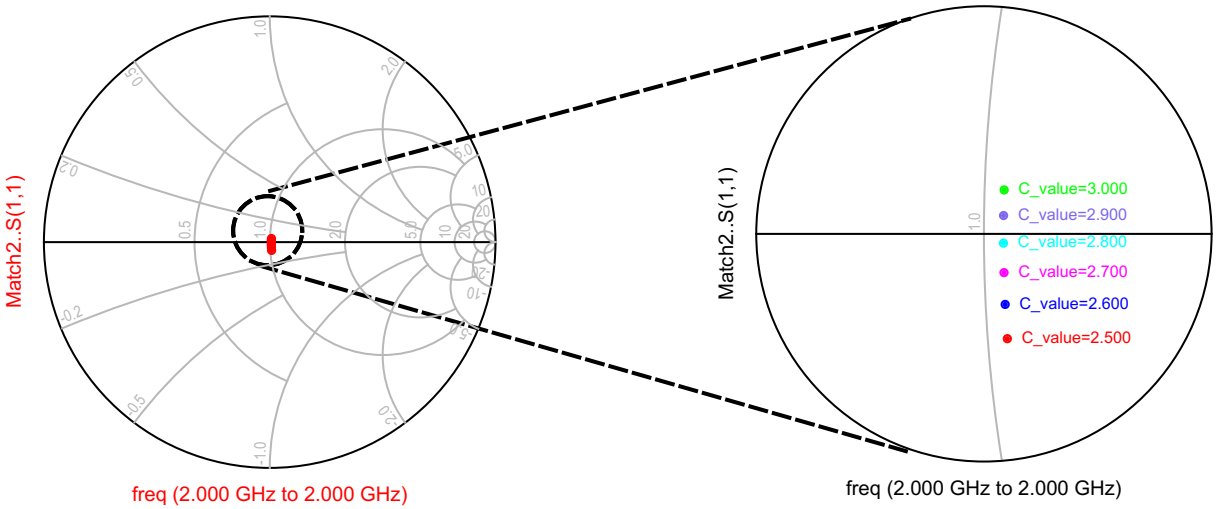


Figure 6.8: The value of the output matching capacitor

7 Finished amplifier performance

The *FinishedAmp* is used to simulate the completed amplifier design presented in Figure 7.1. The used bandwidth is [1 GHz - 4 GHz] which represents the largest bandwidth for which the noise parameters of the transistors are available. Figure 7.2 shows the result of the simulation and clearly, the amplifier meets the requirement ($NF < 2\ dB$, $S_{21} > 9\ dB$) over the bandwidth of operation [2.0 GHz - 2.1 GHz].

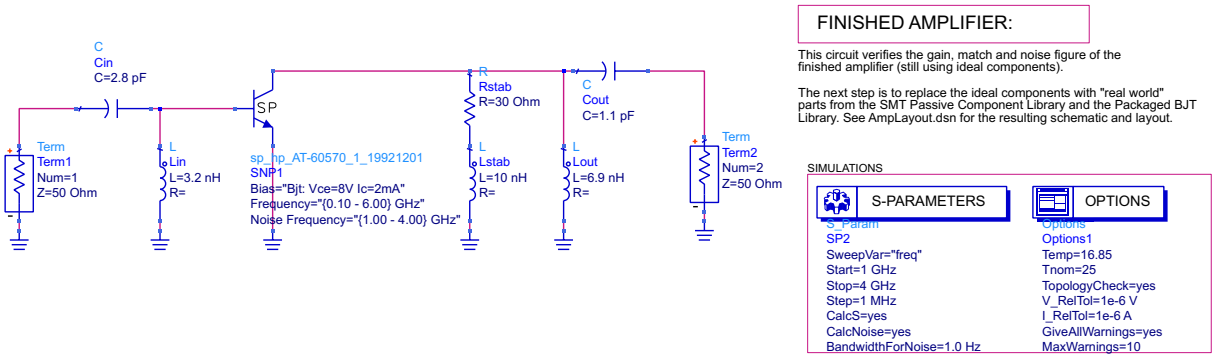


Figure 7.1: Simulation circuit for complete amplifier design

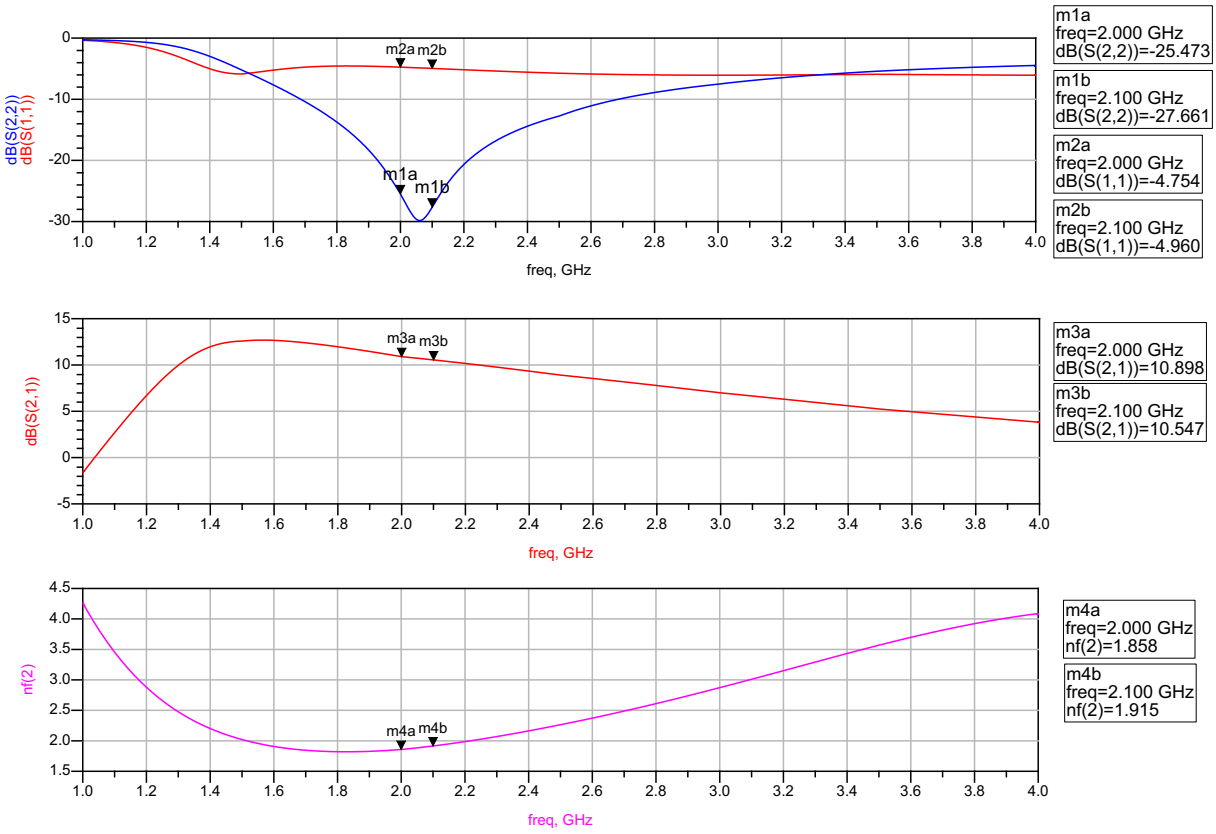


Figure 7.2: Simulation results for complete amplifier design

8 Matching with transmission lines

The matching performed previously is done using lumped elements. Another way to perform the same matching is to use a transmission line along with proper termination. Here, we study this approach for both input and output matching.

8.1 Input matching with TLs

As previously shown, the input is matched to obtain a minimum noise figure. Thus, $\Gamma_{in} = S^*_{opt} = 0.444\angle{-98.626°}$. Instead of using the manual calculations for matching, the ADS optimizer is used, as shown in the schematic of Figure 8.1 (the values are updated in the design after the optimization is completed). Here, a series TL with and a parallel open TL are used to match the input of the source to the input of the transistor. The matching network TLs are optimized to insure minimum noise figure which is conveyed by the transistor having $\Gamma_{in} = S^*_{opt} = 0.444\angle{-98.626°}$. The goal block is set to ensure minimum reflection (conveyed by S_{11} in this simulation) between the source and the matching network that presents the transistor. The electrical length βl of the transmission lines is the variable set to be optimized and it is set to be between 0° and 90° to have minimum possible physical lengths l between 0 and 0.25λ.

Figure 8.2 shows the ADS optimizer results and the number of iterations performed to converge to values used in Figure 8.3. The simulation results, Figure 6.2, shows that the suitable value for the series TL electrical length is $E_{in,series} = 72.5063°$ to lie in the unity conductance circle. It also shows that the suitable value for the parallel open stub electrical length is $E_{in,OC} = 44.7455°$ to cancel out the imaginary part of the input admittance and lie on the center of the smith chart.

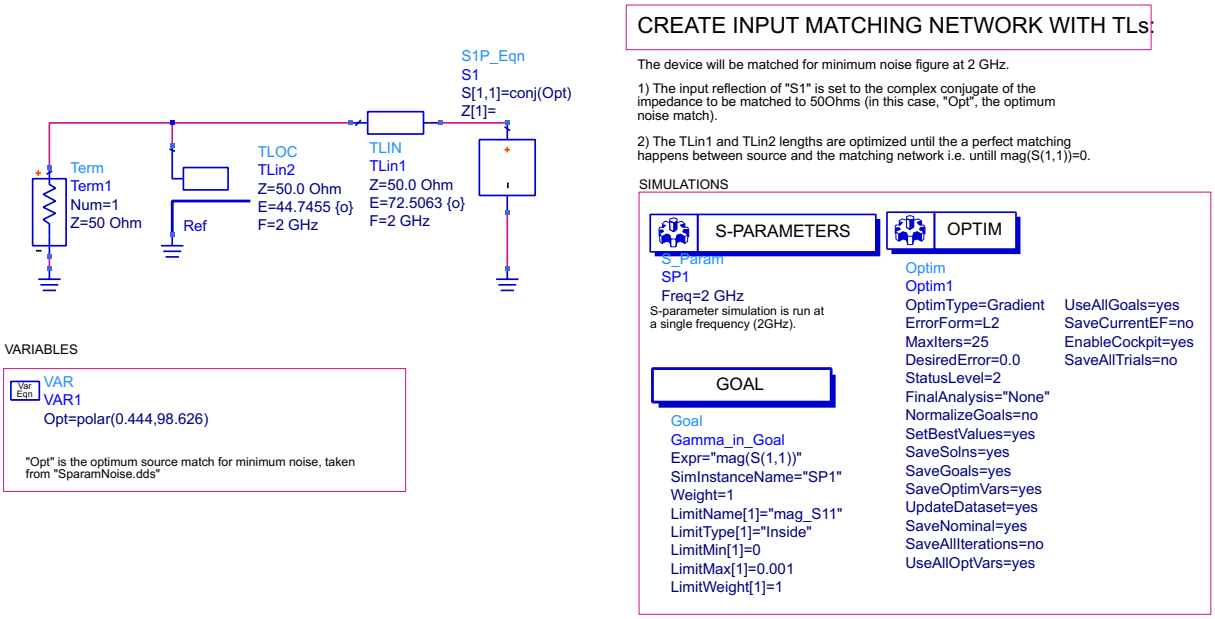


Figure 8.1: Simulation circuit for matching the input with TLs

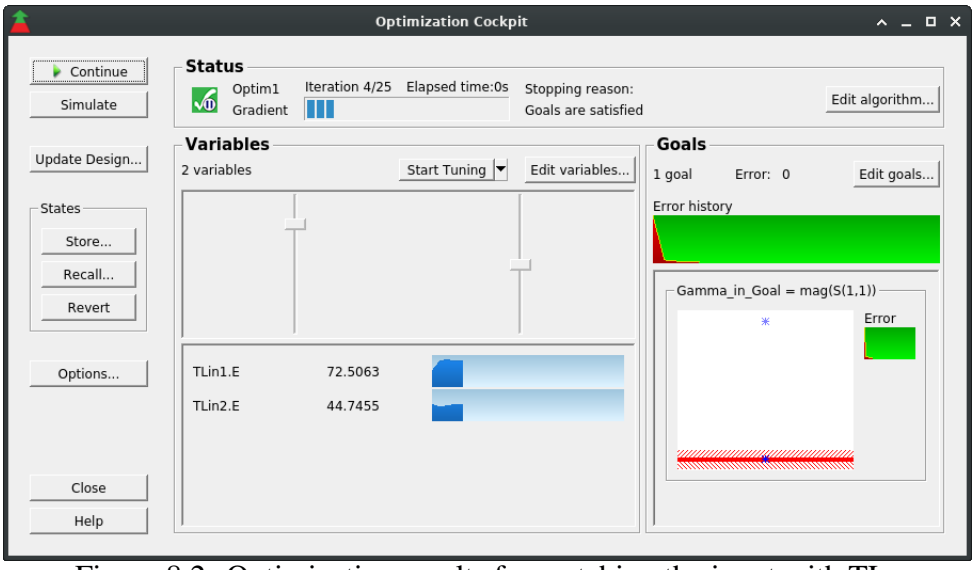


Figure 8.2: Optimization results for matching the input with TLs

Setting "SaveGoals=yes" means the expression in each goal is written to the dataset.

freq	Gamma_in_Goal	
	optIter=0	optIter=4
2.000 GHz	0.456	5.061E-5

Setting "SaveSolns=yes" means results are written to the dataset.

optIter	OPTIM.TLin1.E	OPTIM.TLin2.E
0	45.000	45.000
4	72.506	44.745

Setting "SaveOptimVars=yes" means values for TLin1.E and TLin2.E are written to the dataset for each iteration.

OPTSOLNVALS.TLin1.E	OPTSOLNVALS.TLin2.E
72.506	44.745

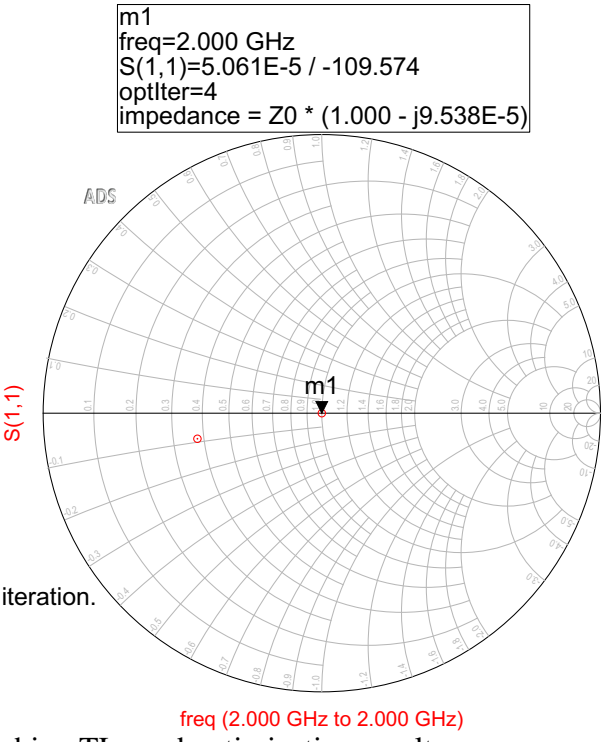


Figure 8.3: The values of input matching TLs and optimization results

8.2 Output matching with TLs

Similar to the matching with lumped elements, the matching with TLs is performed in the same manner where the electrical length βl of the lines is swept and the suitable values are used in the other sweep, but a similar approach to input with TLs using the ADS optimizer could be used also. Here a series TL with a parallel shorted stub are used to match the amplifier to the load

after adding the input matching circuit ($TL_{out,series}, TL_{out,OC}$) and terminating the source port in a 50Ω resistor.

The circuit shown in Figure 8.4 is used to determine the value of the electrical length of $TL_{out,series}$ to lie on a unity conductance circle. The simulation results, Figure 8.5, shows that the approximate suitable value for the electrical length of $TL_{out,series}$ is $E_{out,series} = 52.8°$.

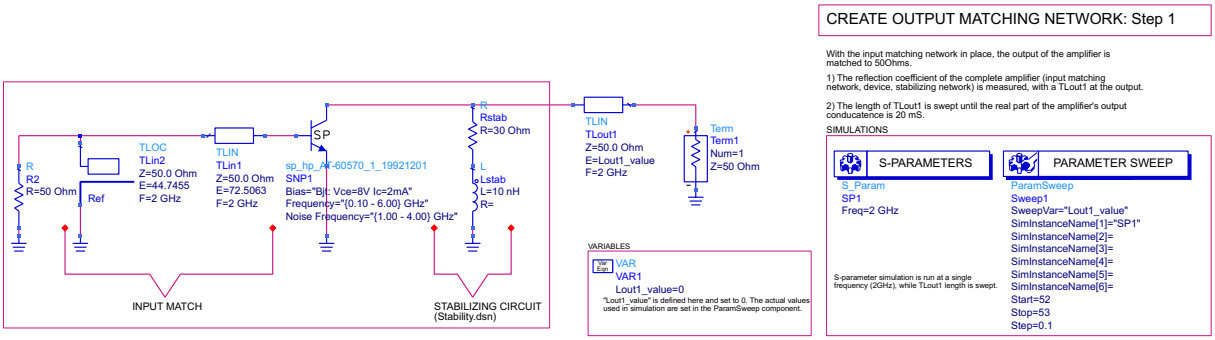


Figure 8.4: Simulation circuit for finding the electrical length of the output matching series TL

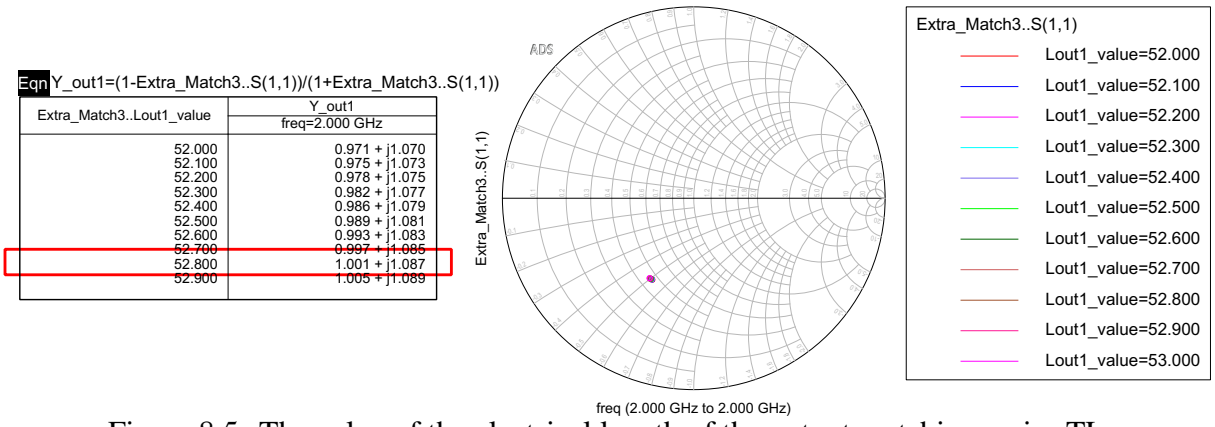


Figure 8.5: The value of the electrical length of the output matching series TL

The circuit shown in Figure 8.6 is used to determine the value of the electrical length of $TL_{out,SC}$ to lie on a center of the smith chart and cancel the imaginary part of the output admittance. The simulation results, Figure 8.7, shows that the approximate suitable value for the electrical length of $TL_{out,SC}$ is $E_{out,SC} = 42.6°$.

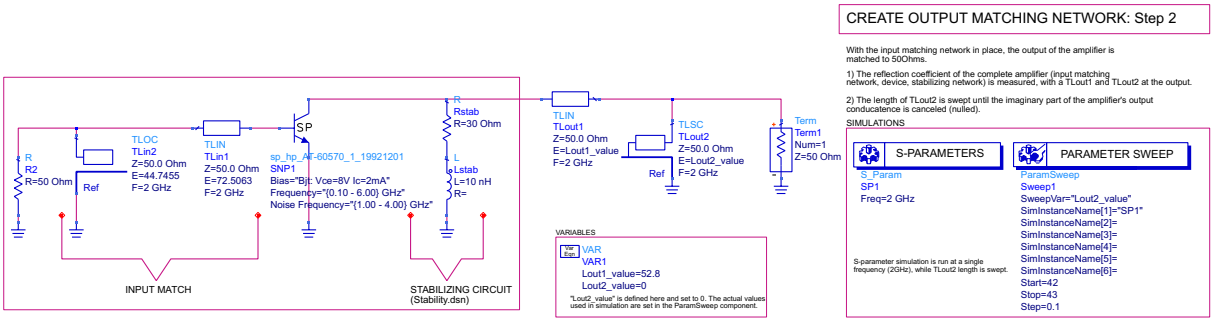


Figure 8.6: Simulation circuit for finding the electrical length of the output matching shorted stub

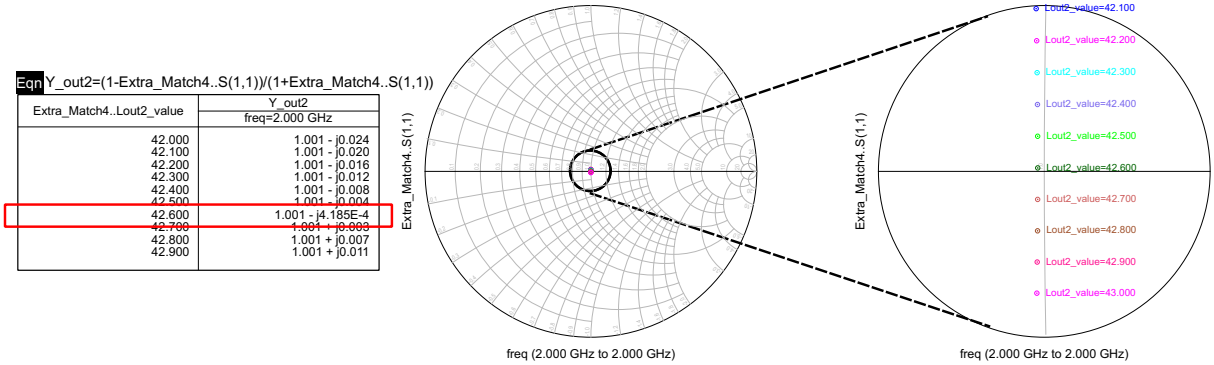


Figure 8.7: The value of the electrical length of the output matching shorted stub

The performance of the TL matched amplifier is tested using the circuit shown in Figure 8.8. The performance was approximately equal to the lumped elements matched over the band of operation $[2GHz, 2.1GHz]$ as shown by plots and markers in Figure 8.9. However, the performance degrades (especially at higher frequencies) due to the narrow matching of the TLs.

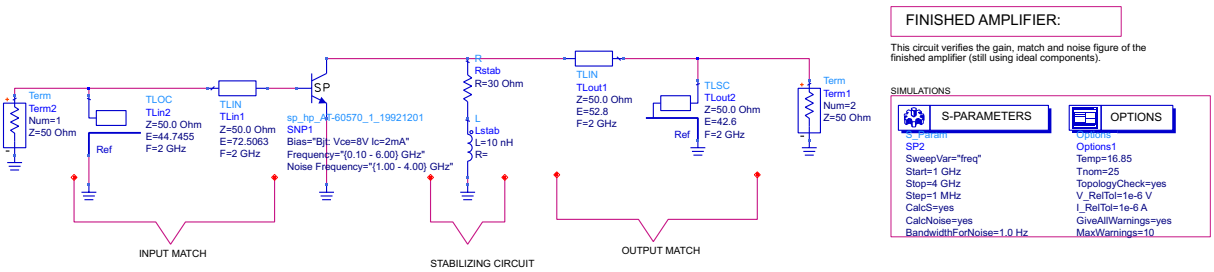


Figure 8.8: Finished design of the TL matched amplifier

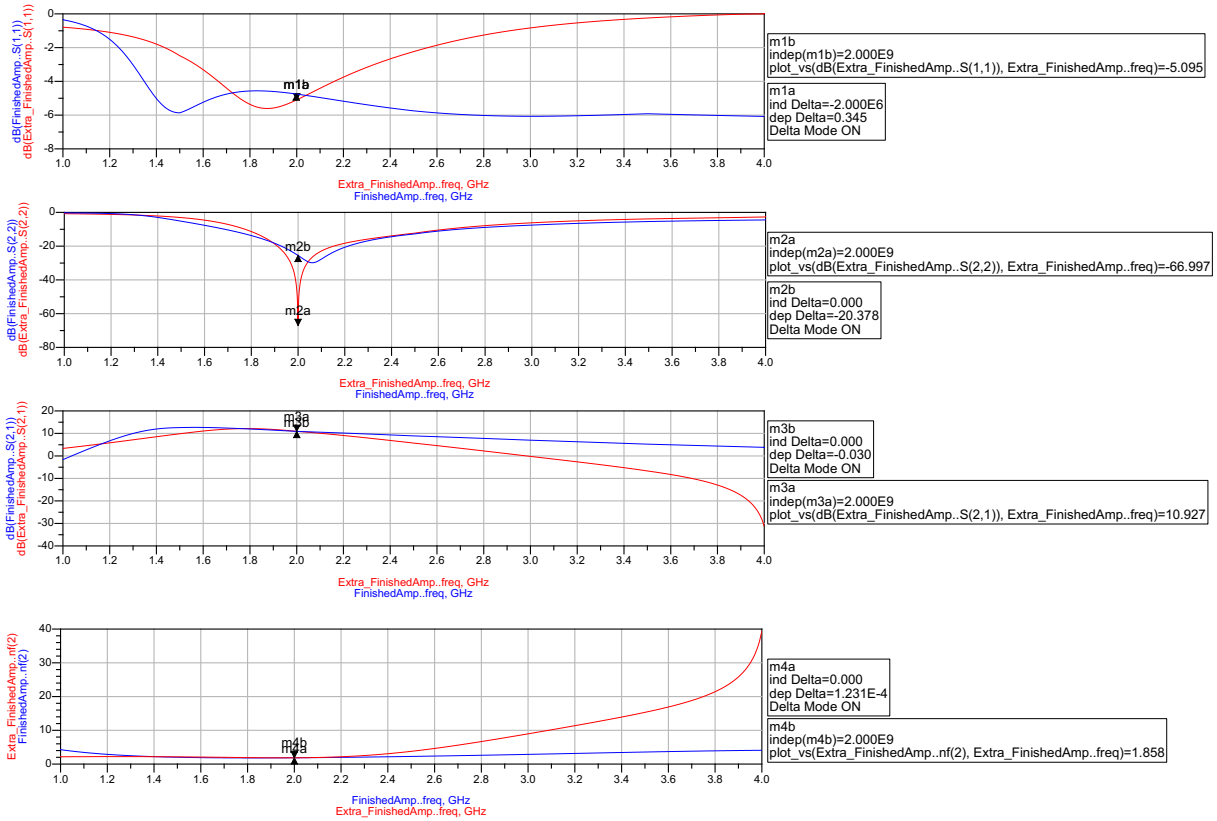


Figure 8.9: Performance comparison of TL and lumped elements matched amplifiers

9 The stability of the final amplifier

The finished amplifier matched using the lumped elements, Figure 7.1, is tested for stability. The amplifier is clearly stable as shown in Figure 9.1.

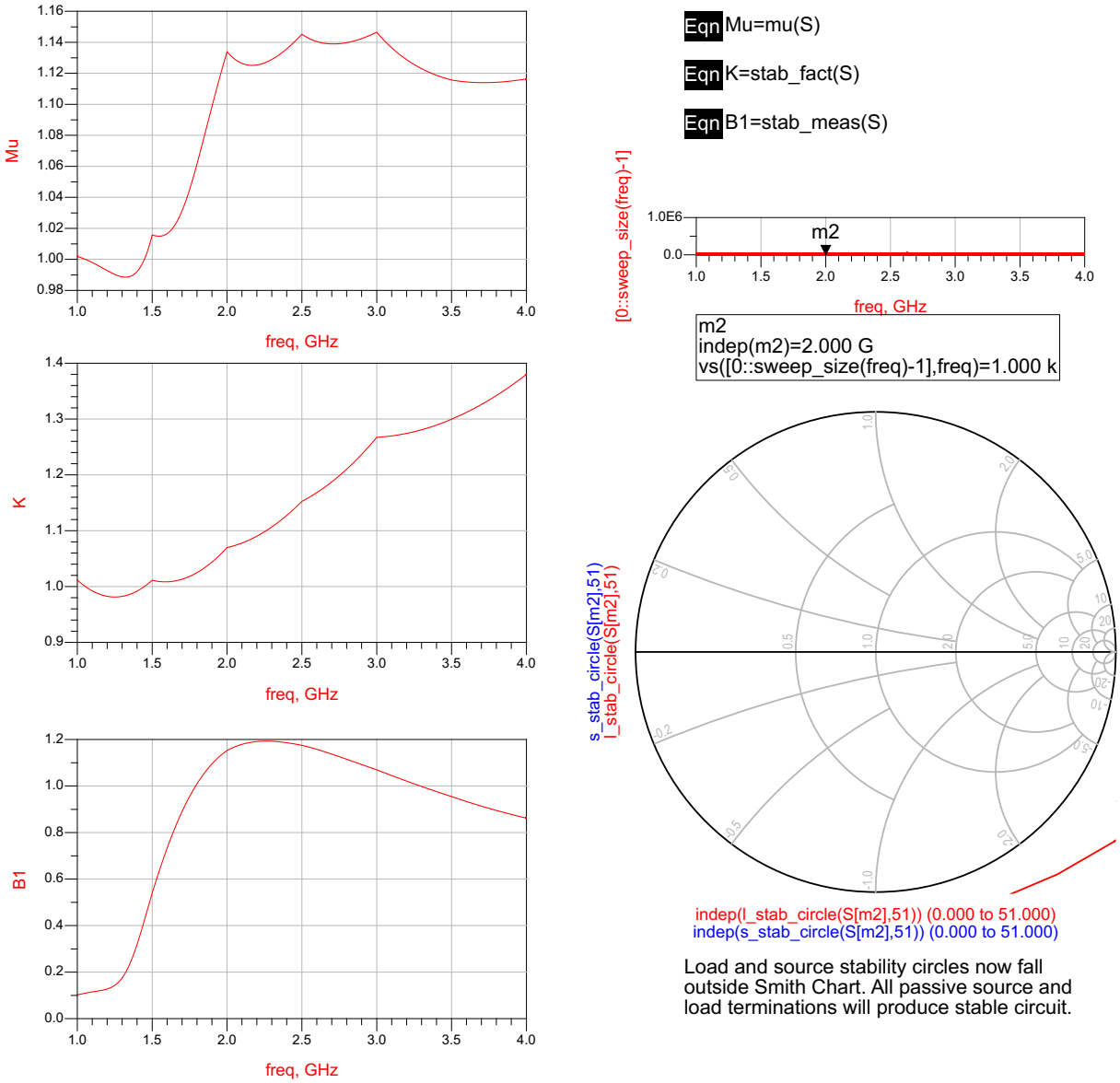


Figure 9.1: Stability results for complete amplifier design

10 Adapting the amplifier for higher frequencies

To increase the operating frequency to 10 GHz, there are a couple of changes that should take place.

The transistor needs to be changed completely because its unity gain frequency f_T is much lower than 10 GHz [2]. The matching networks need to be implemented using the TLs as the lumped elements (especially inductors) are rare to operate at such frequencies and they introduce a lot of parasitics that needs to be modeled. The bias circuitry need to be coupled correctly to the transistors with better DC and AC blockers such as TL based quarter wave transforms to suppress the leakages in the layout phase.

11 Feedback

We did find the laboratory work very helpful as it presents how the course theory could be applied in the design phase. The lab work proceeded smoothly. The main problem in this lab was interfacing to a Linux machine and ADS through the browser, it was hard to switch between the ADS windows and deal with latency of the clicks. There was a small problem with the license but once one of us finished working he passed and freed the license to the other. The design exercise content was reasonable and it didn't take much time to finish.

We wish the deadline was fixed so that we keep focus on the design exercise and get our grades in the expected time but we acknowledge the license issues that lead to various extensions. We wish if the lab work touched other blocks we learned about in the theory of the course such as mixers and oscillators and also we wish if it had a layout phase where the designed amplifier would be layed out on certain PCB and then the the effects of the PCB could be studied and the performance is further compared with the schematic design.

Appendices

A Manual Matching

A.1 Input matching

In this part, we're performing the manual matching of input and output circuits for our design and comparing it with the values we got from the trial and error for the simulation. The manual matching could be done using the smith chart or by calculations [3] [4]. To achieve a minimum noise figure as we saw earlier we need to match the input to S_{opt} or in other words $\Gamma_{in} = S^*_{opt} = 0.444\angle{-98.626}°$.

At first, the impedance Z^*_{opt} (corresponding to$Y^*_{opt} = G^*_{opt} + jB^*_{opt}$) is placed on the chart at corresponding $\Gamma_{in} = \Gamma^*_{opt}$. Then, the inductor L_{in} will move the admittance seen by the source ($Y_{source} = G_{source} + jB_{source}$) counterclockwise. The value required for L_{in} is the one that indicates the intersection of the impedance seen by the source with the unity resistance circle on the top half of the smith chart (due to the nature of the L network elements selected in this design), and its could be calculated as

$$\Delta B = \left|B^*_{opt} - B_{source}\right| = \frac{1}{\omega L_{in}} = \frac{1}{2\pi f L_{in}} \implies L_{in} = \frac{1}{2\pi f \left|B^*_{opt} - B_{source}\right|} = 3.1691nH$$

Then the input capacitance C_{in} will move the impedance seen by the source ($Z^{'}_{source} = R^{'}_{source} + jX^{'}_{source}$) from the intersection with unity resistance circle to the center of the smith chart Z_0 along a constant resistance circle counterclockwise, and its could be calculated as

$$\Delta X = |X_0 - X_{source}| = X_{source} = \frac{1}{\omega C_{in}} = \frac{1}{2\pi f C_{in}} \implies C_{in} = \frac{1}{2\pi f X_{source}} = 2.7909nH$$

Both input matching steps are presented in Figure A.1[5]. The resulting values of the capacitor and inductor at 2 GHz agree with the values we found using the sweeping in Section 6.1.

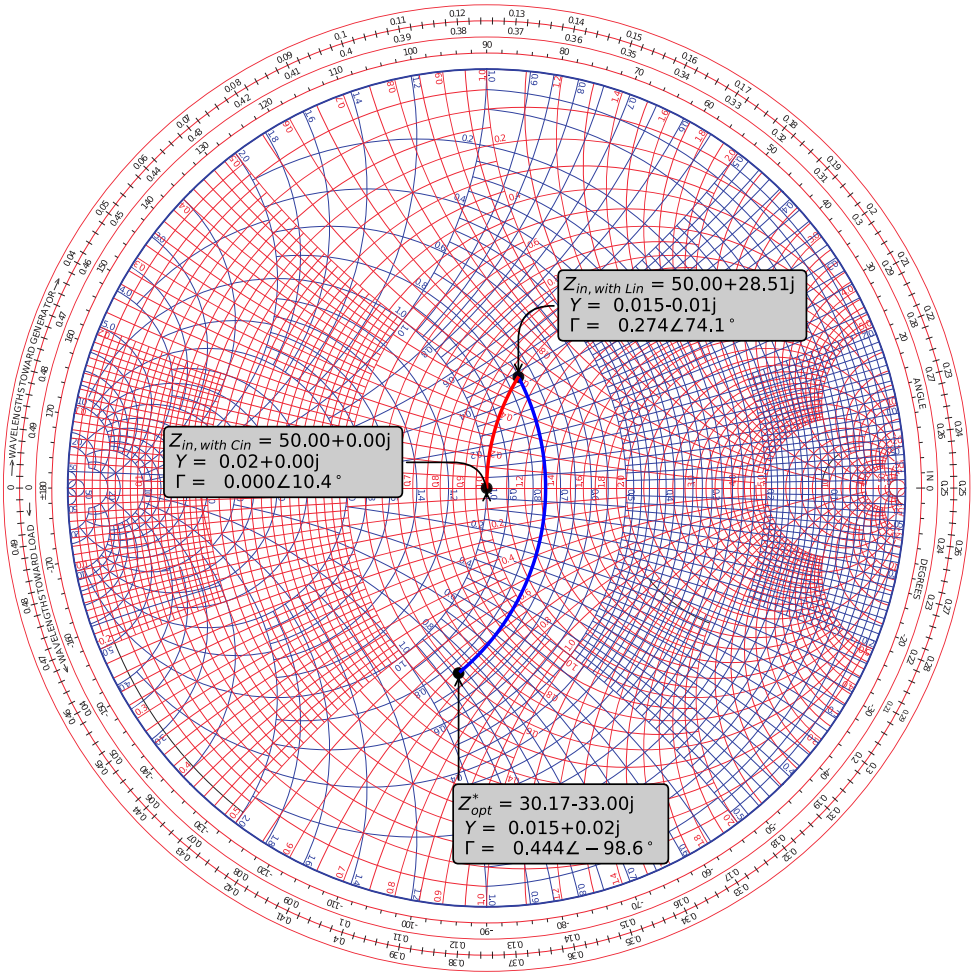


Figure A.1: Manual input matching using Smith Chart

A.2 Output matching

For the output matching we should have $\Gamma_L = \Gamma^*_{out}$. Γ_{out} in this case represents the reflection coefficient seen by the load corresponding to $(Z_{out} = R_{out} + jX_{out})$ and $(Y_{out} = G_{out} + jB_{out})$.

First, the output impedance of the transistor is calculated assuming the optimum termination at the input as follows

$$\Gamma_{out} = S_{22} + \frac{\Gamma_{source} S_{21} S_{12}}{1 - \Gamma_{source} S_{11}} = S_{22} + \frac{\Gamma_{opt} S_{21} S_{12}}{1 - \Gamma_{opt} S_{11}} = 0.6575\angle{-52.9476}^\circ$$

$$Z_{out} = Z_0 \frac{1 + \Gamma_{out}}{1 - \Gamma_{out}} = 93.2254\angle{-61.5939}^\circ\Omega$$

Then, the stability $Z_{stab} = R_{stab} + j\omega L_{stab}$ is added in parallel to get

$$Z_{out,\,with\,StabCkt} = Z_{out} \parallel Z_{stab} = 134.64 - j37.202\Omega$$

$$\implies \Gamma_{out,\,with\,StabCkt} = \frac{Z_{out,\,with\,StabCkt} - Z_0}{Z_{out,\,with\,StabCkt} + Z_0} = 0.4909\angle{-12.3346}^\circ$$

The output matching is performed in a similar manner to th input matching (moving to the intersection to with unity resistance circle then to the origin) and we get

$$L_{out} = \frac{1}{2\pi f \left| B_{out,\ with\ StabCkt} - B_{out,\ with\ Lout} \right|} = 6.9719nH$$

$$C_{out} = \frac{1}{2\pi f X_{out,\ with\ Lout}} = 1.1551nH$$

The previous output matching steps are presented in Figure A.2[5]. Again, the resulting values of the capacitor and inductor at 2 GHz agree with the values we found using the sweeping in Section 6.2.

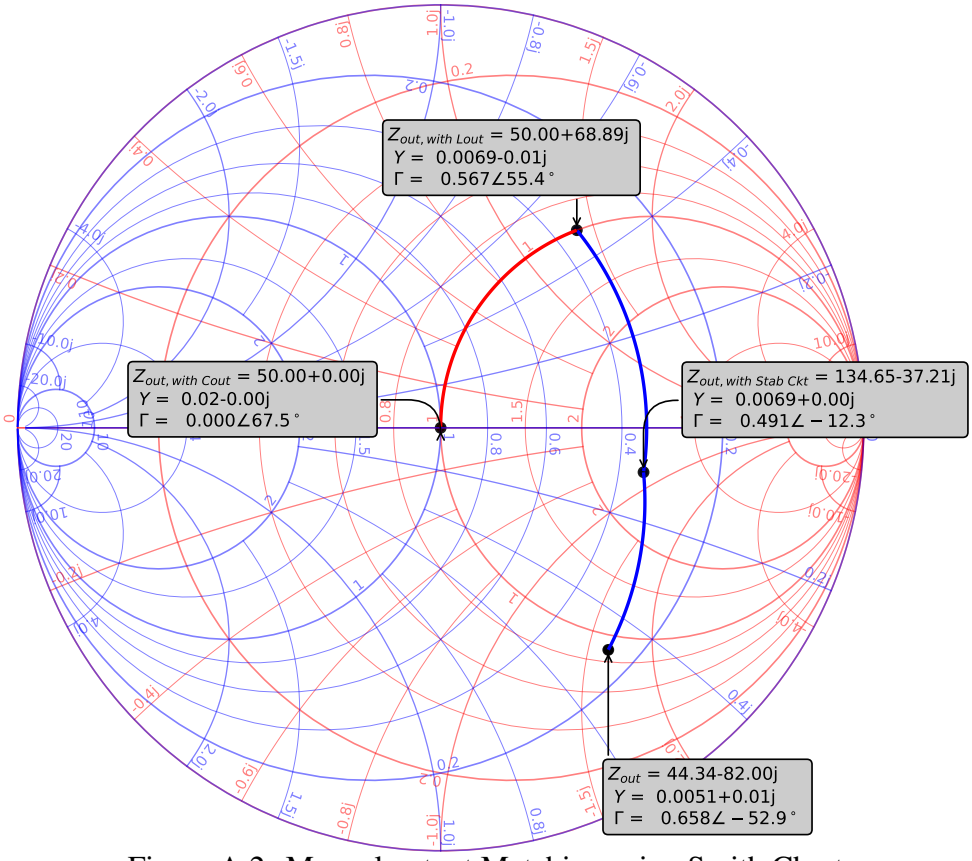


Figure A.2: Manual output Matching using Smith Chart

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