UNIVERSITY OF OULU

FACULTY OF INFORMATION TECHNOLOGY AND ELECTRICAL ENGINEERING - ITEE

ELECTRONICS DESIGN 3

DESIGN EXERCISE REPORT

Students:

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1. Mirror based OTa

The two stage OpAmp to be used in the design exercise is shown in Figure **??** in which the bias circuitry is simplified.

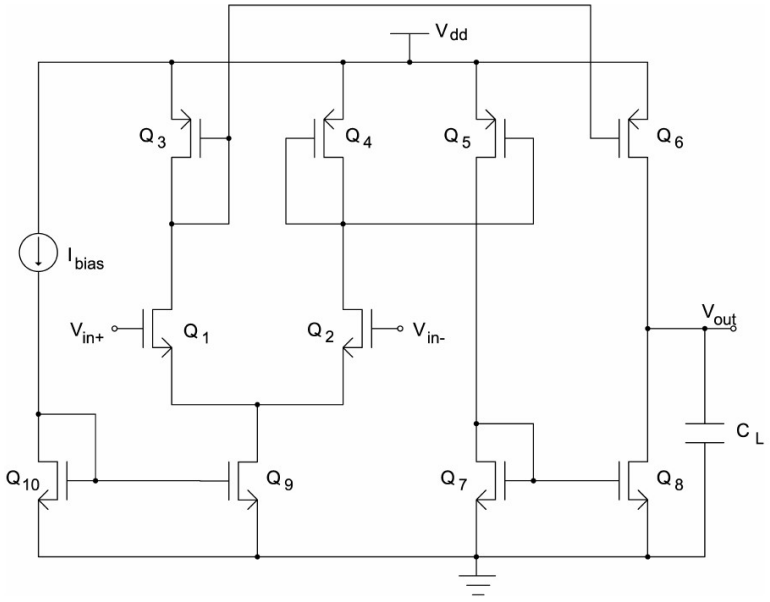

Figure 1: Mirror based OTA schematic

2. Sizing the OTA

The hand calculation of the Mirror based OTA are provided in the textbook [Analog Integrated Circuit Design, 2E] and are further explained in exercise 2.2 and the lab manual. The specifications of f_t and SR were stressed by 20% to meet the requirements, and the output and CM input ranges were increased by 200 mV for the same reason.

Figure 2 shows the OTA without the bias circuit. A constant G_m circuit is used to provide the bias current and Figure 3 shows the OTA with the bias circuit. In addition transistor were divided using the finger multiplier coefficient and dummy ones were added to prepare for the layout. Table 1 shows the results of hand calculations and the tweaking and optimization to ease the layout and match the DC operating points with the simplified bias circuit.

Table 1: The results of all the simulations

	Length (μm)	Calculated total Width (μm)	Optimized total Width (μm)	Nbr Fingers
W_1, W_2	0.4	3.95	4	4
W_3, W_4, W_5	3	3.91	4	4
W_6	3	7.81	8	8
W_7	3	4.69	4.6	2
W_8	3	9.38	9.2	4
W_9, W_10, W_11	3	3.54	3.6	6
W_12, W_14	3	3	3	2
W_15	3	3	12	8
R_{bias}	/	15.5 KΩ	4.4 KΩ	/
I_{bias}	/	74 μA	75 μA	/

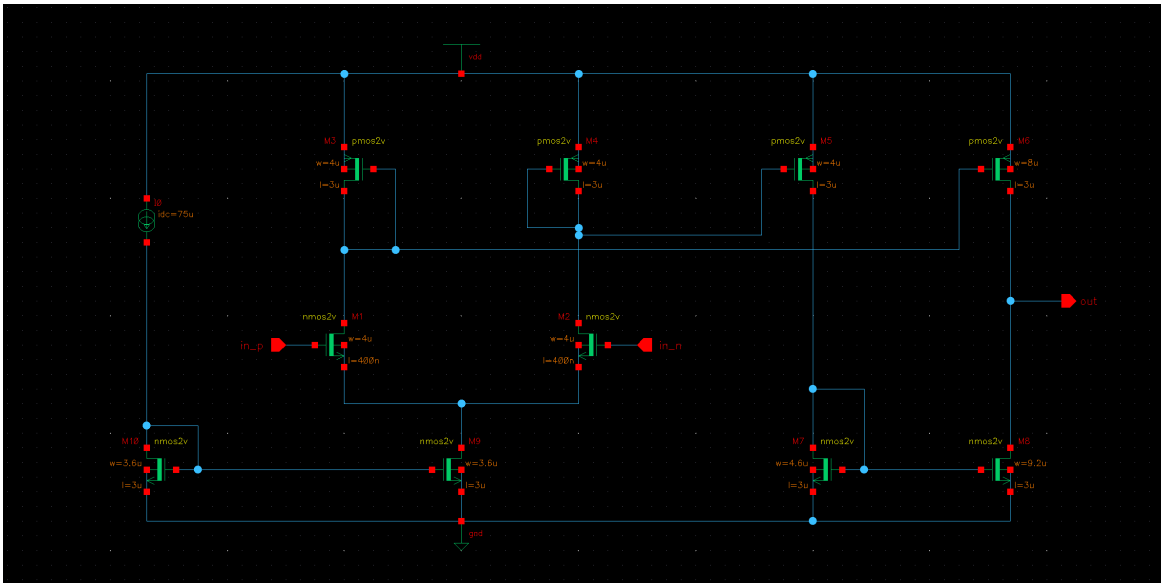

Figure 2: OTA schematic with simplified bias circuit

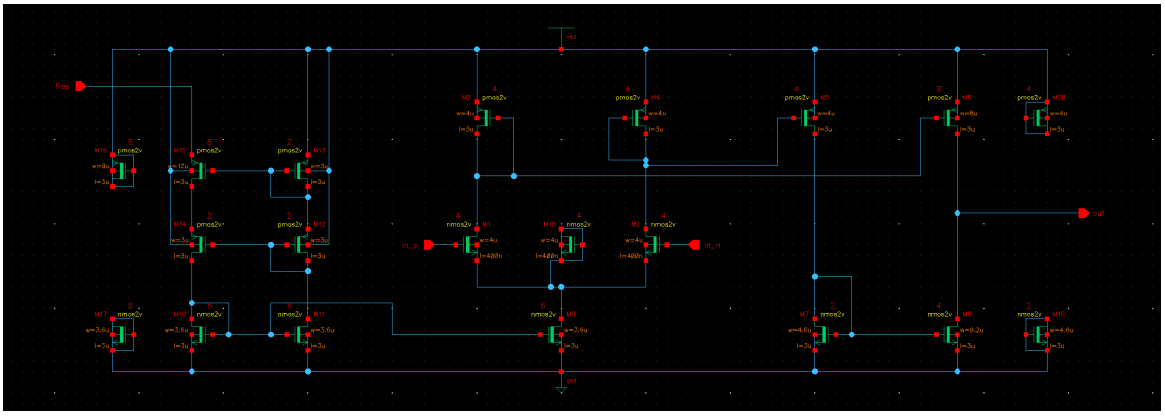

Figure 3: OTA schematic with constant G_m bias circuit

3. Schematic Simulations

In th subsections bellow, the different test benches and their results, Figure 4 are presented. The main results are summarized in Table 2 bellow.

Table 2: The results of all schematic simulations

	OTA simulation result	Figure
f_{ta}	11.56908 MHz	7
BW	123.163 kHz	7
A_0	39.48111 dB	7
PM	75.3938°	7
Slew Rate	14.334105 MV/s	12
$V_{in,CM}$ range	[1.014768 V , 2.325984 V]	11
V_{out} range	[564.0741 mV , 2.235647 V]	13

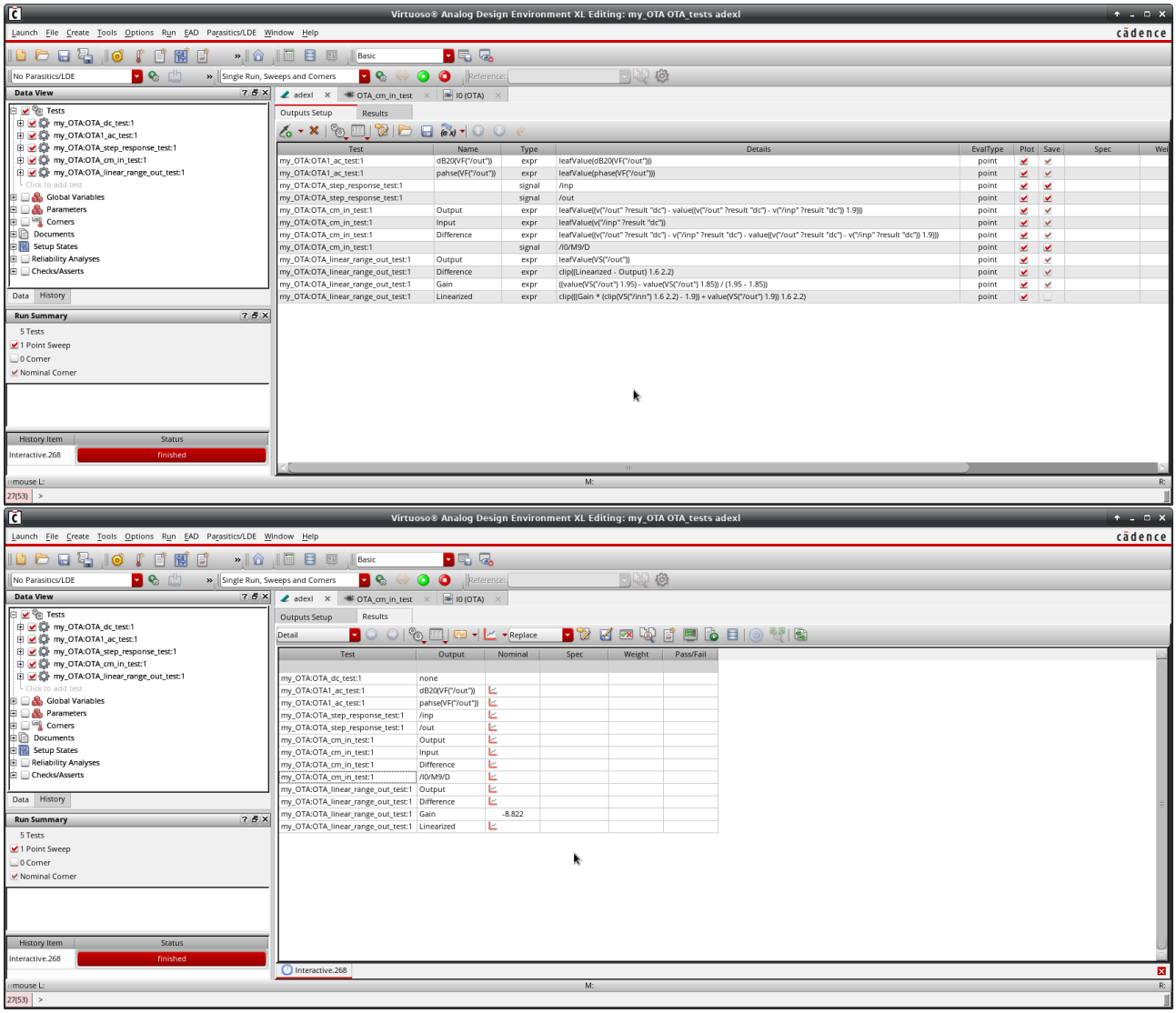

Figure 4: Tests setup and their results

3.1 DC simulation

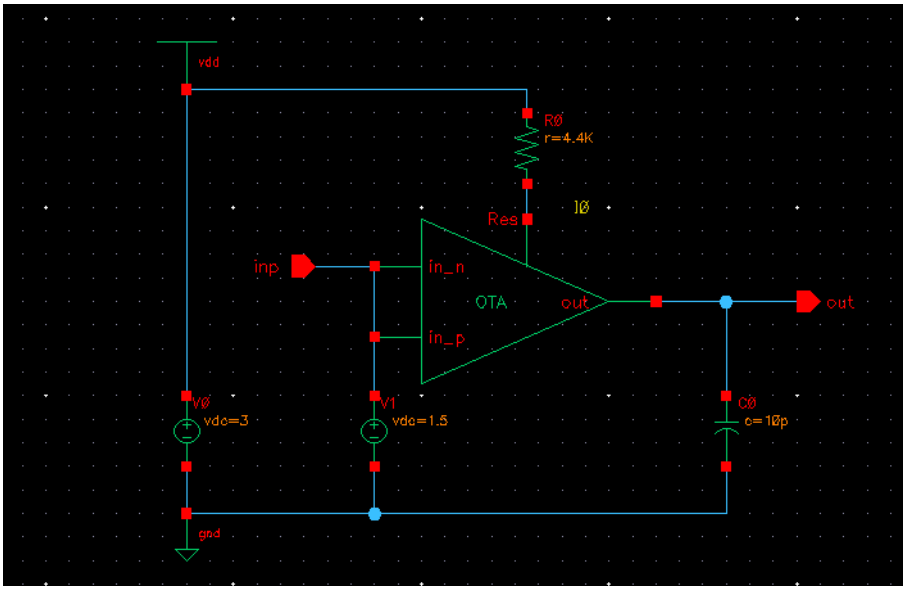

Figure 5: DC simulation test bench

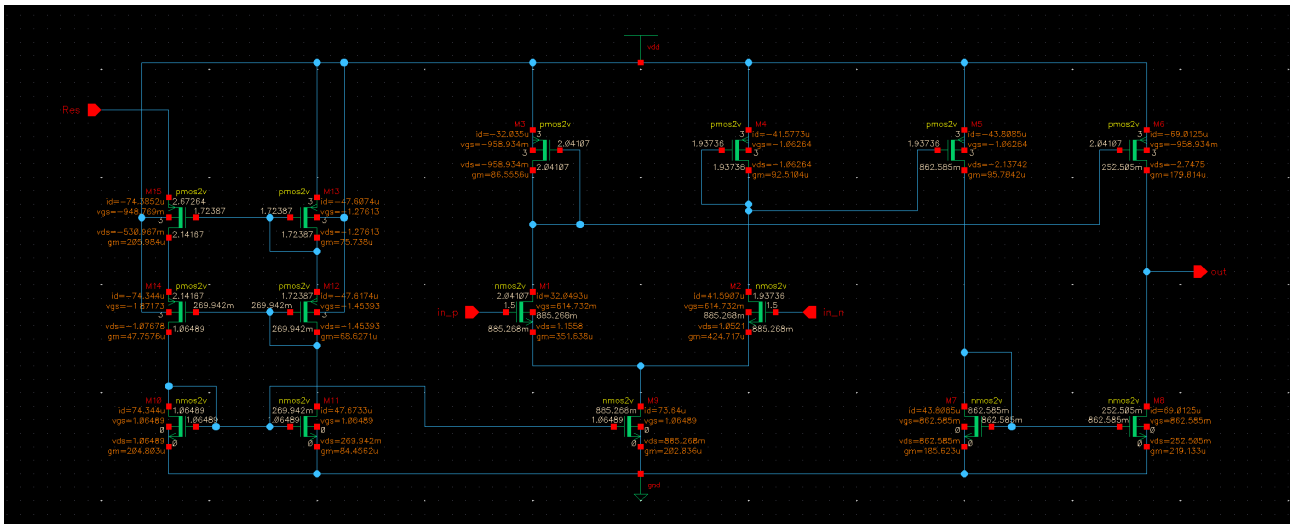

Figure 6: DC operating point of the OTA

3.2 AC Response

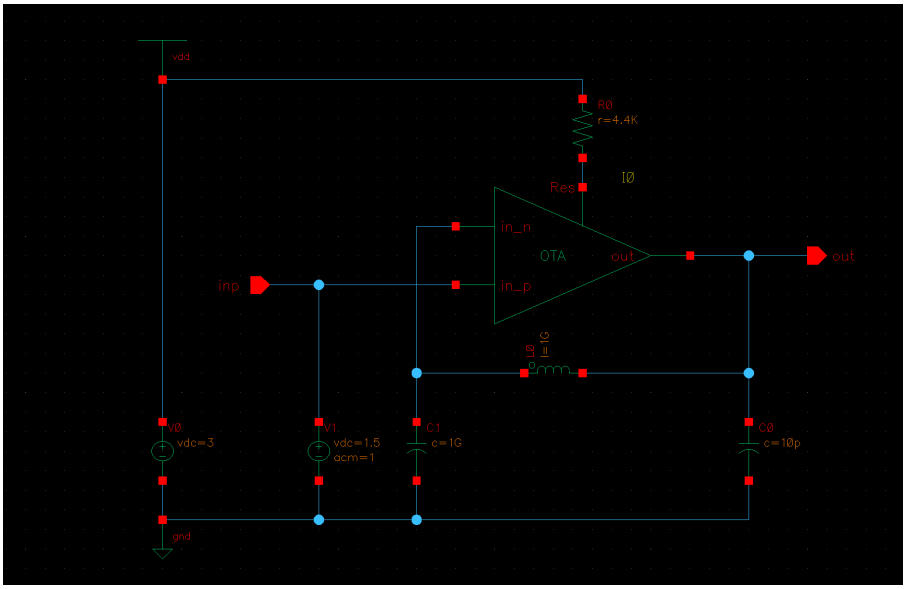

Figure 7: AC response test bench

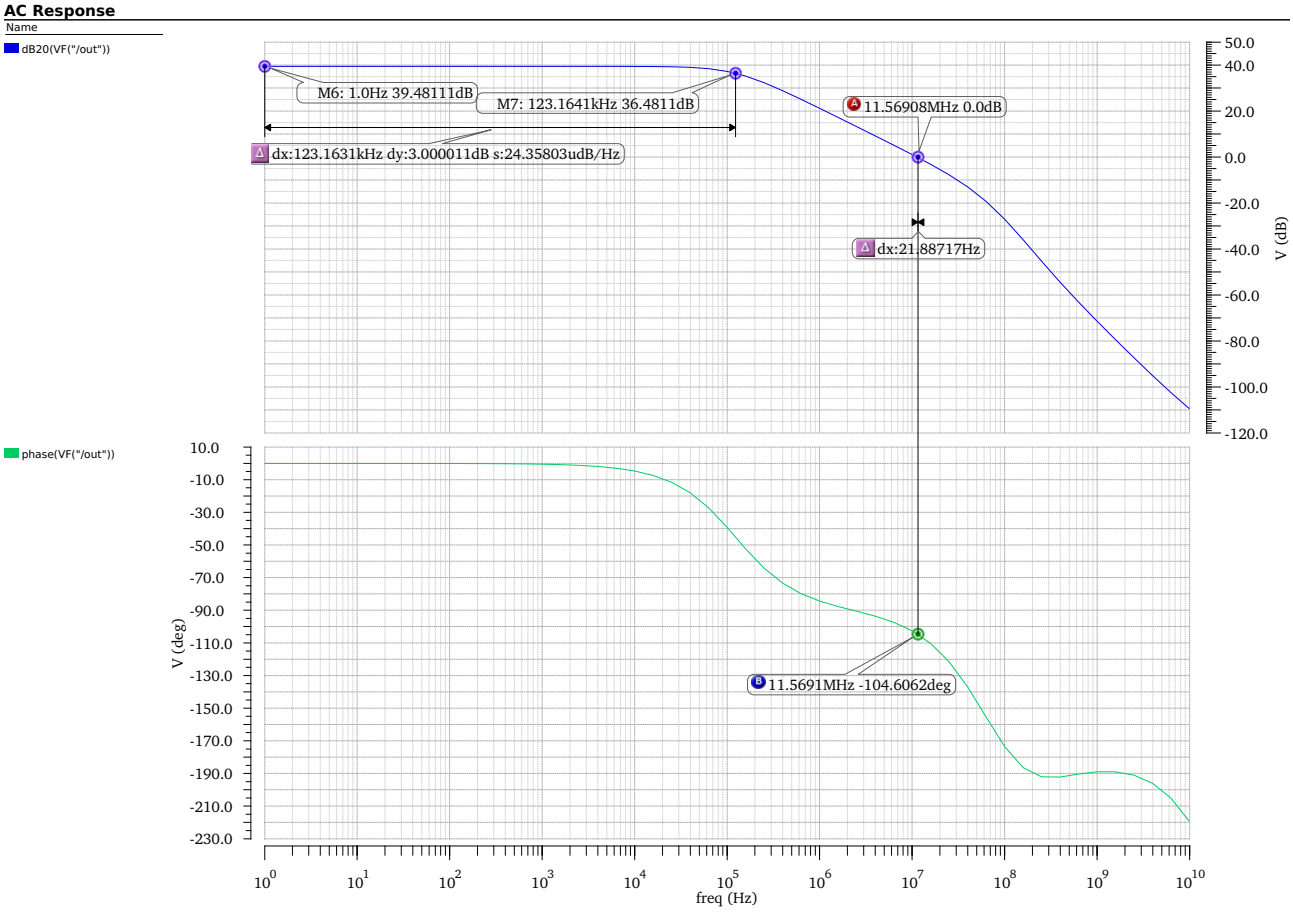

Figure 8: AC response of the OTA

3.3 Step Response

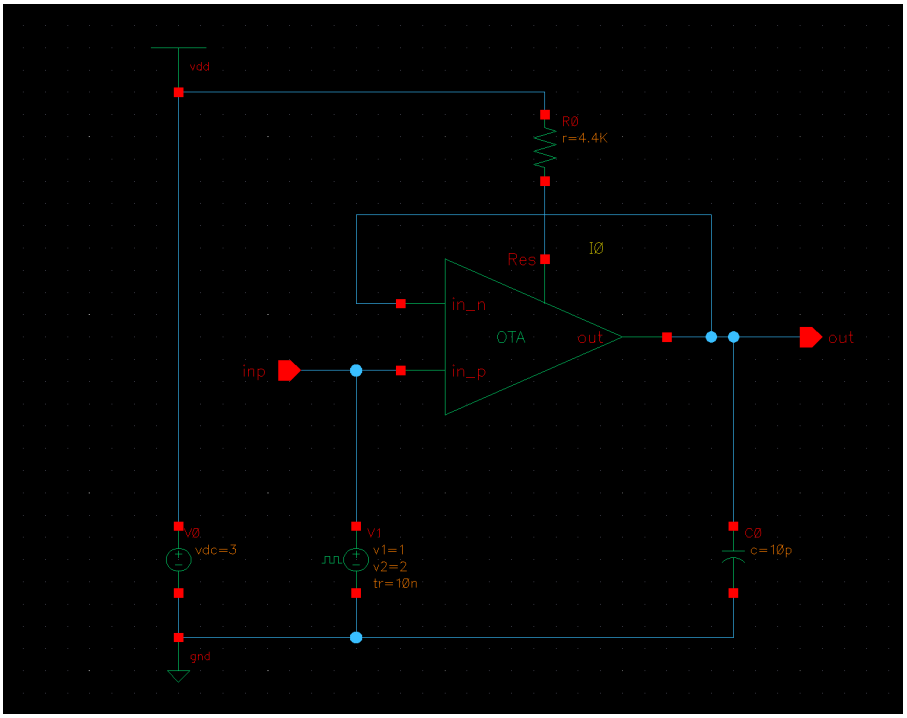

Figure 9: Step response test bench

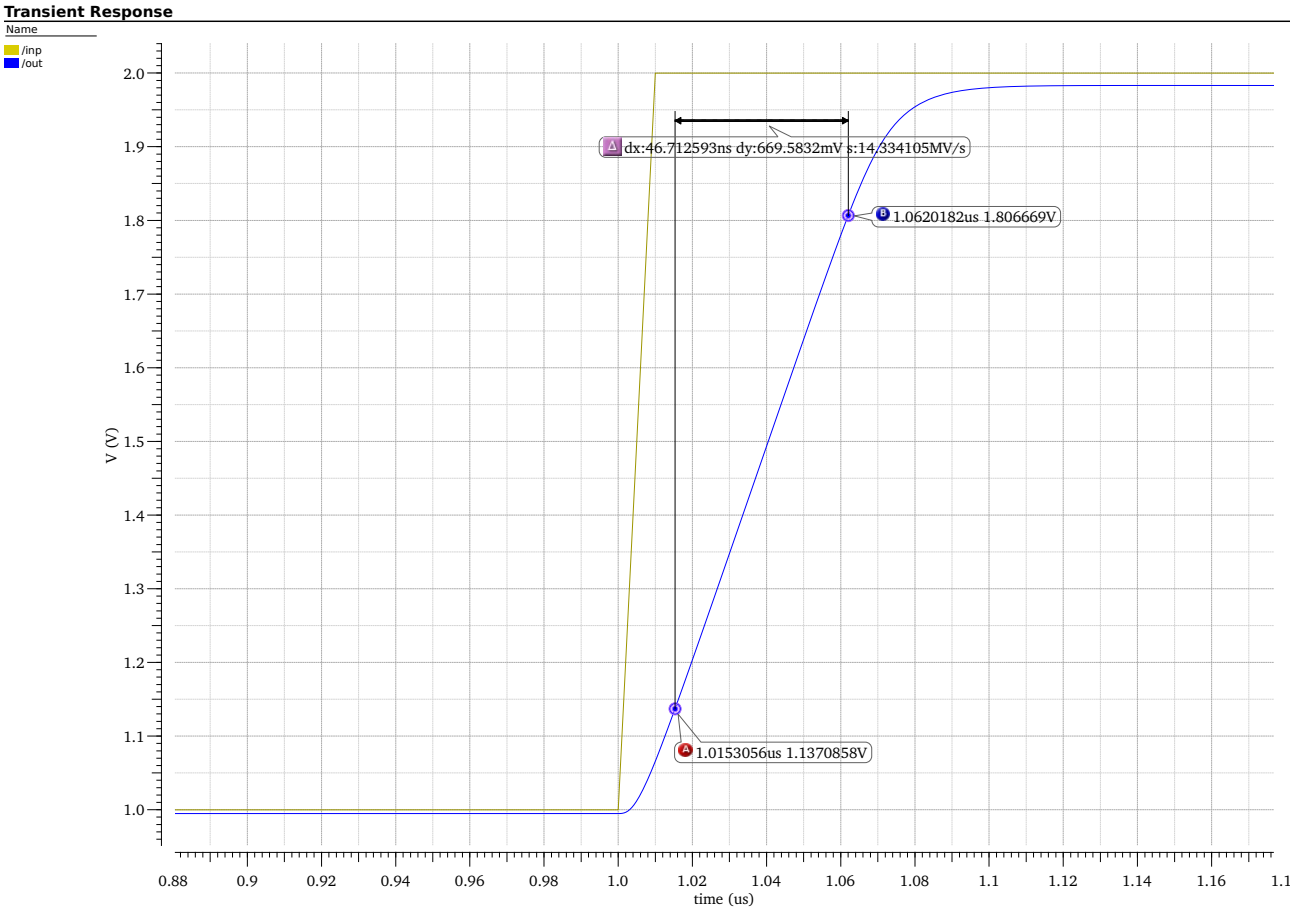

Figure 10: Step response of the OTA

3.4 Input Common mode (CM) range

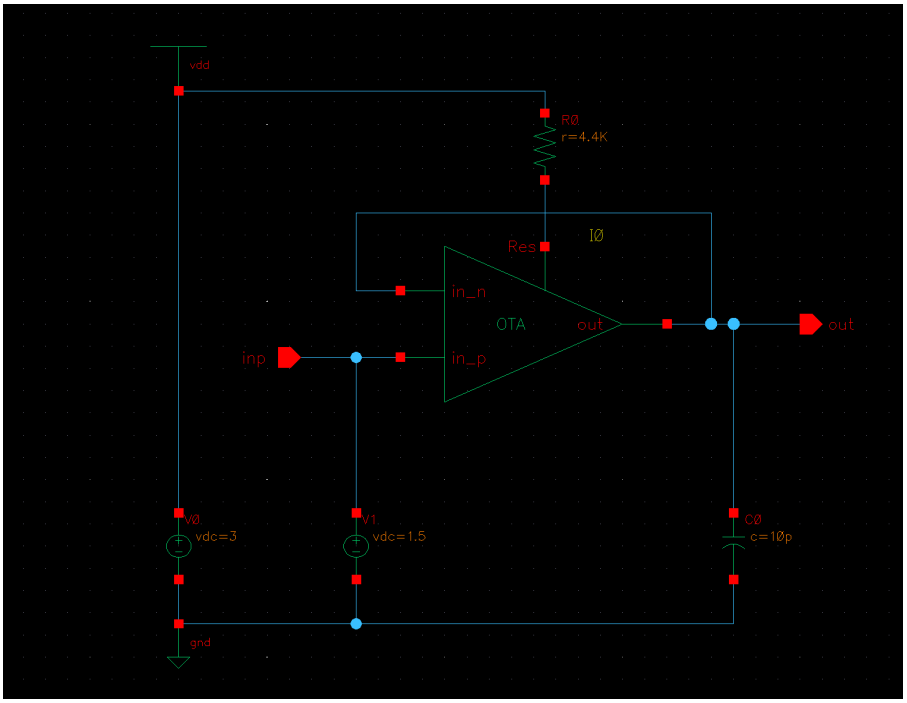

Figure 11: Input CM range test bench

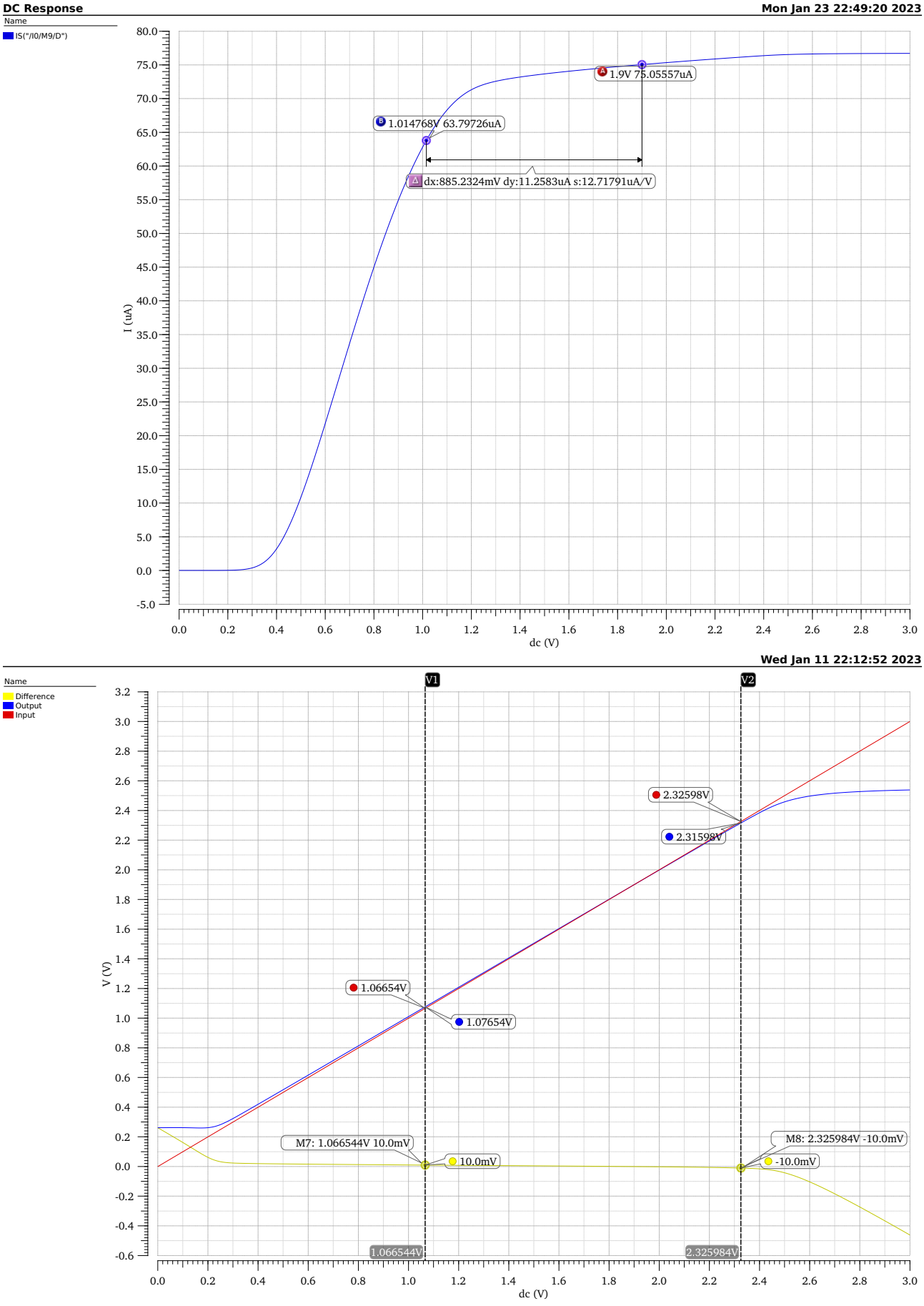

Figure 12: Minimum and maximum input CM range simulation for the OTA

3.5 Output range

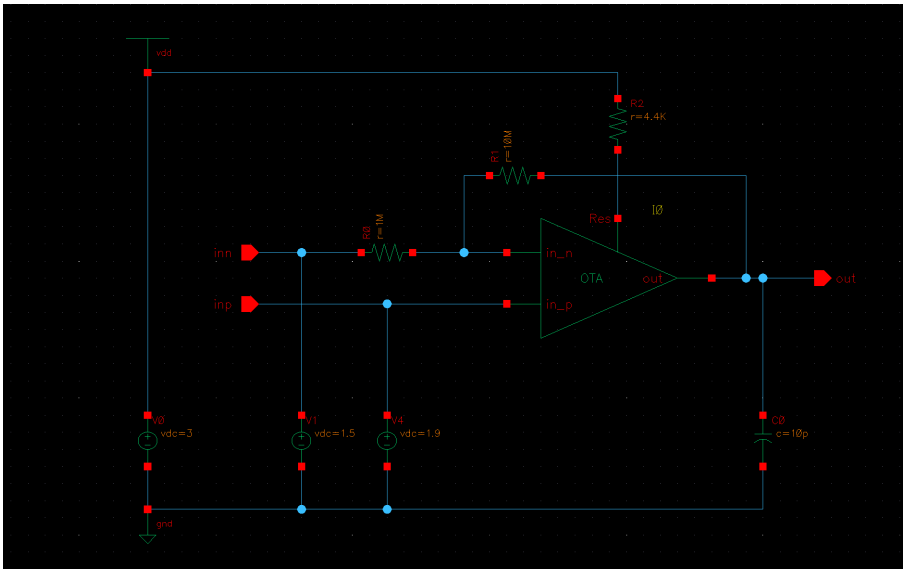

Figure 13: Output range test bench

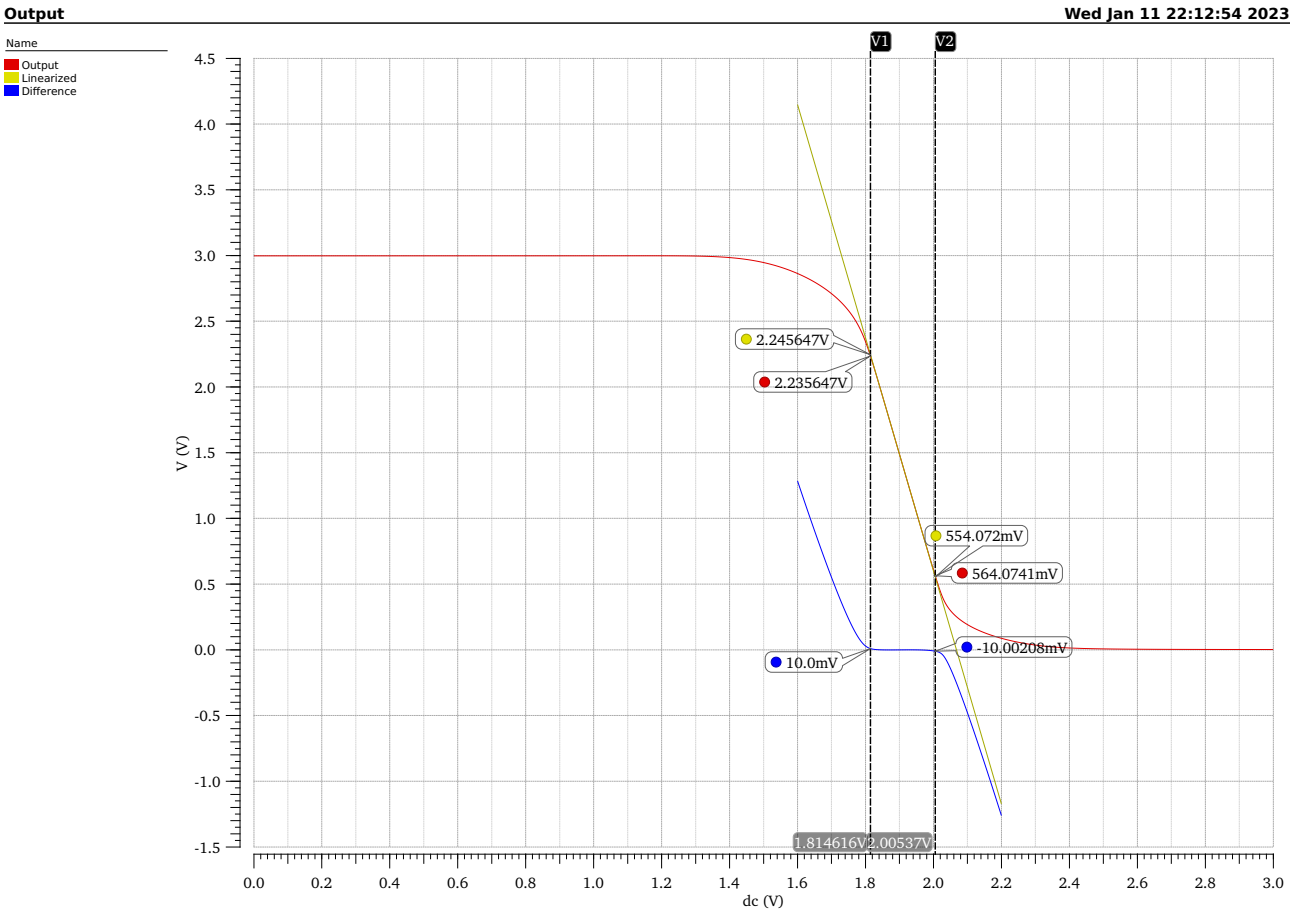

Figure 14: Output range simulation for the OTA

4. The layout

The common centroid structure with mirrored elements is used as shown in Figures 15 and 16. In addition the dummy elements were distributed around each matched set of transistor. The layout passes both DRC and LVS checks as shown in Figure 17.

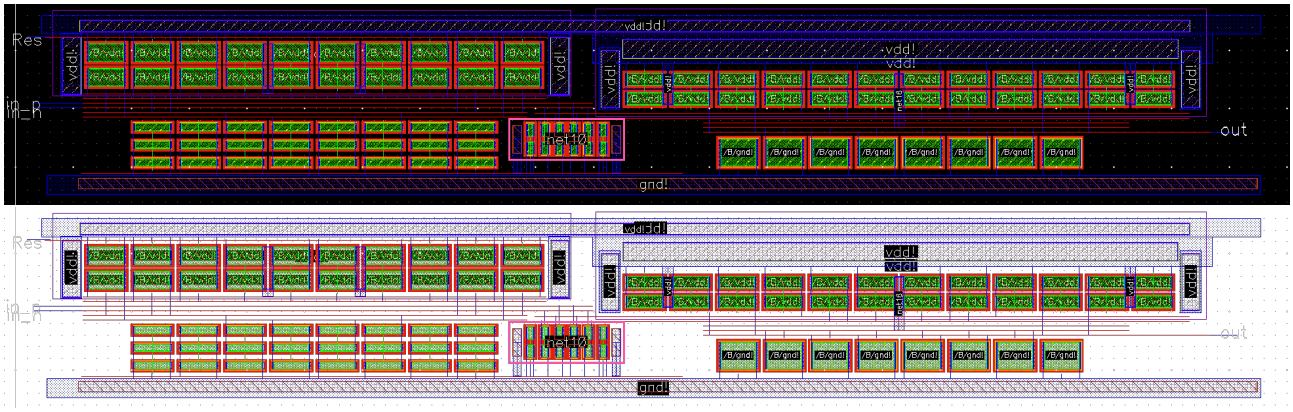

Figure 15: The full OTA layout

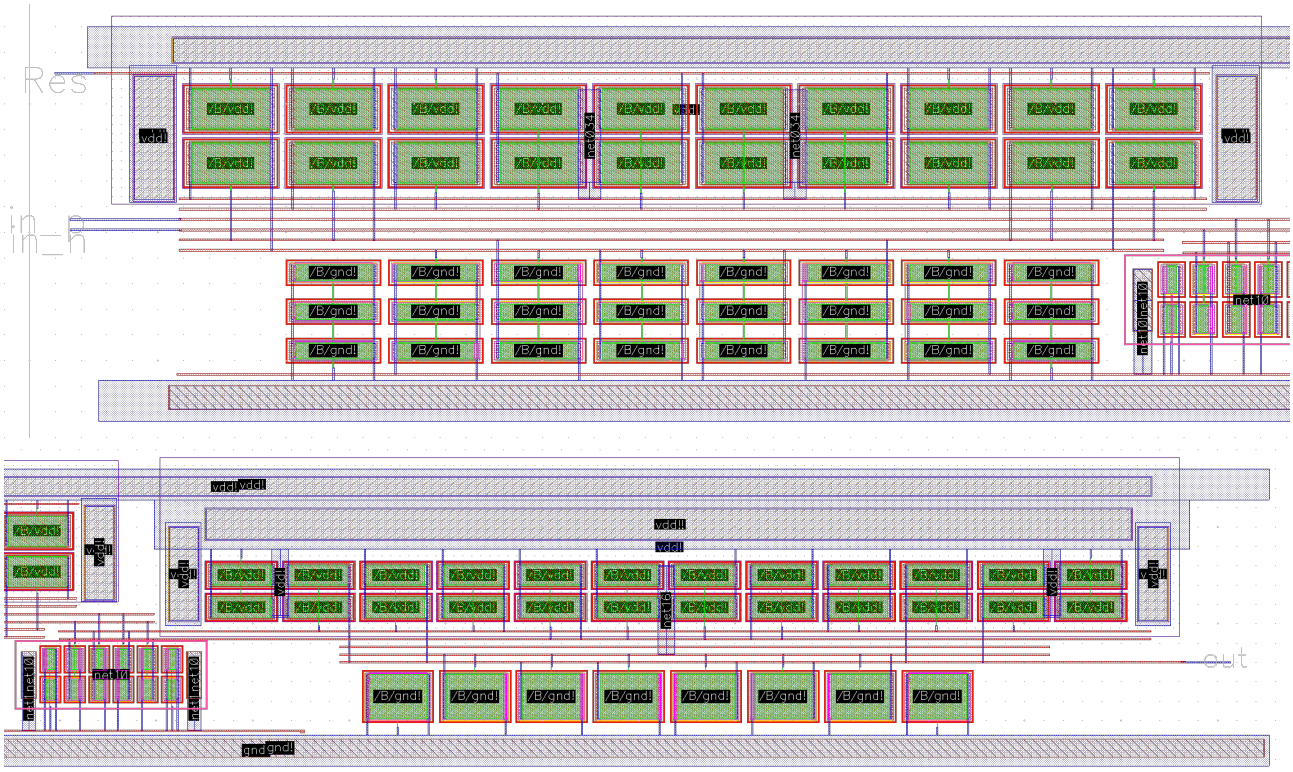

Figure 16: The partial OTA layouts

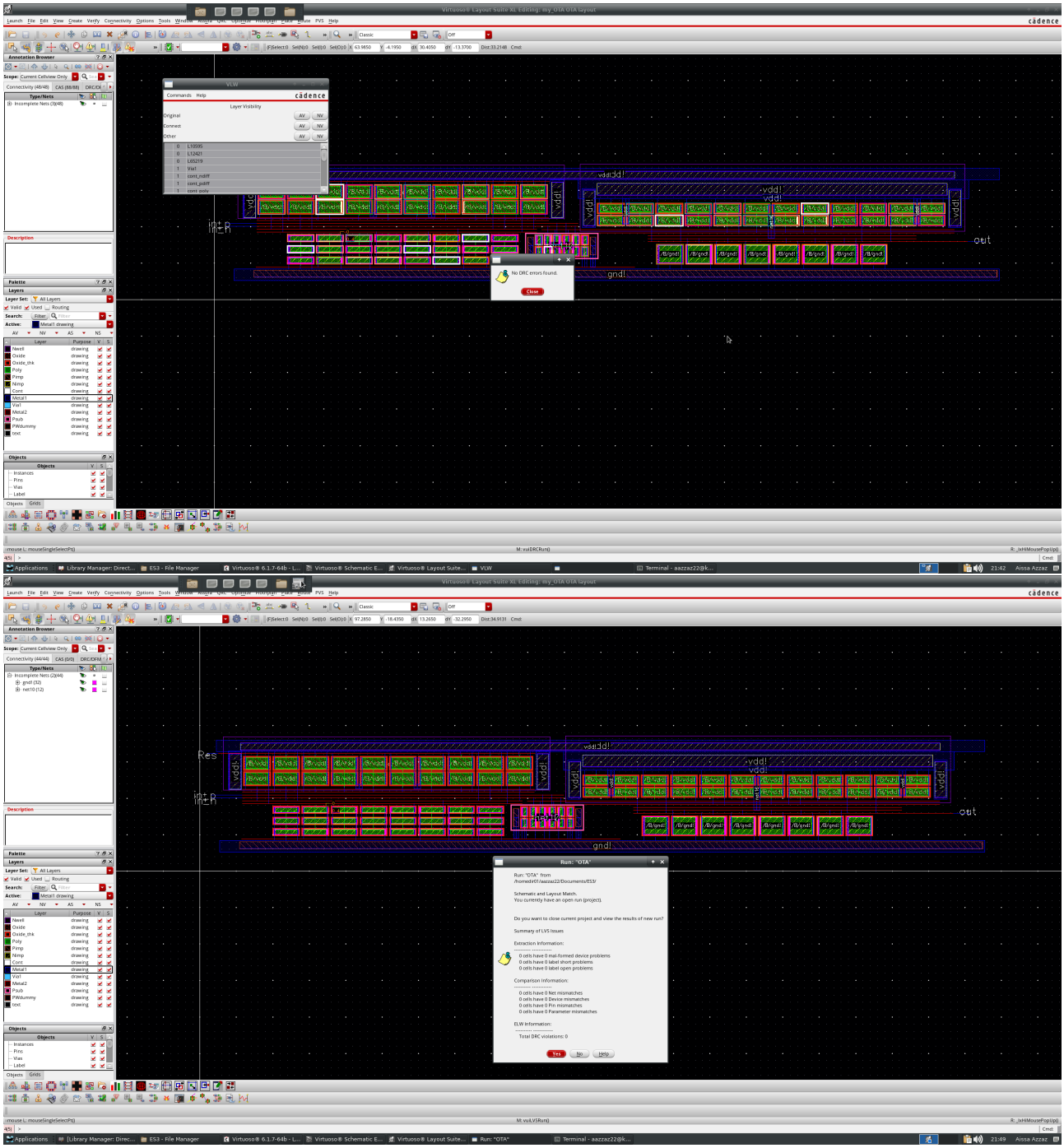

Figure 17: DRC and LVS results of the OTA layout

5. Layout Simulations

In the subsections bellow, the simulation results of schematic with the parasitics extracted from the layout are shown. The same test benches of the schematic simulations were used.

5.1 AC Response

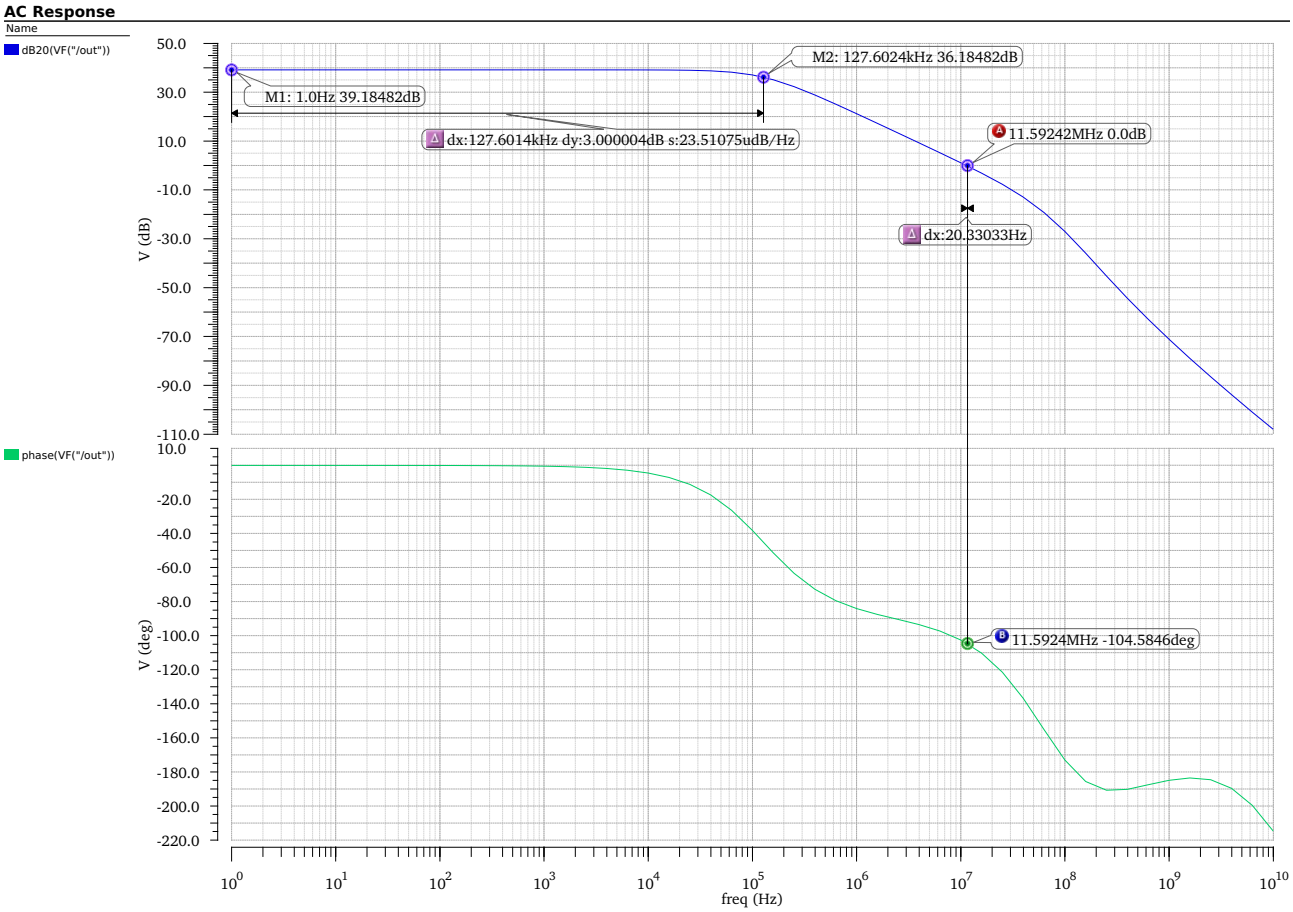

Figure 18: AC response of the OTA with the extracted parasitics

5.2 Step Response

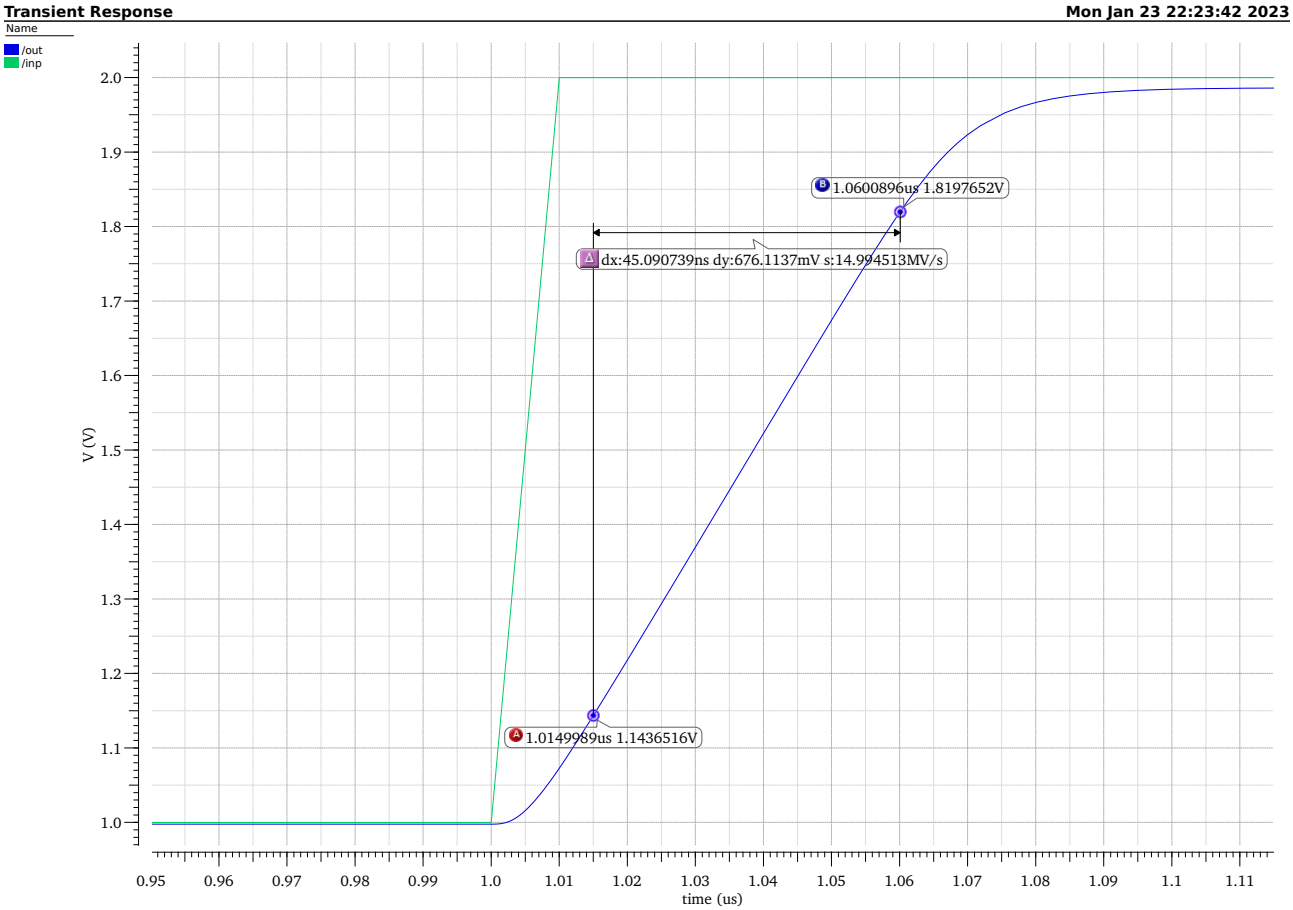

Figure 19: Step response of the OTA with the extracted parasitics

6. Comparison

Table 3 shows the AC and step response for both simulation as well as Figures 20 and 21.

In this OTA including the extracted parasitics in the simulation resulted in slightly better f_t and SR. Overall, the both results for when including the prasitics or ignoring them are almost identical.

Table 3: The results of all the simulations

	Results without prasitics	Results with prasitics
f_{ta}	11.56908 MHz	11.59242 MHz
BW	123.163 kHz	127.6024 kHz
A_0	39.48111 dB	39.48111 dB
PM	75.3938°	75.4154°
Slew Rate	14.334105 MV/s	14.994513 MV/s

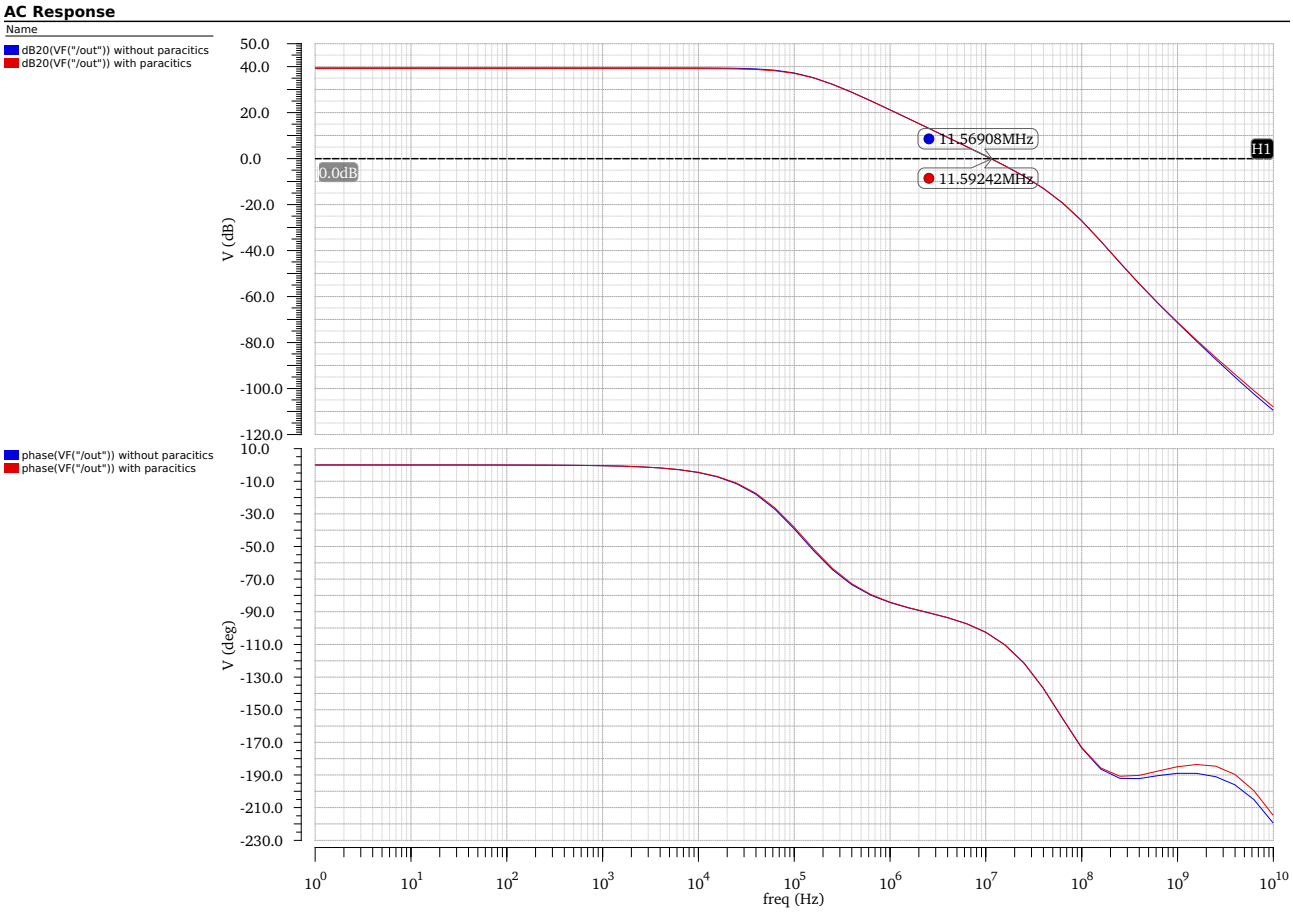

Figure 20: Comparison of the AC response of the OTA with and without the extracted parasitics

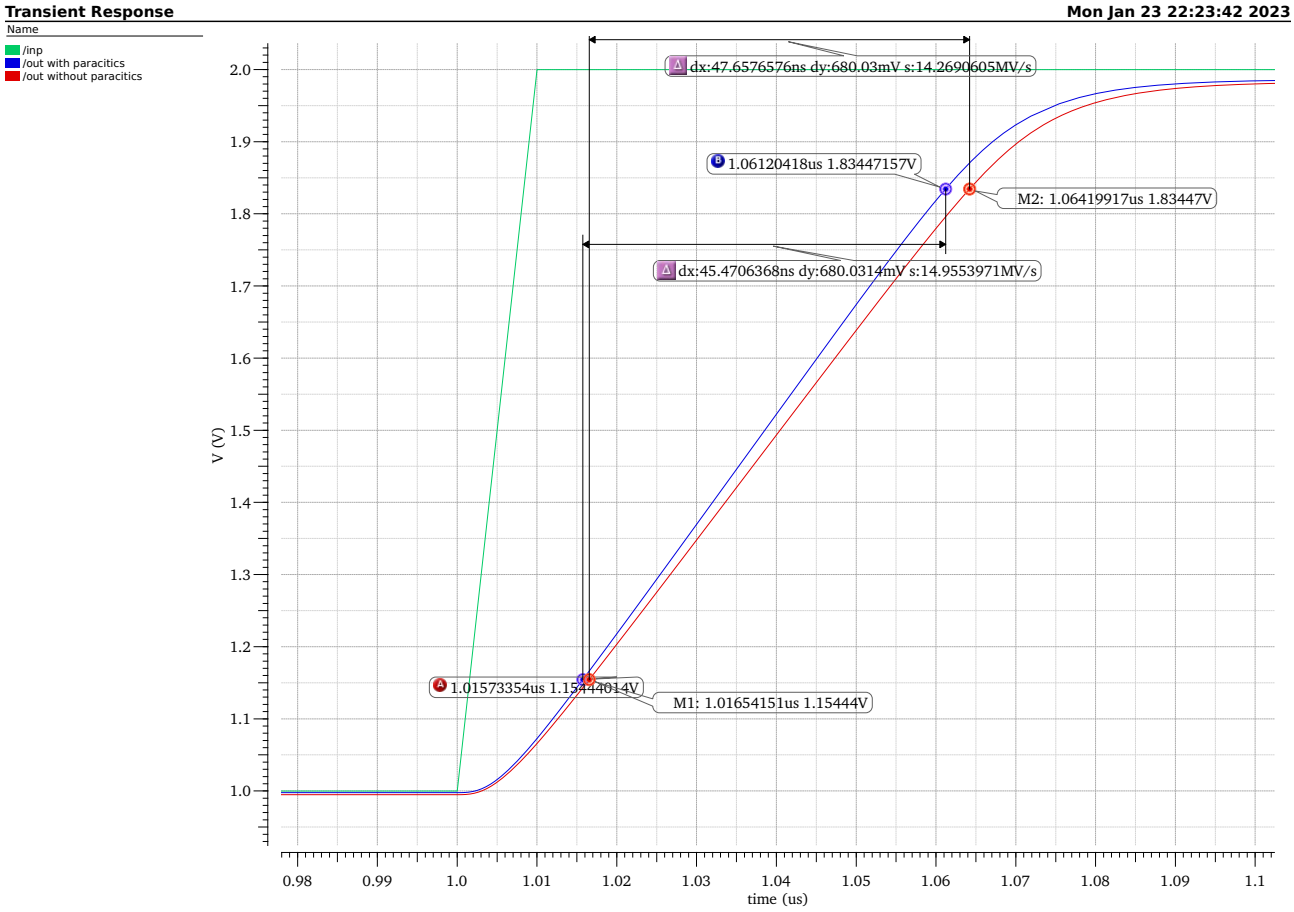

Figure 21: Comparison of the step response of the OTA with and without the extracted parasitics