DDCO Laboratory Mini_Project

Session: Aug – Dec, 2019

Design & implement a 16–bit Shift Register (serial–in, serial–out & serial–in, parallel–out).

Shift Register

Shift Register is a group of flip flops used to store multiple bits of data. The bits stored in such registers can be made to move within the registers and in/out of the registers by applying clock pulses. An n-bit shift register can be formed by connecting n flip-flops where each flip flop stores a single bit of data.
The registers which will shift the bits to left are called “Shift left registers”.
The registers which will shift the bits to right are called “Shift right registers”.

Shift registers are basically of 4 types. These are:

1. Serial In Serial Out shift register
2. Serial In parallel Out shift register
3. Parallel In Serial Out shift register
4. Parallel In parallel Out shift register

Serial In Serial Out Shift Register:

Serial In Serial Out (SISO) shift registers are a kind of shift registers where both data loading as well as data retrieval to/from the shift register occurs in serial-mode. Figure given below shows a n-bit synchronous SISO shift register sensitive to positive edge of the clock pulse. Here the data word which is to be stored is fed bit-by-bit at the input of the first flip flop. Further it is seen that the inputs of all other flip-flops (except the first flip-flop FF_1) are driven by the outputs of the preceding ones say for example, the input of FF_2 is driven by the output of FF_1. At last the data stored within the register is obtained at the output pin of the n^{th} flip-flop in serial-fashion.

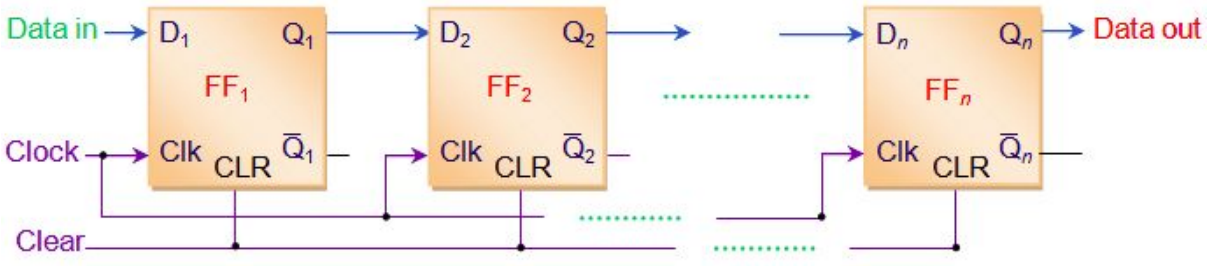

Figure 1 ***n*-bit Right-Shift Serial-in Serial-Out Shift Register**

Initially all the flip-flops in the register are cleared by applying high reset. Next the input data word is fed serially to FF_1.

This causes the bit appearing at the D_1 pin (B_1) to be stored into FF_1 as soon as the first leading edge of the clock appears. Further at the second clock tick, B_1 gets stored into FF_2 while a new bit enters into FF_1 (B_2).This kind of shift in data bits continues for every rising edge of the clock pulse. This indicates that for every single clock pulse the data within the register moves towards right by a single bit.

One can note that the first bit of an input word appears at the output of n^{th} flip-flop for the n^{th} clock tick. On applying further clock cycles, one gets the next successive bits of the input data word as the serial output

Clock Cycle	Data in	Q_1	Q_2	...	Q_n = Data out
1	B_1	B_1	0	...	0
2	B_2	B_2	B_1	...	0
3	B_3	B_3	B_2	...	0
4	B_4	B_4	B_3	...	0
5	B_5	B_5	B_4	...	0
6	B_6	B_6	B_5	...	0
.	.	.	.	...	.
.	.	.	.	...	.
.	.	.	.	...	.
n	B_n	B_n	B_{n-1}	...	B_1
n+1	B_{n+1}	B_{n+1}	B_n	...	B_2
.	.	.	.	...	.
.	.	.	.	...	.
.	.	.	.	...	.

Serial Output Bits of SISO (Right-Shift) Shift Register

Table I **Data Movement in Right-Shift SISO Shift**

Serial in parallel out shift register:

In **Serial In Parallel Out (SIPO) shift registers**, the data is stored into the register serially while it is retrieved from it in parallel-fashion. Figure 1 shows an n-bit synchronous **SIPO shift register** sensitive to positive edge of the clock pulse. Here the data word which is to be stored (Data in) is fed serially at the input of the first flip-flop (D_1 of FF_1). It is also seen that the inputs of all other flip-flops (except the first flip-flop FF_1) are driven by the outputs of the preceding ones say for example, the input of FF_2 is driven by the output of FF_1. In this kind of shift-register, the data stored within the register is obtained as a parallel-output data word (Data out) at the individual output pins of the flip-flops (Q_1 to Q_n).

The register contents are cleared by applying high on the reset(clear) pins of all the flip-flops at the initial stage. After this, the first bit, B_1 of the input data word is fed at the D_1 pin of FF_1.

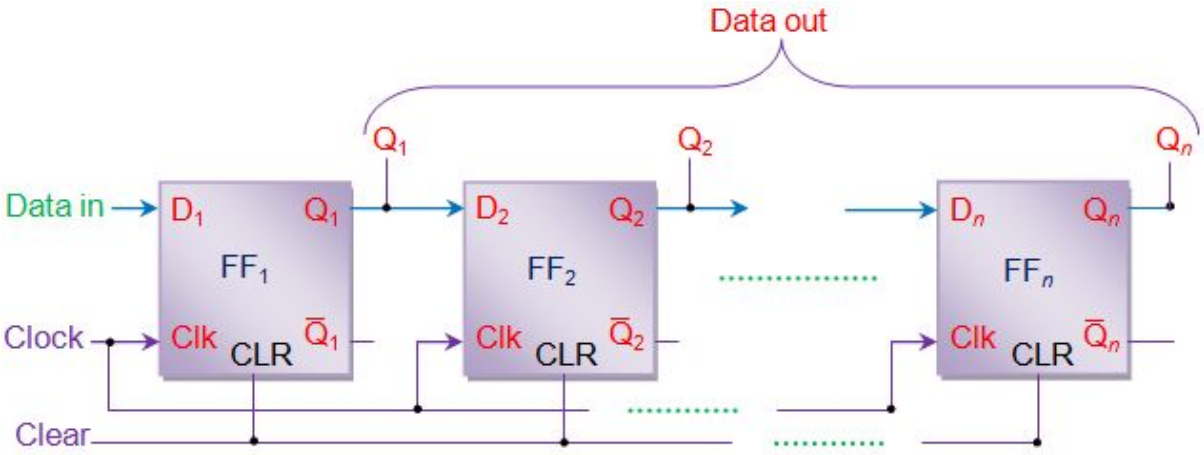

Figure 1 *n*-bit Serial-In Parallel-Out Right-Shift Shift Register

This bit (B_1) will enter into FF_1, get stored and thereby appears at its output Q_1 on the appearance of the first leading edge of the clock. Further at the second clock tick, the bit B_1 right-shifts and gets stored into FF_2 while appearing at its output pin Q_2 while a new bit, B_2 enters into FF_1. Similarly at each clock tick the data within the register moves towards right by a single bit while a new bit of the input word enters into the register. Meanwhile one can extract the bits stored within the register in parallel-fashion at the individual flip-flop outputs. One can note that the n-bit input data word is obtained as an n-bit output data word from the shift register at the rising edge of the n^{th} clock pulse.

Table I Data Movement in Right-Shift SIPO Shift Register

Clock Cycle	Data in	Q_1	Q_2	...	Q_n
1	B_1	B_1	0	...	0
2	B_2	B_2	B_1	...	0
3	B_3	B_3	B_2	...	0
4	B_4	B_4	B_3	...	0
5	B_5	B_5	B_4	...	0
6	B_6	B_6	B_5	...	0
.	.	.	.	...	.
.	.	.	.		.
.	.	.	.		.
n	B_n	B_n	B_{n-1}	...	B_1

Output of SIPO (right-shift) Shift Register