AR13 **Set 01**

Code: 13EC2003

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT, TEKKALI
(AUTONOMOUS)
II B.Tech I Semester Supplementary Examinations, January-2019
SWITCHING THEORY AND LOGIC DESIGN
(Common to EEE & ECE)

Time: 3 hours **Max. Marks: 70**

PART – A

Answer all Questions [10X1=10M]

1. a) Given that $(259)_{10} = (216)_b$, determine the Value of the base 'b'.
   b) Convert 3 BE5.D to octal.
   c) State four Boolean Postulates.
   d) Differentiate between binary and BCD adders.
   e) What are sequential logic circuits?
   f) Simplify $A + A\overline{B}$.
   g) Draw the symbol and truth table of Ex-Nor Gate.
   h) Convert gray code 101001 to binary.
   i) What is the difference between shift register and counter?
   j) Convert JK Flip-Flop to 'T' Flip-Flop.

PART – B

Answer one question from each unit [5x12=60M]

UNIT-I

2. (a) $(4500)_{10} = ?_8 = ?_2$ [3 M]
   (b) Perform 1's and 2's Complement subtraction for 10110 – 11010 . [4 M]
   (c) Represent 75_{10} and 18_{10} in BCD and add them in BCD Code. [5 M]

(OR)

3. (a) What is excess – 3 code? Explain the self complementary property of Excess – 3 code with an example. [3 M]
   (b) Explain how the counting progresses in hexadecimal and octal number systems. [4 M]
   (c) Explain error detecting and error correcting codes with examples. [5 M]

UNIT – II

4. (a) Find the dual of $(x + y)(y + \overline{z})$ and implement it using NAND gates. [4 M]
   (b) Obtain the truth table of the following functions and express each function in sum of min terms and product of max terms.
   (a) $(xy + z)(y + xz)$ (b) $\overline{y}z + wx\overline{y} + w \times \overline{z} + \overline{w} \times \overline{z}$ [8 M]

(OR)

5. (a) Simplify the following Boolean expressions to a minimum number of literals [6 M]
   (i) $xy + x(wz + w\overline{z})$
   (ii) $x\overline{y} + \overline{y}\ \overline{z} + \overline{x}\,\overline{z}$
   (iii) $(B\overline{C} + \overline{A}D)(A\overline{B}+C\overline{D})$
   (b) Find the complement of the following expressions [6 M]
   (i) $x\overline{y} + \overline{X}Y$
   (ii) $(A\overline{B} + C)\ \overline{D} + E$
   (iii) $(\overline{B}C + A\overline{D})(\overline{A}B+\overline{C}D)$

UNIT – III

6. (a) Simplify the following functions using K-maps [6 M]
   (i) f(A,B,C,D) = $\sum (2, 3, 10, 11, 12, 13, 14, 15)$
   (ii) f(A,B,C,D) = $\sum (1, 4, 5, 6, 12, 14, 15)$
   (b) Simplify the following expressions and implement them using two – level NAND gates. [6 M]
   (i) $f = A\overline{B} + ABD + AB\overline{D} + \overline{A}\,\overline{C}\,\overline{D} + \overline{A}\,B\,\overline{C}$
   (Ii) $f = BD + BC\overline{D} + A\overline{B}\,\overline{C}\,\overline{D}$

(OR)

7. (a) Minimize the following logic function using Tabulation method f(a,b,c,d) = $\sum m\,(0, 1, 2, 8, 10, 11, 14, 15)$ [6 M]
   (b) Simplify the following Boolean functions using four-variable maps. [6 M]
   (i) F = $\sum (2, 3, 10, 11, 12, 13, 14, 15)$
   (ii) F = $\sum (0, 2, 4, 5, 6, 7, 8, 10, 13, 15)$

UNIT - IV

8. (a) Design a combinational circuit with three inputs and six outputs. The output binary numbers should be the square of the input binary number. [6 M]
   (b) What is the importance of carry look ahead adder? Explain its operation for 4 – bit addition. [6 M]

(OR)

9. (a) Design an Excess-3 to BCD code converter that gives output 0000 for all invalid input combinations. [8 M]
   (b) Implement the following Boolean function with 8 x 1 multiplexer f(A,B,C,D) = $\sum m\,(0, 3, 5, 6, 8, 9, 14, 15)$ [4 M]

UNIT – V

10. (a) Draw the Circuit of SR Flip-Flop with NAND gates and explain its operation. What is the draw back in SR Flip-Flop? [6 M]
    (b) Design a synchronous BCD counter with JK Flip-Flops . [6 M]

(OR)

11. (a) Draw the Circuit schematic of an edge triggered JK Flip-Flop with active low preset and active low clear inputs using NAND gates and explain its operation with help of truth table. [6 M]
    (b) Draw the logic diagram of a 4-bit shift register with serial in parallel in, Shift left and shift right facility and explain its operation. [6 M]