AR13

CODE: 13CE3011 **SET-1**

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT, TEKKALI
(AUTONOMOUS)
III B.Tech I Semester Supplementary Examinations, March-2017
TRANSPORTATION ENGINEERING-I
(Civil Engineering)

Time: 3 Hours **Max Marks: 70**

PART-A

ANSWER ALL QUESTIONS **[1 X 10 = 10 M]**

1. a) Write any two recommendations of Jayakar Committee?
   b) List out Basic requirement of ideal Alignment ?
   c) Define Overtaking sight distance?
   d) Differentiate between "Cant" and super elevated height (E).
   e) Which IRC code is used to design of traffic signals?
   f) What is PCU and its significance?
   g) List out the Road user characteristics?
   h) What are the Causes of Road Accidents?
   i) Draw the Typical Collision Diagram at a junction?
   j) Draw the Different forms of Intersections?

PART – B

Answer one question from each unit **[5x12=60M]**

UNIT- 1

2. a) What are the different types of Road patterns? Draw the neat sketch on Road patterns? 6M
   b) With the help of neat sketches explain about various factors controlling highway alignment? 6M

(OR)

3. a) What are the objects of Highway geometric design? List the various geometric elements to be considered in highway design? 5M
   b) Explain briefly about Modal, Elemental & Functional Classification? 7M

UNIT- II

4. The speeds of overtaking and overtaken vehicles are 80 and 60 KMPH respectively. If the acceleration of the overtaking vehicle is 2.5 KMPH per second, calculate the OSD for
   a) One-Way Traffic
   b) Two – way traffic 12M

(OR)

5. Explain about Design procedure of super elevation for mixed traffic. 12M

UNIT-III

6. a) Discuss about the Different Traffic Surveys in Detail? 6M
   b) Explain about basic parameters of Traffic? 6M

(OR)

7. a) Explain the Condition Diagram and collision Diagram with neat sketch? 8M
   b) Explain the term Traffic Volume? What are the objectives of carrying out traffic Volume Studies? 4M

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UNIT-IV

8. What are the types of traffic signs? Explain various traffic signs with the help of neat sketch? 12M

(OR)

9. a) Explain the Webster's design procedure for traffic signals. 8M
   b) Differentiate between Webster's method and IRC methods of Signal Design? 4M

UNIT-V

10. a) Write down the Basic requirements of intersection at grade? 6M
    b) Write down the advantages of Traffic rotary? 6M

(OR)

11. Explain grade separated intersections and the advantages and limitations of these? 12M

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CODE: 13EE3015 **SET-1**

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT, TEKKALI
(AUTONOMOUS)
III B.Tech I Semester Supplementary Examinations, March-2017

ELECTRICAL MACHINES – III
(Electrical and Electronics Engineering)

Time: 3 Hours **Max Marks: 70**

PART-A

ANSWER ALL QUESTIONS **[1 x 10 = 10 M]**

1. a) What is the application of salient pole machine.
   b) What is the nature of armature reaction for lagging pf load
   c) What are the different methods used to be determine voltage regulation of alternator
   d) Define infinite busbar
   e) What are the conditions for parallel operation of alternator
   f) Write the characteristics infinite bus
   g) What are the different methods of starting of synchronous motor
   h) What is inverted V curves
   i) Why is a single phase induction motor not self starting
   j) Write at least two applications of AC series motor

PART-B

Answer one question from each unit **[5x12=60M]**

UNIT-I

2. a) Distinguish between distributed and concentrated windings. Also explain any one type of distributed winding employed in synchronous machines **[6M]**
   b) An 8-pole alternator has an armature with 30 slots and 8 conductors per slot. The flux per pole is 0.08 Wb and machine rotates at 750 rpm. Calculate EMF generated, if winding factor is 0.94 and all conductors in a phase are connected in series **[6M]**

(OR)

3. a) With neat sketch, describe the constructional features and operation of salient pole alternator. **[6M]**
   b) Explain about the integral slot winding and fractional slot winding. Discuss their merits and demerits. **[6M]**

UNIT-II

4. a) Give the expression for regulation of a salient pole synchronous generator. **[6M]**
   b) A 550V, 55KVA, 1-phase alternator has an effective resistance of 0.2Ω. A field current of 10 A produces an armature current of 200 A on short-circuit and an electromotive force of 450V on open circuit. calculate the full regulation with 0.8 power factor lagging **[6M]**

(OR)

5. a) Describe the method of finding regulation of given a alternator by using synchronous impedance method. **[6M]**
   b) A 1500 KVA, 6600V 3 phase star connected alternator with a resistance of 0.4 ohm and reactance of 6 ohm per phase, delivers full load current at power factor 0.8 lagging, and normal rated voltage. Estimate the terminal voltage for the same excitation and load current at 0.8 power factor leading. **[6M]**

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UNIT-III

6. a) Discuss the condition required for paralleling two synchronous generators. **[6M]**
   b) A 1500 KVA, 6600 3-phase, 8 pole, 750 rpm, synchronous generator is operating on 6000V bus bars. The synchronous reactance is 6 ohm/phase. find the synchronizing power at full load and 0.8 power factor lagging. **[6M]**

(OR)

7. a) What is synchronizing power and explain its role in load sharing during parallel operation? **[6M]**
   b) Calculate the maximum load of a 5000KVA, 1 phase alternator having an equivalent reactance of 5 ohm when connected to 6600 V bus bar, if its excitation is such that the electromotive force on open circuit would be 6000V. Find the armature current and power factor at this load. **[6M]**

UNIT-IV

8. a) Explain the construction and principle of operation of a synchronous motor? **[6M]**
   b) A 2000 V, 3-phase star-connected synchronous motor has an effective resistance and synchronous reactance per phase of 0.2 ohms and 2.2 ohms respectively. The input is 800 KW at normal voltage and induced line e.m.f is 2500 V. Calculate line current and power factor **[6M]**

(OR)

9. a) Explain the various starting methods of synchronous motor **[6M]**
   b) A 1000 HP, 6 kV, 3-phase, star connected synchronous motor has a synchronous impedance of (1.5+j16) ohms per phase. It is excited to develop an open circuit e.m.f of 5 kV. Draw the locus diagram of the current for loads up to 1250 HP with constant excitation. Determine the maximum value of the power factor. **[6M]**

UNIT-V

10. a) Explain the operation of a single phase induction motor using split phase technique **[6M]**
    b) Show that the starting torque of a single phase induction motor is zero. **[6M]**

(OR)

11. Explain why a universal motor operate both on AC and DC supply. What are the differences in construction between universal motor and DC series motor? Discuss its applications. **[12M]**

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CODE: 13ME3014 **SET-1**

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT, TEKKALI
(AUTONOMOUS)
III B.Tech I Semester Supplementary Examinations, March-2017

METAL CUTTING & MACHINE TOOLS
(Mechanical Engineering)

Time: 3 Hours **Max Marks: 70**

PART-A

ANSWER ALL QUESTIONS **[1 x 10 = 10 M]**

1. a) What are the types of chip formation?
   b) What are the major functions of cutting fluid?
   c) Write down at least four special attachments are being used in Lathe machine tool?
   d) Compare single and multiple spindle machine tools?
   e) Define slotter process?
   f) Differentiate the reaming and boring process?
   g) What are types of grinding process?
   h) Bring out few differences between generation and forming?
   i) What are special features in CNC machine?
   j) What is the need of slide ways in CNC machine?

PART-B

Answer one question from each unit **[5x12=60M]**

UNIT-I

2. a) Explain mechanism of material removal in single point cutting tool machining process? 6M
   b) Explain cutting tool geometry of single point cutting tool with neat diagram? 6M

(OR)

3. a) Describe about tool wear mechanism with neat diagram? 4M
   b) Derive the equation to find cutting forces of orthogonal cutting process with help of Merchant's circle diagram? 8M

UNIT-II

4. a) Explain various methods of taper turning methods in lathe machine tool with neat diagram? 8M
   b) Explain in detail about various thread cutting methods in lathe machine tool? 4M

(OR)

5. a) Compare capstan and turret lathe and bring out at least four basic differences. 4M
   b) Describe turret indexing mechanism in Lathe machine tool with neat diagram. 8M

UNIT-III

6.	a)	Explain power and motion transformation from motor to tool and work piece in shaper machine with neat diagram?	8M
	b)	Compare the shaper and planer processes for producing flat surfaces?	4M
		(OR)	
7.	a)	Explain types of indexing mechanism in milling machining with neat diagram?	8M
	b)	Explain the broach tool with constructional features and function with neat diagram?	4M

UNIT-IV

8.	a)	Explain about centerless grinding process with neat diagram and discuss its process parameters?	6M
	b)	Explain how to specify the grinding wheel and discuss in detail about each parameter?	6M
		(OR)	
9.	a)	Suggest a suitable process to finish the cylindrical wall of IC engine and explain the process in detail and also discuss effect of process parameters on surface finish?	6M
	b)	Explain the abrasive jet machining process with neat diagram and discuss about its process parameter?	6M

UNIT-V

10.	a)	Explain the basics construction details and special features of CNC machine with diagram?	8M
	b)	Explain the various types of CNC machine in detail?	4M
		(OR)	
11.	a)	Explain the requirement and basic features of part programming and also discuss about G –codes and M-codes	8M
	b)	Briefly explain the following terms such as linear bearings, ball screws, spindle drives and feed drives	4M

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CODE: 13EC3013 **SET-2**

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT, TEKKALI
(AUTONOMOUS)
III B.Tech I Semester Supplementary Examinations, March-2017

DIGITAL IC APPLICATIONS
(Electronics and Communication Engineering)

Time: 3 Hours **Max Marks: 70**

PART-A

ANSWER ALL QUESTIONS **[1 x 10 = 10 M]**

1. a) Draw the logic levels for TTL.
   b) Define Noise Margin of CMOS logic family.
   c) Draw the logic symbol for IC 74X157.
   d) Define parity circuits?
   e) Write behavioural VHDL code for 2x1 multiplexer.
   f) Explain the significance of dual priority encoder.
   g) Explain the operation of Decade Counter.
   h) Convert JK flip-flop to T flip-flop.
   i) Draw the basic structure of CPLD.
   j) Realize the output function of half adder using PLA.

PART-B

Answer one question from each unit **[5x12=60M]**

UNIT-I

2. a) Design a CMOS circuit for 4 input AOI gate. Draw the logic diagram and function table. 6M
   b) Explain about dynamic electrical behavior of CMOS logic family. 6M

(OR)

3. a) With neat diagram, explain the operation of two input NOR gate using TTL logic family. 6M
   b) Explain about how interfacing can be done between TTL/ CMOS with the help of diagrams. 6M

UNIT-II

4. a) Design and write a behavioural VHDL code for IC 74X138. 6M
   b) Realize and explain the operation of 16x1multiplexer using IC 74X151 6M

(OR)

5. a) Explain the operation of IC 74X148 with the help of function table. 4M
   b) Design and write a behavioural VHDL code for IC 74X85. 8M

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CODE: 13EC3013 **SET-2**

UNIT-III

6.	a)	Explain the operation of ALU and write a VHDL code for the same.	8M
	b)	Write short notes on dual priority encoder.	4M
		(OR)	
7.	a)	Design and write a VHDL code for 4-bit parallel adder/subtractor.	6M
	b)	Draw the gate level diagram for 4X4 combinational multiplier using adders.	6M

UNIT-IV

8.	a)	Design excess-3 counter using IC 74x163.	6M
	b)	Write a VHDL code for IC 74X194	6M
		(OR)	
9.	a)	Design and explain the operation of modulo-6 counter using flip-flops.	8M
	b)	Draw the gate level diagrams for different conversion of flip-flops.	4M

UNIT-V

10.	a)	Explain the logic diagram for PAL16R6.	6M
	b)	Explain about SRAM operation with timing diagrams.	6M
		(OR)	
11.	a)	Design binary to gray code converter using PAL.	6M
	b)	Design logic diagram for 8X4 diode ROM circuit for the given data 0-7.	6M

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CODE: 13CS3011

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT, TEKKALI
(AUTONOMOUS)
III B.Tech I Semester Supplementary Examinations, March-2017

COMPILER DESIGN
(COMMON TO CSE & IT)

Time: 3 Hours **Max Marks: 70**

PART-A

ANSWER ALL QUESTIONS **[1 X 10 = 10 M]**

1. a) What is the significance of grouping the phases in a compiler?
   b) Explain the reasons for separating lexical analysis from syntax analysis.
   c) What is meant by ambiguous grammar? Explain with example
   d) Distinguish between SLR & CLR parsers.
   e) What is dependency graph? What is its significance?
   f) How are the shifts reduce conflicts resolved in bottom-up parsing?
   g) Explain L-attributed definition.
   h) Explain frequency reduction with example.
   i) What is a flow graph? Explain with example.
   j) Discuss various object code forms.

PART-B

Answer one question from each unit **[5x12=60M]**

UNIT-I

2. (a) Explain the phases of compiler. [6M]
   (b) Explain various language translators (lex, yacc). [6M]

(OR)

3. (a) Write a short note on lex tool. [6 M]
   (b) Explain the boot strapping process with suitable examples and diagrams. [6 M]

UNIT-II

4. (a) Construct the predictive parser for the following grammar. [6 M]

$E \rightarrow TE^1$
$E^1 \rightarrow + TE' \mid \varepsilon$
$T \rightarrow FT^1$
$T^1 \rightarrow *FT^1 \mid \varepsilon$
$F \rightarrow (E) \mid id$

   (b) Write short notes on following. [6 M]
   i) Left Recursion (ii) Left Factoring

(OR)

5 (a) Construct SLR parsing Table for the following grammar [12 M]

$E \rightarrow E+T \mid T$
$T \rightarrow T*F \mid F$
$F \rightarrow (E) \mid id$

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UNIT-III

6	(a)	Give a translation scheme for case statement.	[6 M]
	(b)	Write short notes on various intermediate code forms.	[6 M]

(OR)

7		What is a symbol table? Explain various data structures used for implementation of symbol tables	[12M]

UNIT-IV

8	(a)	Explain various storage allocation strategies.	[6M]
	(b)	Discuss local optimization techniques.	[6M]

(OR)

9	(a)	Explain register allocation and assignment	[6M]
	(b)	Explain data flow diagram with an example.	[6M]

UNIT-V

10		Explain the induction variable elimination technique and explain with an example	[12M]

(OR)

11		What is live variable? Write algorithm for live variable analysis and explain with example	[12M]

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