CODE: 19MTE1005   **SET-1**

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT, TEKKALI
(AUTONOMOUS)
I M.Tech. I Semester Regular & Supplementary Examinations, August-2021
AIR CONDITIONING SYSTEM DESIGN
(Thermal Engineering)

Time: 3 Hours   Max Marks:60

Answer any FIVE questions
All questions carry EQUAL marks

1. a) Describe DBT, WBT, specific humidity and relative humidity properties with the help of psychometric chart.   6M
   b) Describe heating & humidification and cooling & dehumidification processes with the help of psychometric chart   6M

2. a) A winter air-conditioning system adds for humidification 0.0025 kg/s of saturated steam at 101 kPa pressure to an airflow of 0.36 kg/s. The air is initially at a temperature of 15^0C with a relative humidity of 20 percent. What are the dry and wet-bulb temperatures of the air leaving the humidifier?   6 M
   b) A laboratory space to be maintained at 24^0C and 50 percent relative humidity experiences a sensible-cooling load of 42 kW and a latent load of 18 kW. Because the latent load is heavy, the air-conditioning system is equipped for reheating the air leaving the cooling coil. The cooling coil has been selected to provide outlet air at 9^0C and 95 percent relative humidity. What is the temperature of supply air?   6 M

3. a) State all the factors that determine human comfort.   4 M
   b) Sketch 'comfort chart' and show on it the 'comfort zone'? Explain clearly the different stages of human body defense against variations of weather conditions during summer and winter.   8 M

4. a) Describe in detail the different ventilation systems used in air-conditioning plants.   6 M
   b) Explain in detail the combined supply and extraction system with neat sketch.   6 M

5. a) What are the basic elements of air-conditioning control systems? Describe each control system briefly.   4 M

    b) The inside design conditions in a space are 21^0C DB and 0.0078 kg/kg moisture content. The outside design conditions are 30^0C DB and 0.011 kg/kg moisture content. The room sensible and latent heat gains are 17.5 and 3.5 kW respectively. The design supply air temperature is 15.5^0C. The ventilation air is 25% of supply air.   8 M
        The air-conditioning plant comprises a mixing chamber, an air washer with chilled-water circulation and a reheater. A room thermostat controls the reheater and a room humidstat controls the chilled-water flow in the air washer. Calculate, under the design conditions, the state and rate of supply air, cooling load on the air washer and amount of reheat.

6. a) What are basic heat pump circuits that are commonly used? Explain each circuit briefly with a neat sketch.   8 M

    b) A heat pump is used for a residence to supply 64,000 kJ of heat per hour. The pump has a coefficient of performance of 3 when outdoor temperature is 10^0C and room temperature is maintained at 20^0C. Under these conditions, the condenser and evaporator coil temperatures are maintained at 28^0C and 5^0C. Compute (a) the power required in kW when the combined motor-compressor efficiency is 0.8 and (b) EPR of the heat pump.   4 M

7. a) Discuss the operation of different solar collectors with the help of neat sketches.   6 M

    b) Draw a neat diagram of air-conditioning system required in winter season. Explain the working of different components in the circuit. Is it possible to use the steam for such air-conditioning systems?   6 M

8. a) Describe steam injection type humidifier in detail with a neat sketch.   6 M

    b) Define the term "Effective Temperature" and explain its importance in air-conditioning system. Describe the factors which affect effective temperature.   6 M

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SET-2

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT, TEKKALI
(AUTONOMOUS)
I M.Tech. I Semester Regular & Supplementary Examinations, August-2021

MICROCONTROLLERS AND APPLICATIONS
(Power Electronics And Drives)

Time: 3 Hours   **Max Marks:60**

Answer any FIVE questions
All questions carry EQUAL marks

1.	a)	Explain RAM organization of 8051 Microcontroller with the help of a diagram.	(6M)
	b)	Discuss in brief the special function registers in 8051 microcontroller.	(6M)
2.	a)	Explain the data transfer instruction with respect to 8051microcontroller with examples.	(6M)
	b)	Discuss the addressing modes of 8051with examples.	(6M)
3.	a)	Discuss TMOD register in 8051 with examples.	(6M)
	b)	Explain the following pins with respect to 8051 microcontroller. (i) $\overline{EA}$ (ii) RST	(6M)
4.		Write an ALP for Stair Case Ramp Generator	(12M)
5.		With neat sketch explain the architecture of PIC 16C61 Micro Controller	(12M)
6.	a)	Explain the different bits of OPTION_REG Register with the help of an example in PIC 16F8XX.	(6M)
	b)	Describe the TIMERS and their features in PIC 16F8XX.	(6M)
7.	a)	Sketch the interfacing diagram of LCD with 8051and write the relevant ALP to display " MICROCONTROLLER" on the LCD display unit.	(6M)
	b)	With a neat schematic, explain the implementation of key-board interfacing with 89C51 microcontroller.	(6M)
8.	a)	Draw and explain Architectural Overview of Atmel 89C51.	(6M)
	b)	Explain the different industrial applications of microcontrollers with examples.	(6M)

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ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT, TEKKALI
(AUTONOMOUS)
I M.Tech. I Semester Regular & Supplementary Examinations, August-2021
CRYPTOGRAPHY AND NETWORK SECURITY
(Computer Science and Engineering)

Time: 3 Hours   **Max Marks:60**

Answer any FIVE questions
All questions carry EQUAL marks

1.	a)	Explain security attacks and security services.	6
	b)	Explain symmetric cipher model.	6
2.	a)	How does the permutation/expansion step in DES enhance diffusion? This is the step in which we expand by permutation and repetition the 32-bit half-block into a 48-bit half-block	6
	b)	What are the steps that go into the construction of the 16×16 S-box lookup table in AES Cryptosystem? What is rationale for the bit scrambling step that is used for finding the replacement byte that goes into each cell of the S-box table of AES Algorithm?	6
3.	a)	The necessary condition for the encryption key e is that it be coprime to the totient of the modulus. But, in practice, what is e typically set to and why? From the public key, we know the modulus n and the encryption integer e. If a bad guy could figure out the totient of the modulus, would that amount to breaking the code? Explain	6
	b)	Consider p = 7 ; q = 11, N = 77 ; Private Key d =13 Find the Public Key 'e'. Suppose the message you wish to transmit is given by m = 2, Perform Encryption and Decryption using RSA algorithm	6
4.	a)	Write about applications of cryptographic hash functions	6
	b)	Explain about message authentication requirements and functions.	6
5.	a)	How the keys are managed and distributed in PGP email security	6
	b)	What are the pros and cons of providing security at the different layers of the TCP/IP protocol stack?	6
6.	a)	How is IPSec grafted onto IPv4? The "Protocol" field of the IPv4header plays a critical role in this. How? Explain	6
	b)	What is the difference between rule-based anomaly detection and rule-based penetration identification?	6
7.	a)	What are two common techniques used to protect a password file? List and briefly define four techniques used to avoid guessable passwords.	6
	b)	What are typical phases of operation of a virus or worm?	6
8.	a)	What is the Diffie-Hellman algorithm for creating a secret session key? Explain with Example	6
	b)	Summarize the operation of Transport and Tunnel modes of AH & ESP.	6

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CODE: 19MVL1007   **SET-1**

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT, TEKKALI
(AUTONOMOUS)
I M.Tech. I Semester Regular & Supplementary Examinations, August-2021

DIGITAL SYSTEM DESIGN
(VLSI System Design)

Time: 3 Hours   **Max Marks:60**

Answer any FIVE questions
All questions carry EQUAL marks

1. a) Explain about various building blocks used in ASM Charts.   [7M]
    b) Draw the ASM chart of Binary Multiplier.   [5M]

2. a) Reduce the following state table to a minimum number of states using [8M]
        Implication chart Method shown in Table-1

Present State	Next State		Output	
	X=0	X=1	X=0	X=1
A	A	E	1	0
B	C	F	0	0
C	B	H	0	0
D	E	F	0	0
E	D	A	0	0
F	B	F	1	0
G	D	H	0	0
H	H	G	1	0

Table-1

    b) Draw the ASM chart for SR Flip-Flop.   [4M]

3.   Explain about the signature analysis and testing for bridge faults with [12M]
        suitable examples

4. a) Explain about stuck at 0 fault and stuck at 1 fault.   [6M]
    b) Explain about different fault classes and models.   [6M]

5. a) Draw the general structure of CPLD and explain   [8M]
    b) Find the successor tree for the following machine shown in table -2. [4M]

Present State	Next State, Output	
	X=0	X=1
A	C,0	D,1
B	C,0	A,1
C	A,1	B,0
D	B,0	C,1

Table -2

6.   a)   Discuss briefly about testable PLA design.   [8M]
      b)   Describe various faults that may occur in PLAs.   [4M]

7.   a)   With relevant examples distinguish between Races, Cycles and Hazards.   [6M]
      b)   What do you mean by State Reduction?   [6M]

8.   a)   Explain necessary steps involved to design full subtractor using PLA   [8M]
      b)   Differentiate between CPLD and FPGA.   [4M]

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CODE: 19MSE1014   SET-1

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT, TEKKALI
(AUTONOMOUS)
I M.Tech. I Semester Regular Examinations, August, 2021

STRUCTURAL HEALTH MONITORING
(Structural Engineering)

Time: 3 Hours   Max Marks: 60

Answer any FIVE questions
All questions carry EQUAL marks

1.	What is Structural Health Monitoring? Explain Scope of Structural Health Monitoring?	12 M
2.	Explain the causes of distress in Civil Engineering structures.	12 M
3.	Explain Static response based-method in SHM	12 M
4.	Differentiate between Non-Destructive Evaluation (NDE) and Structural Health Monitoring?	12 M
5.	Explain importance and Need of Non-Destructive Testing in SHM.	12 M
6.	Discuss about various global damage detection methods in SHM	12 M
7.	Explain the Role of Piezoelectric Sensors in Structural Health Monitoring System?	12 M
8.	Explain the Role of Smart Materials in Structural Health Monitoring System and Discuss about Active and Passive Smart Materials?	12 M

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT, TEKKALI
(AUTONOMUS)
I M.Tech. I Semester Supplementary Examinations, August-2021
DIGITAL SYSTEM DESIGN & TESTING
(VLSI System)

Time: 3 hours   **Max. Marks: 60**

Answer any Five questions
All questions carry equal marks

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1. a) Develop mealy state machine and circuit for serial adder.
    b) Draw the state diagram and logic expressions for following sequences of input and output signals

Clock cycle	t0	t1	t2	t3	t4	t5	t6	t7	t8	t9	t10
w	0	1	0	1	1	0	1	1	1	0	1
z	0	0	0	0	0	1	0	0	1	1	0

2. a) Draw the architecture of Xilinx FGPA and explain each block.
    b) Compare the CPLD and FPGA.
3. a) Explain the following types of faults:
       (i) Stuck at faults (ii) Bridge faults
    b) Implement the Lookup Table (LUT) circuit for given function using 2-input MUX.
       $f_1 = x_1'x_2'+x_1x_2$
4. a) Explain the signature analysis and testing for stuck at faults.
    b) Perform the analysis and explain the test pattern generation using PODEM algorithm.
5. a) Explain in detail about various types of fault that occur in PLAs.
    b) With an example, explain the LFSR concept.
6. a) Explain Static and Dynamic Hazards and its significant.
    b) What is clock skew? Explain positive and negative clock skew.
7. a) comparison between ROM and PLA
    b) Implement the following Boolean function using PLA:
       Sum $(A,B,Cin) = \Sigma\ m(1,2,4,5)$; Cout $(A,B, Cin) = \Sigma\ m(3,5,6,7)$
8. a) Design a combinational circuit using ROM which takes a 3-bit number and produces output as the binary equivalent of the square of the input numbers.
    b) What is HDL? Write any HDL code to binary to gray code converter circuit.

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