AR13

CODE: 13CE3011 **SET-1**

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT, TEKKALI
(AUTONOMOUS)
III B.Tech I Semester Supplementary Examination, January-2018
TRANSPORTATION ENGINEERING-I
(Civil Engineering)

Time: 3 Hours **Max Marks: 70**

PART-A

ANSWER ALL QUESTIONS **[1 x 10 = 10 M]**

1. a) What is the name of the CSIR-funded lab (located in New Delhi) focussing on research in the area of transportation engineering?
   b) Define Alignment ?
   c) What is the necessity of providing super elevation?
   d) Define skid?
   e) Define density with reference to traffic flow studies?
   f) What is a condition diagram?
   g) Draw a rough sketch of the STOP sign?
   h) Draw a rough sketch of speed limit restriction sign?
   i) What are the number of crossing conflicts at an uncontrolled 2-way 2-lane 4 road-intersection (ignoring the pedestrian crossing)
   j) What is channelisation?

PART-B

Answer one question from each unit **[5x12=60M]**

UNIT-I

2. Four new road links are to be constructed P,Q,R and S with different road lengths. Suggest the order of priority for phasing the road construction programme based on maximum utility approach. Assume the utility units as given below. 12

Population range	**Utility value**
1000-2000	0.50
2000-5000	1.00
5000-10000	1.50
>10000	2.00

Road	**Length (km)**	**No. of villages with population ranges**			
		1000-2000	**2000-5000**	**5000-10000**	**>10000**
P	300	100	80	30	6
Q	400	200	90	0	8
R	500	240	110	70	10
S	550	248	112	73	12

(OR)

3. a. Explain the obligatory points with reference to highway alignment? 6
   b. Write a brief note on Jayakar Committee's recommendations? 6

UNIT-II

4. a. Explain the elements of highway geometric design 6
   b. For a highway with design speed of 80kmph, determine the safe OSD (assume acceleration as 0.45 ms^{-2}, and reaction time = 2.0s). 6

(OR)

5. a. Explain the procedure to design the rate of super elevation? 6
   b. Find the minimum sight distance to avoid head-on collision of two cars approaching at 80kmph and 50kmph. Reaction time is 2.0s, coefficient of longitudinal friction is 0.65 and brake efficiency is 60% in either case. 6

UNIT-III

6. a. Explain O-D study? What are the uses of O-D studies? 6
   b. It is observed that on an average a vehicle driver drives 6000km during the course of the year. The probability of having an accident is 100 per 200million vehicle-kilometres. What is the probability of a driver having at least three accidents during his driving career extending to 30years? 6

(OR)

7. a. A two-lane urban road with one-way traffic has a maximum capacity of 1800 vehicles/hour. Under the jam condition, the average length occupied by the vehicles is 5.0 m. The speed versus density relationship is linear. Determine the density (in vehicles/km) for a traffic volume of 1000 vehicles/hour. 6
   b. What is a collision diagram? 6

UNIT-IV

8. a. What are traffic control devices? Explain these briefly. 6
   b. Roads 1 & 2 intersect at right angle. Road 1 has four lanes with a total width of 13.0m and Road 2 has two lanes with a total width of 7.0m. The volume of traffic approaching the intersection during the design hour are 1040 PCU/h and 850 PCU/h on the two approaches of Road 1 and 340 PCU/h and 260 PCU/h on the two approaches of Road 2. Design a two-phase traffic signal using Webster's method. 6

(OR)

9. a. What is the need for road markings? Explain about the types of road markings? 6
   b. An isolated three-phase traffic signal is designed by Webster's method. The critical flow ratio for the three phases are 0.25, 0.30 and 0.25 respectively and lost time per phase is 4 second. Determine the optimum cycle length in seconds. 6

UNIT-V

10. a. Briefly explain the various design factors that are to be considered in rotary intersection design. 6
    b. A roundabout is provided with an average entry width of 8.40m, width of weaving section as 14.0m, and length of the weaving section between channelizing islands as 35.0m. The crossing traffic and total traffic on the weaving section are 1000 PCU per hour and 2000 PCU per hour respectively. Determine the nearest rounded capacity of the roundabout (in PCU per hour)? 6

(OR)

11. a. Write a note on forms of intersections? 6
    b. When would one recommend grade separated intersections? Discuss their advantages and limitations. 6

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13EE3015 **SET-2**

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT, TEKEKALI
(AUTONOMOUS)
III B.Tech I Semester Supplementary Examination, January-2018
ELECTRICAL MACHINES-III
(Electrical & Electronics Engineering)

Time: 3 Hours **Max Marks: 70M**

PART – A **[1 x 10 = 10M]**

Answer All Questions

1. a) Write the EMF equation of an Alternator.
   b)Define winding factor.
   c)Define direct axis reactance (X_d) and quadrature axis reactance(X_q).
   d)What are the differences between MMF and EMF methods?
   e)What is the effect of varying excitation of an alternator running in parallel with other alternator?
   f)What is synchronous condenser?
   g)What could be the reasons if a 3-phase synchronous motor fails to start?
   h)What are V-Curves and inverted V curves?
   i) Write the principle of AC series motor and give its applications.
   j)Show that the starting torque of a single phase-phase induction motor is zero.

PART-B

[5x12=60M]

Answer one Question from each Unit:

UNIT – I

2. a) Discuss about the determination of synchronous reactance of an alternator. [6M]
   b). Calculate the speed and open-circuit line and phase voltages of a 4-pole,3-phase,50hz star-connected alternator with 36 slots and 30 slots 30 conductors per slot. The flux per pole is 0.05wb [6M]

(OR)

3. a) Compute the distribution factor for a 36-slot, 4-pole, single-layer 3-Phase winding. [6M]
   b) A 3-phase,16-pole alternator has the following data: number of slots=192,conductors per slot=8,coil span 10 slots; speed of alternator=375rpm;flux per pole =60mwb.calculate the phase and line voltage. [6M]

UNIT – II

4. a) Discuss in brief, how voltage regulation can be computed by ZPF method [6M]
   b) A 3-phase star-connected synchronous generator is rated at 25MVA, 11KV. the armature effective resistance and synchronous reactance are 1.2 Ω and 25Ω respectively per phase. Calculate the percentage voltage regulation for a load of 22MVA at (i) 0.8pf lagging and (ii) 0.8pf leading. also find out the pf at which the regulation becomes zero [6M]

(OR)

5. a) Discuss in brief, how voltage regulation can be computed by MMF method [6M]

   b) A synchronous generator has Xd=0.8 pu and Xq=0.625 pu. It is supplying full-load at rated voltage at 0.9 lagging power factor. Draw the phasor diagram and compute the excitation emf [6M]

UNIT – III

6. a) Describe the factors which affect the sharing of load between two alternators operating in parallel [6M]

   b) A 11MVA,3-phase,8-pole alternator runs at 750rpm in parallel with other machines on 11kV bus-bars. Find synchronizing power on full load 0.8 pf lagging per mechanical degree of displacement and the corresponding synchronizing torque. The synchronous reactance is 6 ohms per phase. [6M]

(OR)

7. a) Derive expressions for synchronizing power and synchronizing torque when two AC generators are connected in parallel. [6M]

   b) Describe with relevant diagram, dark lamp method of synchronizing two 3-phase alternators [6M]

UNIT – IV

8. a) Derive the expression for power developed in a synchronous motor, various conditions for maximum power developed [6M]

   b) List out different methods of starting a synchronous motor, explain any one in detail. [6M]

(OR)

9. A 75 kw 3phase Y connected, 50Hz,440V cylindrical rotor synchronous motor operates at rated condition with 0.8pf leading. The motor efficiency excluding field and stator losses, is 95% and Xs=2.5Ωcalculate (i) mechanical power developed (ii) armature current (iii) back emf (iv) power angle and(v)max or pull out toque of the motor. 12M

UNIT –V

10. Discuss in detail about the [6M+6M]
    a) split-phase motors,
    b) Capacitive start and run motor.

(OR)

11. **A** single phase induction motor has stator windings in space quadrature and is supplied with a single phase voltage of 230V at 50Hz. The stand still impedance of the main winding is (5.5+10.5i) and the auxiliary winding is(20.4+15.2i). find the value of capacitance to be inserted in the auxiliary winding for maximum starting torque. 12M

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CODE: 13ME3014 **SET-2**

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT, TEKKALI
(AUTONOMOUS)
III B.Tech I Semester Supplementary Examination, January-2018

METAL CUTTING & MACHINE TOOLS
(Mechanical Engineering)

Time: 3 Hours **Max Marks: 70**

PART-A

ANSWER ALL QUESTIONS **[1 X 10 = 10 M]**

1. a) What are the different types of chips obtained in metal cutting?
   b) How tool life is influenced by cutting speed.
   c) Sketch and indicate the parts on a positive rake single point tool.
   d) Sketch and describe the functions of four jaw chuck.
   e) Classify the different types of milling cutters used in machining.
   f) Explain the basic principle of gear shaping.
   g) Explain the role of adhesives in abrasive tools.
   h) How pull broaching differs from that of push broaching.
   i) List out the various sensors used in NC machine tools.
   j) Describe the concept of cutter compensation in NC.

PART-B

Answer one question from each unit **[5x12=60M]**

UNIT-I

2. (a) What is meant by BUE? Explain the format of BUE with a neat sketch. [6M]
   (b) Derive the expression for shear angle in orthogonal cutting in terms of rake angle and chip thickness ratio. [6M]

(OR)

3. (a) Explain why is it not always advisable to increase cutting speed in order to increase production rate? [6M]
   (b) Why does the temperature in cutting depend on the cutting speed, feed and depth of cut? Explain in terms of the relevant process variables [6M]

UNIT-II

4. (a) Describe the types of machining operations that can be performed on a lathe. [6M]
   (b) Explain the functions of different angles on a single point lathe cutting tool. [6M]

(OR)

5 (a) What are the types of lathes you are familiar with? Give their applications [6M]

   (b) Sketch and explain the working of a headstock on an all gear lathe machine. [6M]

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CODE: 13ME3014 **SET-2**

UNIT-III

6 (a) Sketch and explain the table feed mechanism used in shaping machine. [6M]

(b) Describe the various types of cutters used in milling operation and give an application of each. [6M]

(OR)

7 (a) Discuss the factors that contribute to broaching force and explain why they do so? [6M]

(b) Why is end milling such a versatile process? Explain with examples. [6M]

UNIT-IV

8 (a) Explain why there are so many different types and sizing of grinding wheels. [4M]

(b) What factors could contribute for chatter in grinding operation? Explain. [4M]

(c) Explain the factors involved in selecting the appropriate type of abrasive for a particular grinding operation. [4M]

(OR)

9 (a) What is honing? What are its similarities to grinding? Discuss. [4M]

(b) Explain the differences between coated and bonded abrasives. [4M]

(c) List-out the functions of grinding fluid. [4M]

UNIT-V

10 (a) Classify the machine tools based on the types of machine tool axis used in NC. [6M]

(b) What are advantages and limitations of CNC machinetools. [6M]

(OR)

11 (a) Distinguish between G and M codes used in NC programming. [6M]

(b) Write an NC program for prismatic job using canned cycles. [6M]

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CODE: 13EC3013 **SET-1**

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT, TEKKALI
(AUTONOMOUS)
III B.Tech I Semester Supplementary Examination, January-2018
DIGITAL IC APPLICATIONS
(Electronics and Communication Engineering)

Time: 3 Hours **Max Marks: 70**

PART-A

ANSWER ALL QUESTIONS **[1 X 10 = 10 M]**

1. a) What is latch up in CMOS circuits?
   b) Draw the circuit of a tri-state TTL inverter.
   c) What are FPGAs?
   d) Draw the logic diagram for 1 × 8 demultiplexer obtained using two 1 × 4 demultiplexers.
   e) State the reason for carry look ahead adder's faster speed of operation compared to ripple carry adder?
   f) What is lock-out in counters?
   g) What are the features of IC 74 × 85?
   h) How a given flip-flop is converted into another ?
   i) Why asynchronous circuits in general are faster when compared to synchronous circuits?
   j) What are the requirements to construct PROM?

PART-B

Answer one question from each unit **[5x12=60M]**

UNIT-I

2. (a) Draw the CMOS circuit diagram of tri-state buffer. Explain the circuit with the help of function table. [6M]

   (b) Design a CMOS transistor circuit that has the functional behavior as f(a) = (P + Q). (Q + R). Also explain its functional operation. [6M]

(OR)

3. (a) Draw the circuit diagram of a two-input TTL NOR gate and explain its functional behavior? [8M]

   (b) Explain the following terms with reference to CMOS logic: [4M]
   i. Logic Levels
   ii. Noise margin
   iii. Power supply rails
   iv. Propagation delay.

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CODE: 13EC3013 **SET-1**

UNIT-II

4. (a) Using two 74×151 multiplexers and an OR gate design a 16 × 1 multiplexer? [4M]
   (b) Write a VHDL program for 74×151 multiplexer. [8M]

(OR)

5 (a) Realize the following expressions using 74×138 IC? [6M]
$A(x,y,z) = \Sigma (1,2,4,6)$
$B(x,y,z) = \Sigma (0,1,6,7)$

(b) Show how the functions for binary full subtractor can be implemented using 74×138 IC and 74×00 IC. [6M]

UNIT-III

6 Write VHDL program for 1-bit comparator circuit with the input bits and equal, greater than and less than inputs from the previous stage and the outputs contain equal, greater than and less than conditions. Using this entity write VHDL program for 16-bit comparator using data flow style. Do not use any additional logic for this purpose. [12M]

.

(OR)

7 A simple floating-point encoder converts 16-bit fixed-point data using four high order bits beginning with MSB. Design the logic circuit and write VHDL data-flow program. [12M]

UNIT-IV

8 (a) Write a VHDL Entity and Architecture for a 3-bit universal shift register. [6M]
(b) Design a switch debouncer circuit using 74×109 IC. Explain its operation using timing diagram. [6M]

(OR)

9 Design a synchronous counter to count in the sequence 1,3,5,7,0,1,3,5,7,0… using 74×74 ICs. [12M]

UNIT-V

10 List the PAL programming table for BCD-to-excess-3 code converter and draw the corresponding PAL circuit. [12M]

(OR)

11 Realize a 3-bit squaring circuit using a suitable size ROM. Eg. For the number 101 at the input, the circuit has to produce an output of 11001. [12M]

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CODE: 13CS3011 **SET 1**

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT, TEKKALI
(AUTONOMOUS)

III B.Tech I Semester Supplementary Examination, January-2018

COMPILER DESIGN
(Common to CSE & IT)

PART-A

ANSWER ALL QUESTIONS **[1 X 10 = 10M]**

1. a) What is a compiler?
   b) What is a symbol table?
   c) Define a context free grammar
   d) List the properties of LR Parser
   e)What is a sentinel? What is its usage?
   f) Define Peephole optimization
   g) What is an activation record?
   h) What are applications of DAG?
   i) Specify the standard storage allocation strategies
   j) What is a three address code?

PART – B

Answer one question from each unit **[5 X 12 = 60M]**

UNIT – I

2. (a)List and explain the phases of compiler with neat sketch. [8M]
   (b) Discuss about lexical analyzer generator. [4M]

(OR)

3. (a) Define lexeme, token and pattern. Identify the lexemes that make up the tokens in the following program segment. Indicate corresponding token and pattern. [6M]

```
void swap(int i, int j)
{
int t;
t=i;
i=j;
j=t;
}
```

(b) Explain in detail the data structures in compilation. [6M]

UNIT- II

4. (a) Construct a predictive parsing table for the grammar given below [12M]

   $E \rightarrow TE^1$

   $E' \rightarrow +\ TE^1 \mid \varepsilon$

   $T \rightarrow FT^1$

   $T' \rightarrow *FT^1 \mid \varepsilon$

   $F \rightarrow (E) \mid id$

. Verify whether the input string id + id * id is accepted by the grammar or not

(OR)

5. (a) Compare bottom up approaches of parsing with all top down approaches. [6M]
   b) Construct a predictive parsing table for the grammar [6M]

   $E \rightarrow E + T \mid T$

   $T \rightarrow T * F \mid F$

   $F \rightarrow (E) \mid id$

UNIT - III

6. (a) Give the representations in quadruples, triples and indirect triples for the assignment statement given below a- b + c * d [6M]

(b) Explain the specification of simple type checker. [6M]

(OR)

7. (a) Construct the syntax tree and postfix notation for the expression (a+ (b*c)) + d-e / (f+g). [6M]

(b) Discuss in detail about the run time storage arrangement. [6M]

UNIT - IV

8. (a) What is a flow graph? Explain how a given program can be converted into a flow graph [6M]

(b) Distinguish between local optimization and global optimization. [6M]

(OR)

9. (a) What is a DAG? Explain its applications. [6M]

(b) Briefly explain copy propagation. [6M]

UNIT - V

10. (a) Discuss about machine dependent cod optimization. [6M]

(b) Explain about register allocation and assignment. [6M]

(OR)

11. (a) Explain the concept of object code forms. [6M]

(b) Discuss about DAG for register allocation. [6M]