CODE: 16CE3013 SET-2

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT, TEKKALI (AUTONOMOUS)

III B.Tech I Semester Supplementary Examinations, January-2020

DESIGN OF CONCRETE STRUCTURES (Civil Engineering)

Time: 3 Hours Max Marks: 70

Answer ONE Question from each Unit
All Questions Carry Equal Marks
All parts of the Question must be answered at one place

UNIT-I

- 1. a) Derive the expression for limiting moment of resistance of singly reinforced balanced section.
 - b) Write about design philosophies used in the design of RC structures.

7M

(OR)

2. A singly reinforced concrete beam has a width 250mm and over all depth 550 14M mm with a clear cover of 50mm is reinforced with 5 bars of 20mm diameter. Find the flexural strength and hence the safe u.d.l on the simply supported beam of span 5m.UseM30 concrete and Fe 415 steel.

UNIT-II

3. Design for flexure and shear, a rectangular beam of cross section 300mmx500mm 14M with an effective span of 7m Width of the support on each side shall be 300mm. The superimposed load on the beam is 50KN/m. use M25 concrete and Fe415steel. Calculate the reinforcement at mid span section. And find minimum and maximum shear zones. Draw the reinforcement details accordingly.

(OR)

4. A-T beam has flange dimensions of 1100×120mm. The width of rib is 250mm 14M and rib depth is 350mm. If the beam is reinforced with 2000 mm² of steel intension zone with an effective cover of 40mm, determine the maximum allowable u.d.l inclusive of self weight over a simply supported span of 6m. M25 grade concrete and Fe415 steel is used

UNIT-III

5. A simply supported slab is resting on 230 mm thick masonry walls on all four 14M sides. If the room dimensions are 4.0 m x 6.0 m, design the slab for live load 2 KN/m2 and floor finishes 1.0 KN/m2. Use M25 grade concrete and Fe415 grade steel and also sketch the reinforcement details. Assume corners are held down.

(OR)

6. Design the slab for a hall has internal dimensions of 12 m × 4 m .the slab 14M supported by 230 mm wide beams with 4 m centre to centre having a live load of 3.5 KN/m² and floor finish of 1KN/m².Consider concrete of grade M20 and HYSD steel of grade Fe500. The thickness of brick masonry walls is 300mm.Draw reinforcement detail

UNIT-IV

7. Design a square column of size 400 mmx 400 mm carrying a factored load of 14M 1200KN and the factored moments $M_{\text{ux}}=150 \text{KN-m}$ and $M_{\text{uy}}=170 \text{KN-m}$. Take the moments due to minimum eccentricities are less than the applied moments . Use $f_{\text{ck}}=20 \text{N/mm}^2$ and $f_{\text{y}}=415 \text{N/mm}$.

(OR)

8. Design a R.C. Circular column section to carry a characteristic load of 1500 14M kN.Provide spiral reinforcement as transverse reinforcement. Adopt M20 concrete and Fe-415 steel.

UNIT-V

9. Design a rectangular isolated footing of a column of size 400×600 mm carrying 14M an axial service load of 1100KN. The safe bearing capacity of the soil at the site is 200kN/m². Use M20 grade concrete mix and steel of grade Fe415.

(OR)

10. Design an isolated footing for a reinforced concrete column of size 500×500 14M mm transfers an axial load of 900 KN and a moment of 150 kN m about the major axis. The safe bearing capacity of the soils 200kN/m² and the materials to be used are M20grade concrete and use steel grade Fe415

2 of 2

CODE: 16EE3016 SET-2

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT, TEKKALI (AUTONOMOUS)

III B.Tech I Semester Supplementary Examinations, January-2020

POWER ELECTRONICS

(Electrical and Electronics Engineering)

Time: 3 Hours

Max Marks: 70

Answer ONE Question from each Unit
All Questions Carry Equal Marks
All parts of the Question must be answered at one place

UNIT-I

UNIT-II

- 3. a) A single phase half wave controlled rectifier is operated from a 120V,50Hz supply. 7M Load resistance, R=10Ω.If the average output voltage is 25% of the maximum possible average output voltage, Determine

 (i)Firing angle (ii)RMS and average output currents
 (iii)Average and RMS SCR currents.

 b) Describe the working of single phase fully controlled bridge rectifier in the following two modes

 (i)Rectifying mode
 (ii)Inversion mode

 Also sketch the load voltage and current waveforms for α=45° and α=120°.

 (OR)
- 4. a) Derive the expression for average output voltage and input power factor of single 7M phase fully controlled bridge rectifier with R load.
 - b) Explain the effect of freewheeling diode in detail. Also justify the statement 7M "freewheeling diode improves the power factor of the system".

UNIT-III

5. a) For a three phase thyristor controlled half wave rectifier with resistive load, show that 7M the average output voltage is given by

$$V_{DC} - \frac{3\sqrt{3}}{2\pi} V_{m} \cos\alpha, \quad \text{for } 0 < \alpha < \frac{\pi}{6} \quad \text{and} \quad$$

$$V_{DC} = \frac{3}{2\pi} V_{m} \left[1 + \cos \left(\alpha + \frac{\pi}{6} \right) \right] \quad , \quad \text{for } \frac{\pi}{6} < \alpha < \frac{5\pi}{6}$$

b) A three phase full bridge converter is fed from a delta-star transformer and it is 7M connected to a RL load with ripple current 15A at firing angle 45°. It is fed from 440V,50Hz AC supply, determine rectification efficiency, transformer utilization factor and input power factor.

(OR)

- 6. a) Draw the circuit diagram of three phase half wave controlled rectifier with RL load and 7M explain its operating principle with voltage and current waveforms.
 - b) A single phase dual converter operates in the circulating current mode when per phase 7M rms voltage is 220V,50Hz and L=20mH with firing angle α =45⁰.
 - (i) Find the expression for average output voltage as function of α .
 - (ii) Find the average output voltage for constant load current(I_{dc})=3Amp

UNIT-IV

- 7. a) Draw the circuit diagram of single phase full wave ac voltage controller with RL load 7M and explain its working principle with waveforms.
 - b) A single phase full wave ac voltage controller is connected with a load of $R=5\Omega$ with an input voltage of 230V,50Hz. When the firing angle of thyristor is 60° , determine the rms output voltage ,power output at load and input power factor.

(OR)

- 8. a) What is cyclo converter? What are the types of cyclo converters? List-out any two 7M applications of cyclo converters.
 - b) Describe the basic principle of working of a single phase to single phase bridge type

 7M

 cyclo converter for discontinuous conductions with the relation

 Mark the conduction of various thyristors also

UNIT-V

- 9. a) Explain the principle of operation buck convertor with the help of waveforms. 7M
 - b) Draw the circuit diagram of a single-phase full bridge voltage source inverter and 7M explain its operating principle with R load.

(OR)

- 10. a) A step down DC chopper has a resistive load of $R=15\Omega$ and input voltage 7M $V_{dc}=200V$. When the chopper remains ON, its voltage drop is 2.5V. The chopper frequency is 1KHz.If the duty cycle is 50%, determine,
 - (i) Average output voltage (ii) RMS output voltage
 - (ii) Chopper efficiency
 - b) Discuss the operating principle of a three-phase bridge inverter with a suitable 7M diagram when each semiconductor switch conducts for 180⁰.

CODE: 16EC3017 SET-1 ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT, TEKKALI (AUTONOMOUS)

III B.Tech I Semester Supplementary Examinations, January-2020 **DIGITAL IC APPLICATIONS**

(Electronics and Communication Engineering)

Time: 3 Hours Max Marks: 70

Answer ONE Question from each Unit All Questions Carry Equal Marks All parts of the Question must be answered at one place

		<u>UNIT-I</u>	
1.	a)	Explain how CMOS can be used as an inverter and give its transfer characteristic curve.	7M
	b)	Show the CMOS circuit diagram for two input NOR gate and explain its operation with function table.	7M
		(OR)	
2.	a)	Explain the basic circuit operation of ECL OR/NOR with neat diagram and truth table.	7M
	b)	With neat sketches, explain about TTL with CMOS interfacing.	7M
		<u>UNIT-II</u>	
2	a)	Design 16X1 multiplexer using IC 74X151.	7M
3.	b)	Write dataflow VHDL modelling for Priority encoder.	7 M
		(OR)	
4.	a)	Design 16- bit comparator using IC 74x85.	7M
	b)	Write dataflow modelling for 1x8 demultiplexer.	7M
		<u>UNIT-III</u>	
5.	a)	Design 24-bit binary adder using 74x283 ICs.	7M
	b)	Write structural VHDL program for 4-bit Ripple adder/subtractor.	7M
		(OR)	
6.	a)	Explain the functionality of combinational multipliers with logic diagram.	7 M
	b)	What is meant by ALU and give HDL modelling for 4-bit ALU	7 M
		<u>UNIT-IV</u>	
7.	a)	Convert JK flip-flop to SR and D flip-flops and give its necessary diagrams.	7M
	b)	Design MOD-9 synchronous counter using JK flip-flops.	7M
		(OR)	
8.		Design 4-bit Excess-3 UP/DOWN_L counter using D flip-flops and write	14 M
		behavioural VHDL modelling for the same.	
		<u>UNIT-V</u>	
9.	a)	Draw the basic structure of FPGA and explain each block of it with suitable	7M
		diagrams.	
	b)	Explain the basic structure of PROM with example.	7M
		(OR)	
10.		Implement the given functions $A(X,Y,Z)=\sum m(2,4,6,7)$; $B(X,Y,Z)=\sum m(1,3,6,7)$ using PLA and PAL.	14M

CODE: 16CS3013 SET-2

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT, TEKKALI (AUTONOMOUS)

III B.Tech I Semester Supplementary Examinations, January-2020 SOFTWARE ENGINEERING (Common to CSE & IT)

Time: 3 Hours Max Marks: 70

Answer ONE Question from each Unit
All Questions Carry Equal Marks
All parts of the Question must be answered at one place

UNIT-I

1.	Exp	lain in detail about software process model with a neat diagram	(14M)					
•	`	(OR)	(73.6)					
2.	a)	What is CMMI in software engineering?	(7M)					
	b)	What are software myths?	(7M)					
<u>UNIT-II</u>								
3.	a)	Write a short note on user requirements.	(7M)					
٥.	b)	Write a short note on system requirements.	(7M)					
	0)	(OR)	(7111)					
4.	a)	Discuss about context model.	(7M)					
	b)	What are behavioural models?	(7M)					
		<u>UNIT-III</u>						
5.	a)	Briefly explain software design process.	(7M)					
	b)	Discuss design quality.	(7M)					
		(OR)						
6.	a)	Explain any one software architectural styles.	(7M)					
	b)	Illustrate interface design steps.	(7M)					
UNIT-IV								
7.	Exp	lain in detail various testing strategies.	(14M)					
		(OR)						
8.	a)	Discuss metrics for testing.	(7M)					
	b)	What are metrics for maintenance?	(7M)					
		<u>UNIT-V</u>						
			(M3. E)					
9.	a)	What is risk projection?	(7M)					
	b)	Discuss risk refinement.	(7M)					
10	۵)	(OR) What is Software Quality Assurance (SQA)?	(7NA)					
10.	a) b)	What is Software Quality Assurance (SQA)? Discuss briefly about software reliability.	(7M) (7M)					
	U)	Discuss offerry about software renability.	(/1/1)					

1 of 1 ***

CODE: 13EC3013 SET-1

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT, TEKKALI (AUTONOMOUS)

III B.Tech I Semester Supplementary Examinations, January-2020 DIGITAL IC APPLICATIONS

(Electronics and Communication Engineering)

Max Marks: 70

Time: 3 Hours

Time: 3	Hou	irs Max Marks: 70)
		PART-A	
ANSWE	RAI	LL QUESTIONS	
1.	a)	74VHCTXX series belongs to which logic family	
	b)	Draw the circuit diagram of 2 input AND gate using Diode Logic	
	c)	What is the importance of cascading inputs in 74x85	
	d)	Which IC acts as a 2 Input, 4 Bit Multiplexer	
	e)	Which type of Adder is used in IC 74x381	
	f)	Which type of shifter has to be used for dividing the given binary data by 2	
	g)	What do you mean by Clock Skew	
		· · · · · · · · · · · · · · · · · · ·	
	h)	Why Asynchronous Counter works slower than Synchronous Counter.	
	i)	Mention any one advantage of PLDs	
	j)	Draw the circuit diagram of 1Bit DRAM Cell	
		PART-B	
Answer	one q	uestion from each unit	[5x12=60M]
		<u>UNIT-I</u>	
2.	a.	Design a CMOS 4-input OR-AND-INVERT gate and explain its Operation with function	[7M]
		table	
	b.	Explain about Power Consumption in CMOS	[5M]
		(\mathbf{OR})	
3.	a.	Draw the circuit diagram of two-input ECL OR/NOR gate and explain its Operation with	[6M]
-		the help of Functional Table	[]
	b.	Analyse the resistive model of a CMOS inverter for Non Ideal Inputs	[6M]
	υ.	UNIT-II	[OIVI]
1	0	Design a 32x1 Multiplexer using 74x151 and 74x139	[6M]
4.	a.		[6M]
	b.	Write the VHDL Code for 74x151 using Selected Signal Assignment Statement	[6M]
_		(\mathbf{OR})	553.63
5.	a.	Design a De-multiplexer using 74x138	[5M]
	b.	Design a 4 Bit Parity Generator and write the VHDL code for the same in Structural	[7M]
		Modelling.	
		<u>UNIT-III</u>	
6.	a.	Write the VHDL code for Floating Point Encoder in Behavioural Modelling	[5M]
	b.	Draw the logic diagram of 4 Bit Ripple Carry Adder and write the VHDL code for the	[7M]
		same in Structural Modelling.	
		(OR)	
7.	a.	Write the VHDL code to perform 2x2 Bit Multiplication using logic gates and adders	[6M]
	b.	Write the VHDL code for performing 8 bit circular left shift operation using case	[6M]
		statement	
		UNIT-IV	
8.	a.	Write the VHDL code for 74x74 in Behavioural Modelling	[6M]
0.	b.	Design a Serial In Parallel out Shift Register using 74x74 and Write the VHDL Code for	[6M]
	υ.	the same in Structural Modelling	[OIVI]
		(OR)	
0			[CM]
9.	a.	Write the VHDL Code for 74x163 in Behavioural Modelling	[6M]
	b.	Design a Mod-100 Counter using 74x163	[6M]
10		<u>UNIT-V</u>	543.63
10.		What are the differences between CPLD and FPGA	[4M]
	b.	Design an 8x8 diode PROM using 74x138 for the following data Starting from the First	[8M]
		Location 11,24,A5,05,C2,73,DB,52	
		(OR)	
11.	a.	Define the timing parameters for Write Operations in a RAM with Timing Diagram	[7M]
	b.	Using PLA logic, implement the following Boolean Expressions	[5M]
		E AD', AC'	

 F_1 =AB'+AC' F_2 =AC+BC