AR16

CODE: 16MTE1012 **SET-1**

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT, TEKKALI
(AUTONOMOUS)
I M.Tech. II Semester Regular & Supplementary Examinations, June-2019

ENERGY MANAGEMENT
(Thermal Engineering)

Time: 3 Hours Max Marks:60

Answer any FIVE questions
All questions carry EQUAL marks

1.	(a)	How audit planning is done in energy management Program?	6 M
	(b)	Explain about organizational structure in energy management program?	6 M
2.	(a)	Explain the basic components of an energy audit.	6 M
	(b)	Explain about the physical and operational data gathering to be done in energy auditing?	6 M
3.	(a)	Explain about the tools commonly needed for energy audits?	6 M
	(b)	Discuss about the post audit analysis?	6 M
4.	(a)	Briefly explain the technologies for energy conservation?	6 M
	(b)	Explain about energy flow networks?	6 M
5.	(a)	What are the general characteristics of Capital Investments?	6 M
	(b)	What is Modified Accelerated Cost Recovery System. Explain in brief?	6 M
6.	(a)	Discuss about time value of money concepts?	6 M
	(b)	Explain about the capital investment cost categories?	6 M
7.	(a)	Explain about the need of an Energy consultant?	6 M
	(b)	Explain the various methods of evaluation of Projects?	6 M
8.	(a)	Explain the various types of solar collectors?	6 M
	(b)	Draw a typical diagram of a wind energy conversion system with storage and explain its important features?	6 M

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CODE: 16MPE1010 **SET-1**

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT, TEKKALI
(AUTONOMOUS)

I M.Tech. II Semester Regular & Supplementary Examinations, June-2019
POWER ELECTRONIC CONTROL OF AC DRIVES
(PED)

Time: 3 Hours Max Marks:60

Answer any FIVE questions
All questions carry EQUAL marks

1.	(a)	Explain Open Loop Volts / Hertz method in Voltage Fed Inverter Control of induction motor.	6 Marks
	(b)	Explain Voltage Fed Current regulated Inverter induction motor Drive with torque and Flux Control	6 Marks
2.		Explain Static Scherbius Drive of Induction Motor Drives in detail with neat sketches and their mode of operation	12 Marks
3		What is Vector Control Explain in detail at least 2 cases the Principle of Vector Control of Induction Motor	12 Marks
4		Explain load Commutated Inverter Fed synchronous machine for Motoring and Regeneration with Corresponding Phasor Diagram	12 Marks
5.	(a)	Explain about Permanent Magnets and their characteristics	6 Marks
	(b)	Explain the Vector Control of PM Synchronous Machine with necessary Phasor diagrams and block Diagrams	6 Marks
6.	(a)	Explain the Operation of Variable Reluctance Motor and also Explain the Torque production of the Variable Reluctance Motor	6 Marks
	(b)	Explain the Current Control Variable Reluctance Motor Servo Drive	6 Marks
7.		Explain the modelling of PMSM machine	12 Marks
8.		Explain the Static Kramers Drive in detail Induction Motor Drives in detail with neat sketches	12 Marks

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CODE: 16MCS1011 **SET-2**

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT, TEKKALI
(AUTONOMOUS)
I M.Tech. II Semester Regular & Supplementary Examinations, June-2019

SOFTWARE ENGINEERING
(Computer Science and Engineering)

Time: 3 Hours Max Marks:60

Answer any FIVE questions
All questions carry EQUAL marks

1.	(a)	Explain Incremental process models	6
	(b)	Explain about Capability Maturity Model Integration (CMMI).	6
2.	(a)	Explain the value of a good SRS with real time example	6
	(b)	Explain Design process and Design quality	6
3.	(a)	List and explain interface design steps	6
	(b)	How do you evaluate the architectures? Explain	6
4.	(a)	Explain about Risk refinement	6
	(b)	Discuss Performing User interface design	6
5.	(a)	Compare different types of testing methods. Explain with an example	6
	(b)	Explain about Black-Box and White -Box testing	6
6.	(a)	Explain software risks	6
	(b)	Explain - A software reengineering process model	6
7.	(a)	Explain Software Reliability	6
	(b)	Explain the RMMM plan	6
8.	(a)	Differentiate between black box and white box testing	6
	(b)	Give the different testing metrics	6

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CODE: 16MSE1012 **SET-1**

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT, TEKKALI
(AUTONOMOUS)
I M.Tech. II Semester Regular & Supplementary Examinations, June-2019

COMPUTER APPLICATIONS AND CAD
(Structural Engineering)

Time: 3 Hours Max Marks:60

Answer any FIVE questions
All questions carry EQUAL marks

1.	Discuss the main difference between conventional and CAD design. Also write the benefits of CAD design	12 M
2.	Explain the working principle of the a) Cursor controlled devises b) Plotters	12 M
3.	Write a detailed note on the screen management. Also discuss the procedure involved in menu handling	12 M
4.	Discuss the following in brief a) Transformation b) Computer aided drafting	12 M
5.	Write a detailed algorithm for the simply supported beam with uniformly distributed load	12 M
6.	With suitable programming explain the analysis of the cantilever beam with the application of point load	12 M
7.	Discuss the stiffness properties of the members with suitable examples	12 M
8.	Explain the following a) Jointed trusses b) Rigid jointed plane frames	12 M

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CODE: 16MVL1010 **SET-1**

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT, TEKKALI
(AUTONOMOUS)
I M.Tech. II Semester Supplementary Examinations, June-2019

ALGORITHMS FOR VLSI DESIGN AUTOMATION
(VLSI System Design)

Time: 3 Hours Max Marks:60

Answer any FIVE questions
All questions carry EQUAL marks

1.	(a)	Discuss briefly about IC Design flow using VLSI Design Automation tools.	7M
	(b)	Define tractable and intractable problems in design automation.	5M
2.	(a)	Write short note on computational complexity of VLSI Design automation algorithms.	8M
	(b)	Explain Breadth-first searching with necessary sketches.	4M
3.	(a)	Explain Design rules and Symbolic layout for Layout Compaction.	6M
	(b)	Explain 1D and 2D Compaction with neat sketches.	6M
4.	(a)	Discuss Liao-Wong Longest-Path Algorithm with example.	8M
	(b)	Briefly Explain routing problems in IC design.	4M
5.	(a)	Explain in detail about Gate level simulation in VLSI Design.	6M
	(b)	Briefly explain Switch level Simulation in VLSI Design	6M
6.	(a)	Explain ASAP Scheduling Algorithm with an example.	7M
	(b)	What is high level synthesis and explain how it is helpful in IC design	5M
7.	(a)	Explain the Full Design cycle to implement any application on FPGAs.	10M
	(b)	Give any two advantages of FPGA over ASIC	2M
8.	(a)	Describe MCM Technologies.	6M
	(b)	Describe Multiple Stage Routing.	6M

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