AR16 **Set-02**

Code No: 16MTE1002

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT, TEKKALI
(AUTONOMOUS)
I M.Tech I Semester Regular & Supplementary Examinations, February-2018
Advanced Thermodynamics
(Thermal Engineering)

Time: 3 hours **Max Marks: 60**

Answer any FIVE questions
All questions carry equal marks

1. (a) Derive Maxwell's equations [6M]
   (b) Derive the expression for the difference in heat capacities C_p and C_v. [6M]

2. A vessel of volume 0.04 m^3 contains a mixture of saturated water and saturated steam at a temperature of 250^0C. The mass of the liquid present is 9kg. Find the pressure, the mass, the specific volume, the enthalpy, the entropy and the internal energy. [12M]

3. (a) What is the heat of reaction? When is it positive and when negative? [6M]
   (b) Explain combustion reactions and enthalpy formation [6M]

4. Explain reheat cycle. Draw T-S and h-s diagram and derive efficiency. [12M]

5. A steam power station uses the following cycle:
   Steam at boiler outlet 150bar, 550^0C
   Reheat at 40 bar to 550^0C
   Condenser at 0.1 bar.
   Using the Mollier chart and assuming ideal processes find the (a) quality at turbine exhaust (b) cycle efficiency (c) steam rate [12M]

6. What is psychrometric chart? Explain any two psychrometric processes. [12M]

7. (a) What is thermodynamic phenomenon? Explain about thermoelectric circuit. [6M]
   (b) Explain phenomenological laws [6M]

8. Explain with neat diagrams thermodynamic devices and Magneto Hydrodynamic generations [12M]

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AR16 **Set 02**

Code No:16MPE1002

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT, TEKKALI
(AUTONOMOUS)
I M.Tech I Semester Regular & Supplementary Examinations, February-2018
ANALYSIS OF POWER ELECTRONIC CONVERTERS
(Power Electronics and Drives)

Time: 3 hours **Max.Marks:60**

Answer any FIVE questions
All questions carry equal marks

1) (a) Determine the expression for Power factor, R.M.S value of thyristor currents for a 1ph Phase controlled AC Voltage controller supplying R-Load? [6M]

(b) A synchronous connection changer has the primary input voltage of 230v, 50hz.The secondary voltages are V1=120V and V2=88V,If the load resistance is R=5ohms and R.M.S load voltage is 180V, For a delay angle of 90 degrees determine.

i) The rms current thyristors

ii) The input power factor [6M]

2) Explain the operation of 3ph full wave ACVC supplying starconnected R-load for $0^0<\alpha<90^0$ and derive the expression for rms value of output voltage. [12M]

3) Compare the performance of 1ϕ, 230V, 50 Hz supply interms of ripple factor and P.F for $\alpha=30^0$,Consider Load current to be continuous and constant DC. [12M]

4) (a) Support that the P.F of conventional converter can be improved by employing Symmetric Angle control. [6M]
(b) Write short notes about the following concepts in PWM inverter [6M]

(i) Multi level inverter

(ii) Over modulation and under modulation regions

5) (a) Explain the operation of 1ϕ Boost PFC converter [6M]
(b) What does the pulse number in a converter signify and what is the advantage of employing higher pulse number converter? [6M]

6) a.List out the advantages and disadvantages of cascaded multilevel inverter. [3M]
b. For a single phase5level cascaded multilevel inverter. Find the generalized fourier series and THD of the phase voltage. [9M]

7) a) What are the advantages of SVPWM over SPWM? [4M]
b) Derive the equations to eliminate third and fifth harmonics by using harmonic elimination technique for 1phase full bridge inverter operated by Bipolar PWM and develop an algorithm to solve these equations. [8M]

8) (a) Explain three phase fully convertor with R-Load [6M]
(b) Explain about three phase PWM – twelve pulse converter [6M]

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AR16

CODE: 16MVL1002 **SET-2**

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT, TEKKALI
(AUTONOMOUS)
I M.Tech I Semester Regular & Supplementary Examinations, February-2018

DIGITAL DESIGN THROUGH HDL
VLSI System Design

Time: 3 Hours Max Marks:60

Answer any FIVE questions
All questions carry EQUAL marks

1.	(a)	Compare in all aspects about between ASIC Design flow and FPGA Design flow	6
	(b)	Write a short note on the following key words in Strings, Logic Values, Strengths and Data Types.	6
2.	(a)	Explain in brief about the following 1. Parameters 2. Memory 3. Operators 4. System Tasks.	8
	(b)	Write a short note on number system and its representation in Verilog.	4
3.	(a)	What are the different Levels of Design Description in verilog explain with respect to 2X1multiplexer.	6
	(b)	Explain in detail about the Test bench Simulation and Synthesis processes.	6
4.	(a)	Explain the structural representations of Tri-State Gates and its functional operations	6
	(b)	Implement a gate level design for a And –Or - Inverter combinational circuit with its test bench and simulation results	6
5.	(a)	Implement a module for 2 TO 4 decoder using i*f* and i*f*-else constructs.	6
	(b)	What is the significance of the following constructs explain with examples 1. assign- de assign construct 2. repeat construct	6
6.	(a)	Write a short note on for loop and for-ever loop with flow diagrams.	5
	(b)	Explain in detail about the path delay, net delays and gate delays, Propagation delays?	7
7.	(a)	Write a verilog code to master-leave JK Flip-Flop using data flow modelling	6
	(b)	Implement a verilog module to implement a 3 to 8 decoder using structural modelling?	6
8.	(a)	Describe about Package Declaration, Package Body and its significance in verilog?	5
	(b)	Explain about the concurrent signal assignment statements and conditional assignment statements with examples?	7

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AR16

CODE: 16MCS1002 **SET-2**

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT, TEKKALI
(AUTONOMOUS)
I M.Tech I Semester Regular & Supplementary Examinations, February-2018

DATABASE MANAGEMENT SYSTEMS
Computer Science and Engineering

Time: 3 Hours Max Marks:60

Answer any FIVE questions
All questions carry EQUAL marks

1.	(a)	Draw the architecture of a DBMS and explain about the functionality of each component in it.	6M
	(b)	Explain that a database can have more than one external schemas but it must contain only one internal and conceptual schemas	6M
2.	(a)	At a weekend retreat the entity type PERSON has three subtypes CAMPER, BIKER and RUNNER. Draw a separate ER diagram segment for each of the following situations. i. At a given time, a person must be exactly one of these subtypes. ii. A Person may or may not be one of these subtypes. However, a person who is one of these subtypes cannot at the same time be one of the other subtypes. iii. A person may or may not be one of these subtypes. On the other hand, a person may be any two or even three of these subtype at the same time. iv. At a given time a person must be at least one of these subtypes.	4M
	(b)	Discuss the various update operations on relations and the types of integrity constraints that must be checked for each update operation.	8M
3.	(a)	Solve the following queries in SQL. (i) To fetch ALTERNATE records from a table (ii) Find the 3rd MAX salary in the emp table. (iii)How to delete duplicate rows in a table. (iv)Count MGR and their salary in emp table. **?**	6M
	(b)	Write short notes on the following: (i) order by clause and LIKE operator (ii) Set operators	6M
4.	(a)	Differentiate functional dependency and multi valued dependency with example.	6M
	(b)	Explain 4NF and 5NF with an example.	6M
5.	(a)	When is it preferable to use a dense index rather than a sparse index? Justify your answer.	6M
	(b)	Describe the hash file organization. What are the causes of bucket overflow in a hash file organization? What can be done to reduce the occurrence of bucket overflows?	6M
6.	(a)	Differentiate logical and physical data independence.	4M
	(b)	Describe the relationship between Entities, Attributes and Entity Sets.	8M
7.	(a)	What motive is there behind nested queries? Discuss how are operators IN, EXISTS,IS , ANY and ALL used in writing nested queries.	6M
	(b)	Provide a comparative analysis of the concepts FD, MVD and JD's in relational database design.	6M
8.	(a)	Describe the transaction states with a neat diagram.	6M
	(b)	What is relation? Differentiate between relation schema and relation instance. Define the terms unity and degree of relation. What are domain constraints?	6M

AR16

CODE: 16MSE1002 **SET-2**

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT, TEKKALI
(AUTONOMOUS)
I M.Tech I Semester Regular & Supplementary Examinations, February-2018

THEORY OF ELASTICITY AND PLASTICITY
(Structural Engineering)

Time: 3 Hours Max Marks:60

Answer any FIVE questions
All questions carry EQUAL marks

1.		The state of stress at a point is given by the stress tensor $\begin{bmatrix} 200 & 200 & 100 \\ 200 & -150 & -300 \\ 100 & -300 & -100 \end{bmatrix}$ MPa. Determine the normal and shear stresses acting on the octahedral plane	12 M
2.	(a)	Write about stress function.	6 M
	(b)	Write about stress ellipsoid	6 M
3.		Derive compatibility equation in terms of stress components for a two dimensional problem.	12 M
4.		Derive expression for finding principal stresses and write stress invariants	12 M
5.		Explain effect of circular hole on stress distribution in a plate and obtain expressions for stress components	12 M
6.		Find stresses due to torsion in an elliptical cross section	12 M
7.		Derive expressions to find maximum shear stresses and their planes.	12 M
8.		Write a short note on yield criterion in theory of plasticity.	12 M

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AR13 SET-02

Code No: 13MVL1002

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT, TEKKALI
(AUTONOMOUS)
I M.Tech I Semester Supplementary Examinations, February-2018
VLSI TECHNOLOGY AND DESIGN
(Common to VLSI System Design and Digital Electronics & Communication Systems)

Time: 3 hours **Max Marks: 60**

Answer any FIVE questions
All questions carry equal marks
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1. a) Explain BiCMOS inverter with neat diagram
   b) Discuss the alternate forms of PULL-UP with diagrams and show its characteristics

2. a) Analyze power consumption of Inverter circuit by considering both the pull up and pull down phases of operation
   b) Define power delay product?

3. a) How glitching and logic factorization influences on low power designs explain
   b) Explain gate testing with the help of simple logic network

4. a) What is the difference between signal skew and clock skew?
   b) Explain the Dynamic latch circuit and draw the stick diagram

5. a) Explain floor planning tips?
   b) Discuss problems associated in power distribution?

6. a) What is logic synthesis
   b) Explain Technology – Independent Logic Optimization
   c) Write notes on switch level simulation

7. a) Explain Hardware / Software co-design
   b) Explain the method architecture-driven voltage scaling for reducing power consumption in the architecture

8. a) Explain Latch-Up in CMOS circuts
   b) Write and explain Alternative gate Circuits with suitable diagrams

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AR13 **Set 02**

Code No:13MPE1002

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT, TEKKALI
(AUTONOMOUS)
I M.Tech I Semester Supplementary Examinations, February-2018
ANALYSIS OF POWER ELECTRONIC CONVERTERS
(Power Electronics and Electric Drives)

Time: 3 hours **Max.Marks:60**

Answer any FIVE questions
All questions carry equal marks

1) (a) Determine the expression for Power factor, R.M.S value of thyristor currents for a 1ph Phase controlled AC Voltage controller supplying R-Load? [6M]

(b) A synchronous connection changer has the primary input voltage of 230v, 50hz.The secondary voltages are V1=120V and V2=88V,If the load resistance is R=5ohms and R.M.S load voltage is 180V, For a delay angle of 90 degrees determine.

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