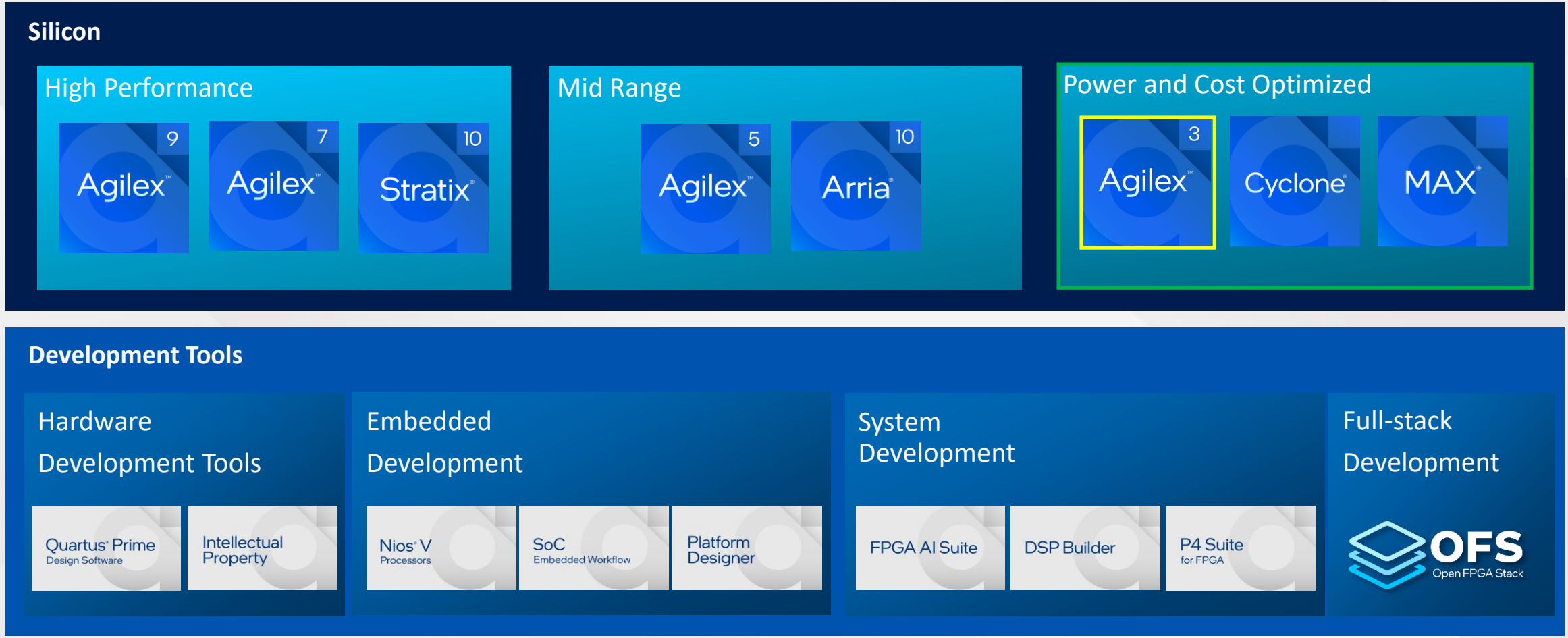
Agilex™ 3 FPGAs

The portfolio that enables ALL

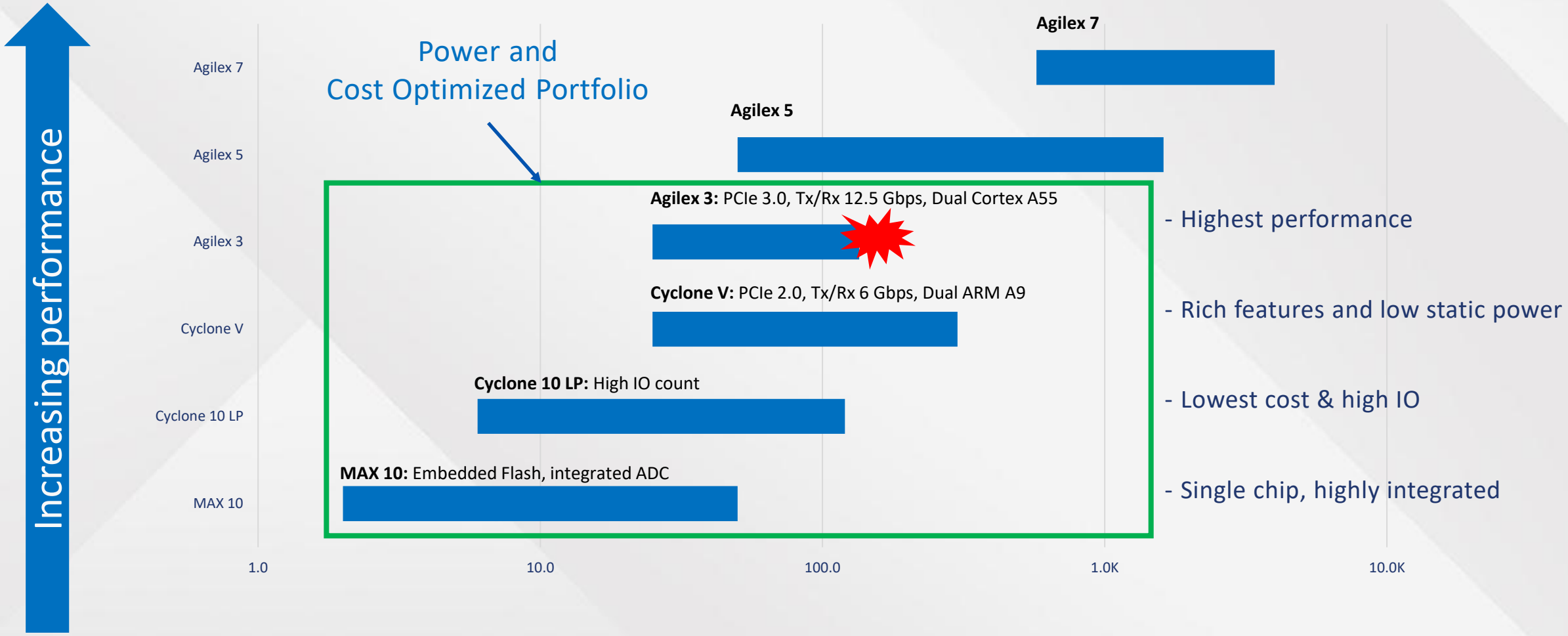
Speed, breadth, simplicity



Driving transformation with a full-stack portfolio

Altera Product Families

A broad set of complementary power and cost-optimized families to meet diverse customer needs



Agilex™ 3 Family
Designed for Wide Range of Applications

- Product family with multiple logic densities from 25K – 135K logic elements
- Variable Pitch BGA (VPBGA) enables high IO density packages w/ 0.8mm design rules
- Flexible IO with high voltage and high speed (MIPI, 1.25G LVDS) support
- 12.5 Gbps Transceiver with PCIe 3.0 and 10G Ethernet Hard IP blocks
- Cost-effective memory standard support with LPDDR4
- Hard processor system support with Dual ARM Cortex A55 cores
- Enhanced device security including PQC Secure boot
- Ease of use and support in Quartus® Prime Pro Edition Software
- Supply Resiliency with Intel Supply Chain

Key Applications and Use-Cases

Industrial

- Sensors / Motors / Connectivity, Functional Safety and Security
- I/O Modules and IoT Devices
- Tiny PLC and Edge AI

Surveillance, Retail, Consumer

- Smart City/Retail
- Trucks, bus systems, trains and railways
- EV Charging
- Vision Processing

Video, Medical

- Video Connectivity
- Video Processing
- Video over IP
- Consumer Electronics
- Diagnostic Imaging & Video
- Patient monitoring

Test & Measurement

- Relay and board management in Automated Test Equipment (ATE)
- Legacy IO interfacing in RF instrument

Military

- Host mgmt. port
- Avionics (control, monitoring, and management for actuators, displays)
- Sensors

Data Center

- Platform Root of Trust
- Board Management Control

Enabling the Edge with FPGAs Designed for Low Power and Cost-Sensitive Applications

Agilex 3 Family Table

Product Line		A3C 025[3]	A3C 050	A3C 065	A3C 100	A3C 135
Specification Options		Y, Z	Y, Z	Y, Z	U, V, W, Y, Z	U, V, W, Y, Z
Logic	Logic elements (LEs)	25K	47K	65K	100K	135K
	ALM	8,500	16,000	22,000	34,000	45,800
Embedded RAM	M20K	65	123	169	262	353
	M20K(Mb)	1.27	2.40	3.30	5.12	6.89
DSP	Variable precision DSP blocks	34	65	88	138	184
	18 x 19 multipliers	64	130	176	276	368
XCVR	@ 12.5 Gbps	0	0	0	4	4
Hard IP	PCIe	0	0	0	3.0 x4	3.0 x4
	10GbE Hard IP	0	0	0	1	1
	MIPI D-PHY @ 2.5Gbps	3	7	7	14	14
GPIO	HVIO (1.8V- 3.3V)	160	160	160	200	200
	HSIO (1.0V -1.3V)	96	96	96	192	192
EMIF	External Memory Interface	-	LPDDR4	LPDDR4	LPDDR4	LPDDR4
PLL	IO and Fabric feeding / System[4]	7 / 0	7 / 0	7 / 0	11 / 1	11 / 1
HPS	Hard Processor	N/A	N/A	N/A	2x A55 up to 800 MHz	
Security	PQC Secure Boot	-	-	-	Yes	Yes
	SDM Secure Device Manager	PQC data path support, SHA-384, ECDSA 256/384 bitstream authentication, AES-256, side-channel attack resistance, cryptographic services, PUF, SPDM attestation, physical anti-tamper support				

Package Code (Package size, ball pitch, array pattern)	HVIO/HSIO/HPSIO/XCVR				
M12A (12x12mm, 0.5 mm, Standard BGA)	160/96/0/0	160/96/0/0	160/96/0/0		
M16A (16x16mm, 0.5 mm, Standard BGA)				40/192/48/4	40/192/48/4
B18A[2] (18x18mm, Variable, VPBGA[1])	160/48/0/0	160/48/0/0	160/48/0/0	160/48/0/0[2]	160/48/0/0[2]
B18B (18x18mm, Variable, VPBGA[1])	160/96/0/0	160/96/0/0	160/96/0/0		
B23C (23x23mm, Varaiable, VPBGA[1])				200/144/48/4	200/144/48/4

Specification

Code	HPS	PQC Boot	Crypto Services	EMIF, MIPI, PUF, SPDM attestation
U	Yes	Yes*	Yes	Yes
V	No	Yes*	No	Yes
W	Yes	No	Yes	Yes
Y	No	No	No	Yes
Z	No	No	No	No

*Note: Post Quantum Cryptography Secure boot is supported on 100k/135k logic density devices

- Full migration
- Conditional Migration
  - A3C 025 does not support EMIF
  - B18A package: A3C 025, A3C 050, and A3C 065 have on package decoupling, A3C 100 and A3C 135 do not.

Definitions:

- HSIO: High-speed IO
- HVIO: High-voltage IO
- HPSIO: HPS IO available with HPS
- VPBGA: Variable Pitch Ball Grid Array
- XCVR: transceiver

Notes:

1) Package ball pitch is variable, please contact to your sales representative for more information.
2) B18A does not support specifications U and W (no HPS enabled devices)
3) A3C025 does not support EMIF
4) The system PLL can be repurposed for core fabric usage if not used for the transceiver

Power and Performance

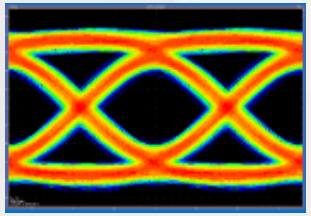
Agilex™ 3 FPGAs Technology Enablers for Power-Efficient Performance

Intel 7

- Intel leadership Technology
  - Intel 7 process technology with interconnect innovations
  - Intel VPBGA packaging technology increases IO density

Hyperflex® FPGA Architecture

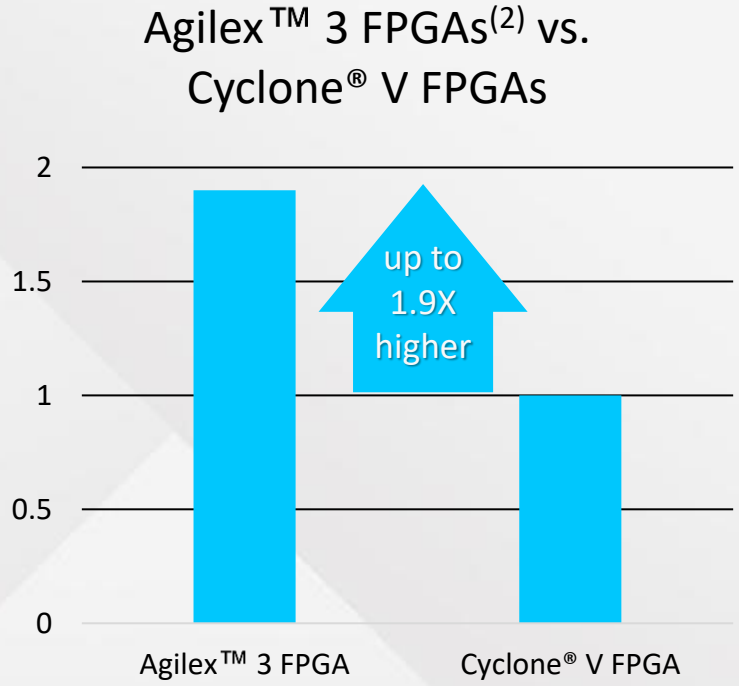
- 2nd Generation Hyperflex™ FPGA Architecture
  - Delivers higher performance/watt than Cyclone® V FPGAs

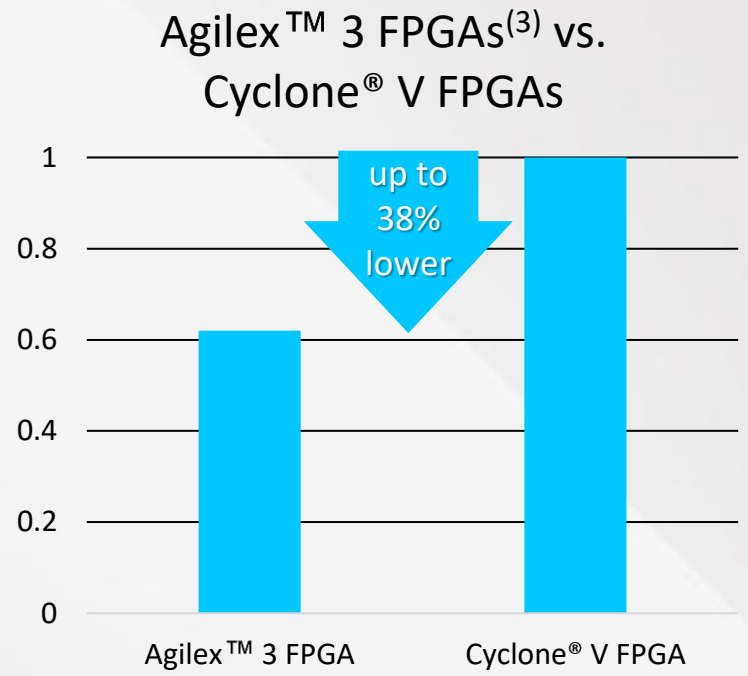


- High level of system integration
  - High-speed transceiver I/O, Ethernet hard IP, DDR controller hard IP , and optional Hard Processor System (HPS)

Agilex™ 3 FPGAs Offer Higher Performance and Lower Power

- Up to 1.9X higher fabric performance or up to 38% lower total power compared to Cyclone® V FPGA(1)





Notes:

(1) Fabric performance comparison is done between Cyclone® V FPGA and Agilex™ 3 FPGA

(2) The performance QoR (Quality of Results) Fmax (maximum frequency) represents the geomean derived from Altera's QoR design suite of 45 separate designs.

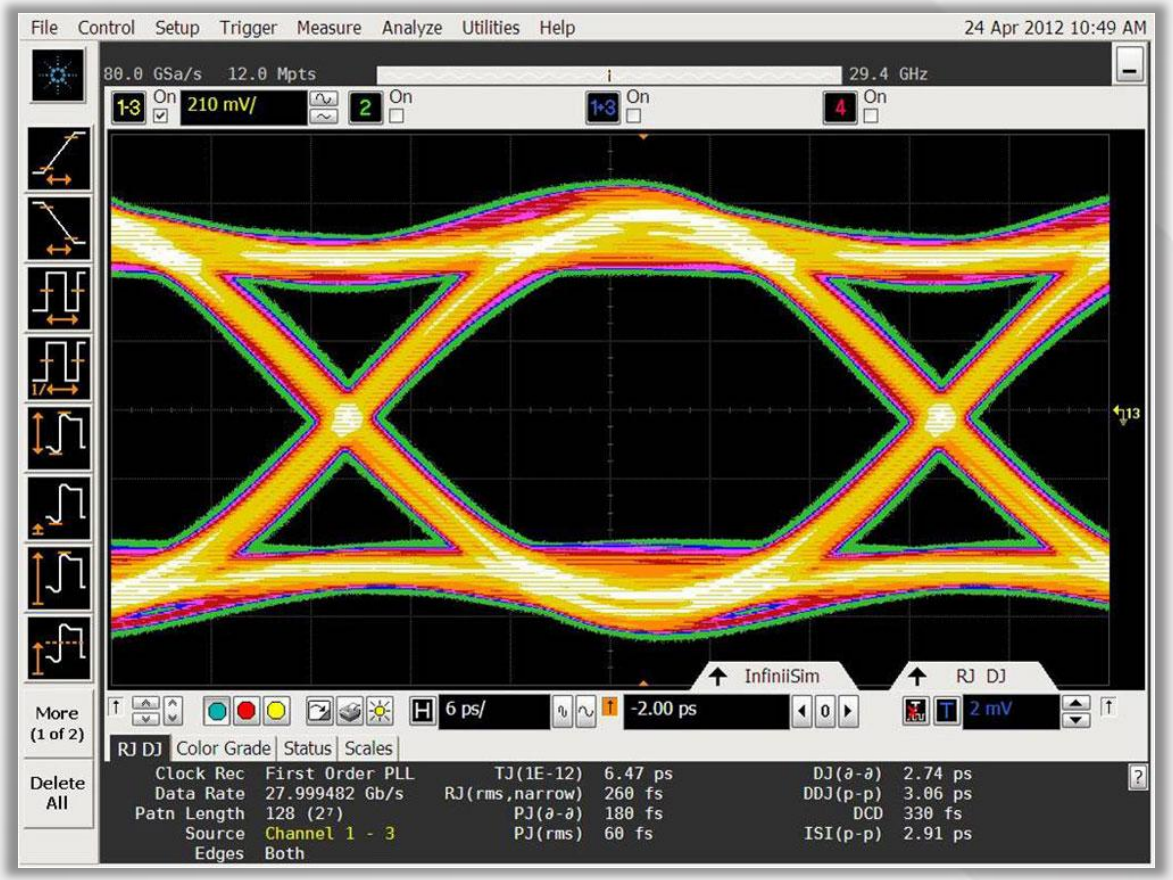
(3) The total power comparison is done with Agilex™ 3 core power at 0.75V and Cyclone V® core power at 1.1V and both devices at 100% utilization running at 150 MHz.

(4) Performance varies by use, configuration and other factors. Learn more at www.intel.com/PerformanceIndex. Performance results are based on testing as of dates shown in configurations and may not reflect all publicly available updates. See backup for configuration details. No product or component can be absolutely secure.

Agilex™ 3 FPGAs Transceivers

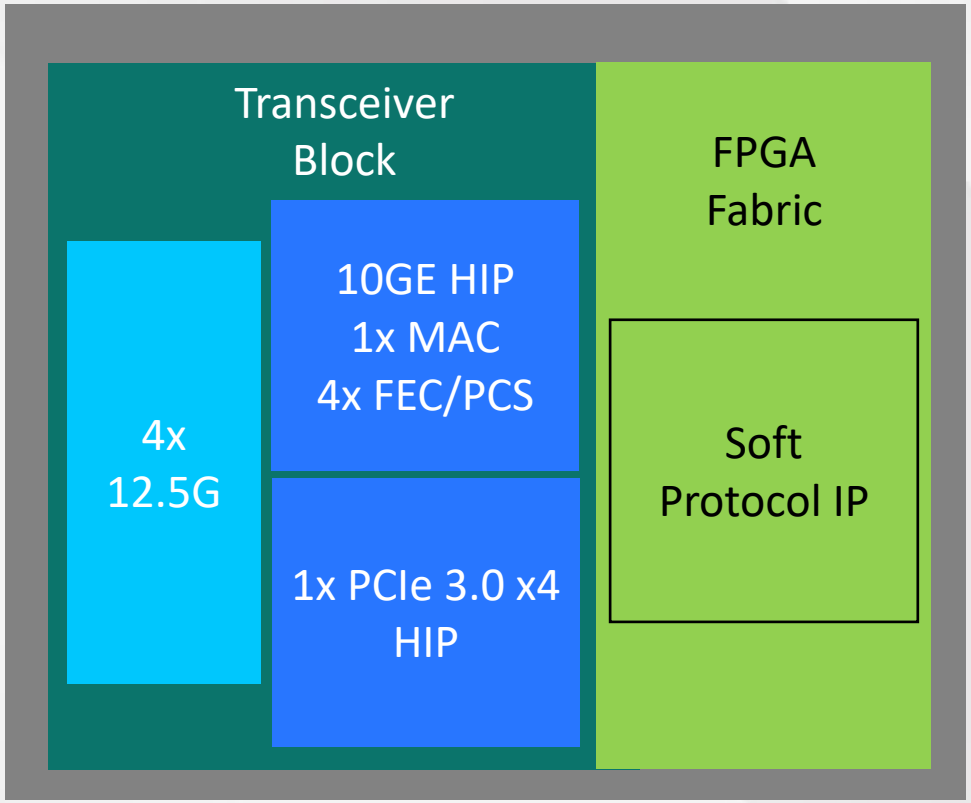
- Monolithic transceiver implementation → low latency for edge applications
- Up to 4 channels
- Transceiver block contains 4 channels
  - 2 reference clock inputs per quad: a local clock and a global clock
  - Each channel can select from its local clock or any global clock on the same side of the FPGA
  - Transmitter is independent of the receiver

Integrated 12.5 Gbps transceivers



Agilex™3 FPGAs Transceivers Features

Key Features
4x 12.5 NRZ (Continuous 1- 12.5 Gbps)
1x 10G Ethernet with optional FEC (IEEE 802.3 Clause 74 Firecode FEC HIP)
4x 10G FEC Direct (IEEE802.3 Clause 74, Clause108 and ETC RS(528,514)FEC)
4x 10G PCS Direct (64b/66b) (IEEE 802.3-compliant Clause 49 PCS)
PCIe 3.0 x4 Controller HIP
Independent TX and RX to support combining simplex protocols
4x PMA Direct (bypass Ethernet and PCIe HIP)



Agilex™ 3 offers a wide variety of IO: Increased performance and cost reduction

- High Speed IO (HSIO):

High-speed I/O (HSIO) (96/bank)	Specification	Comments
Low Voltage CMOS (LVCMOS) 1.05 V and 1.2 V single-ended	717 MHz	-
1.3 V LVDS	1.25 Gbps	Vicm: 0.5 to 1.375 V Vocm: 0.9 to 1.1 V
MIPI D-PHY 2.1	2.5 Gbps (HS/LP)	No external components required
SGMII (LVDS)	1.25 Gbps	Add AC coupling if required

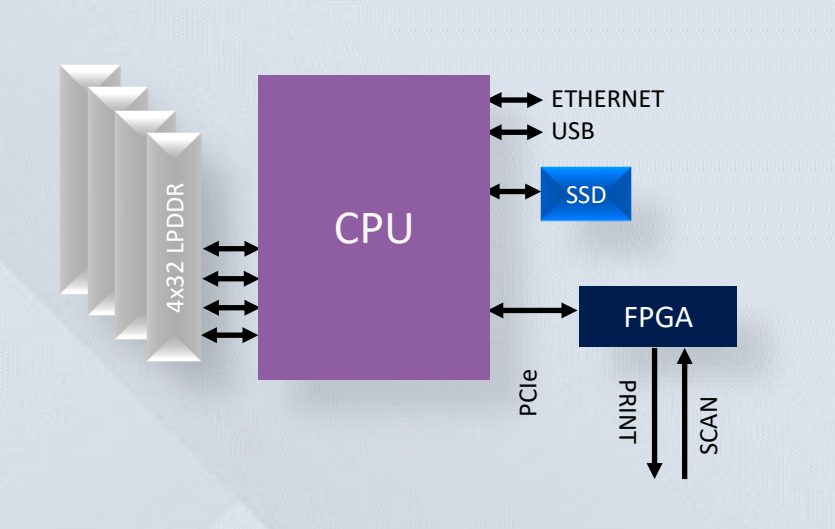
- High Voltage IO (HVIO):

High Voltage I/O (HVIO) (20/bank)	Specification	Comments
1.8 V single-ended LVCMOS	250 MHz (125 MHz DDR)	RGMII supported at 1.8 V
2.5 V / 3.3 V single-ended LVCMOS	200 MHz (100 MHz DDR)	

HPS Integration Streamlines Your Product Development

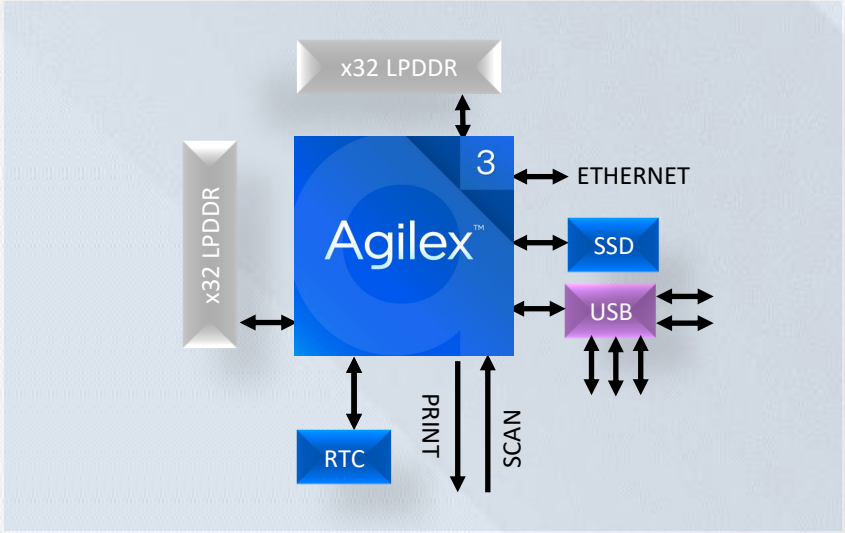
SoC FPGA: Benefits of Integration

Disaggregated Software and Hardware



- CPU lifecycles are short
- Harder to integrate
- Harder to co-optimize

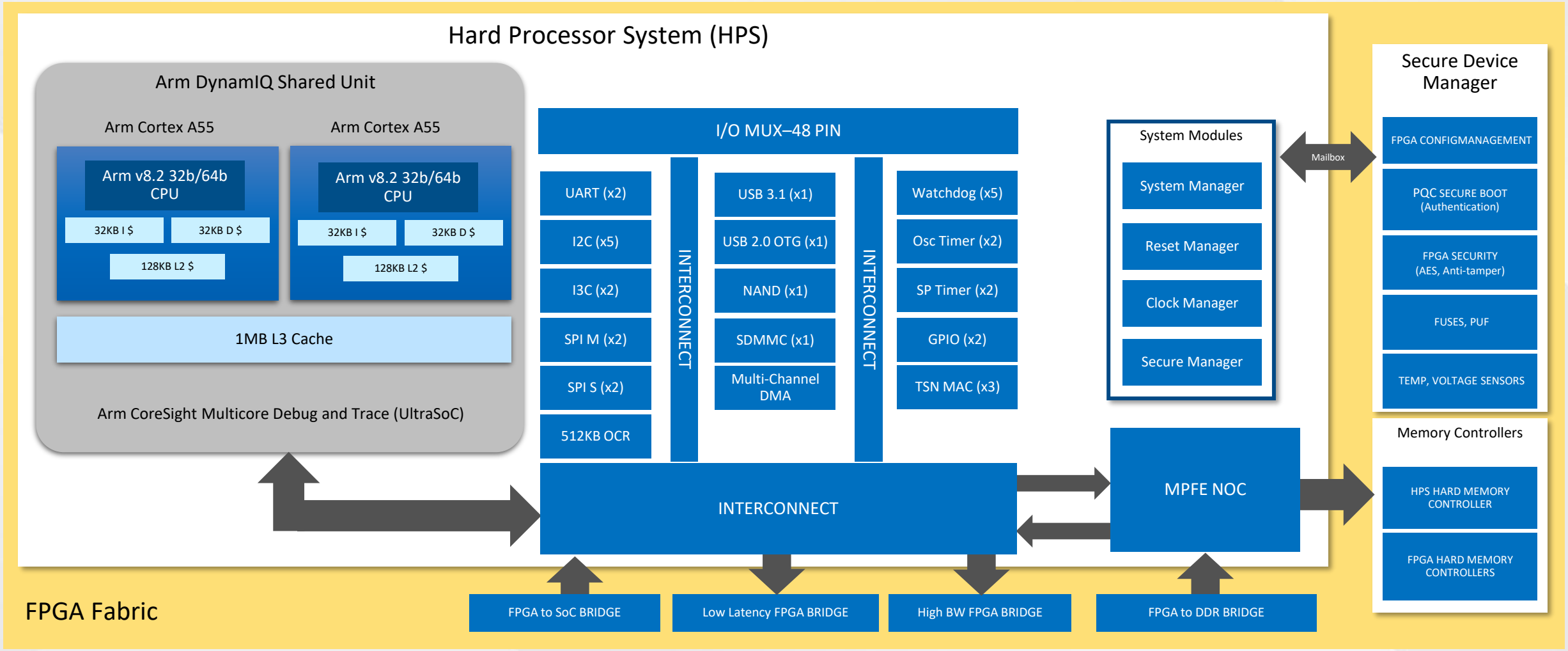
Co-optimization of Software and Hardware



Portability

- Increased system performance
- Reduced power consumption
- Reduced board size
- Reduced system cost

Agilex™ 3 Hard Processor System with Quad Arm Cores



High-Speed Transceivers PHY, PCS, Device I/O, Hard PCIe 3.0

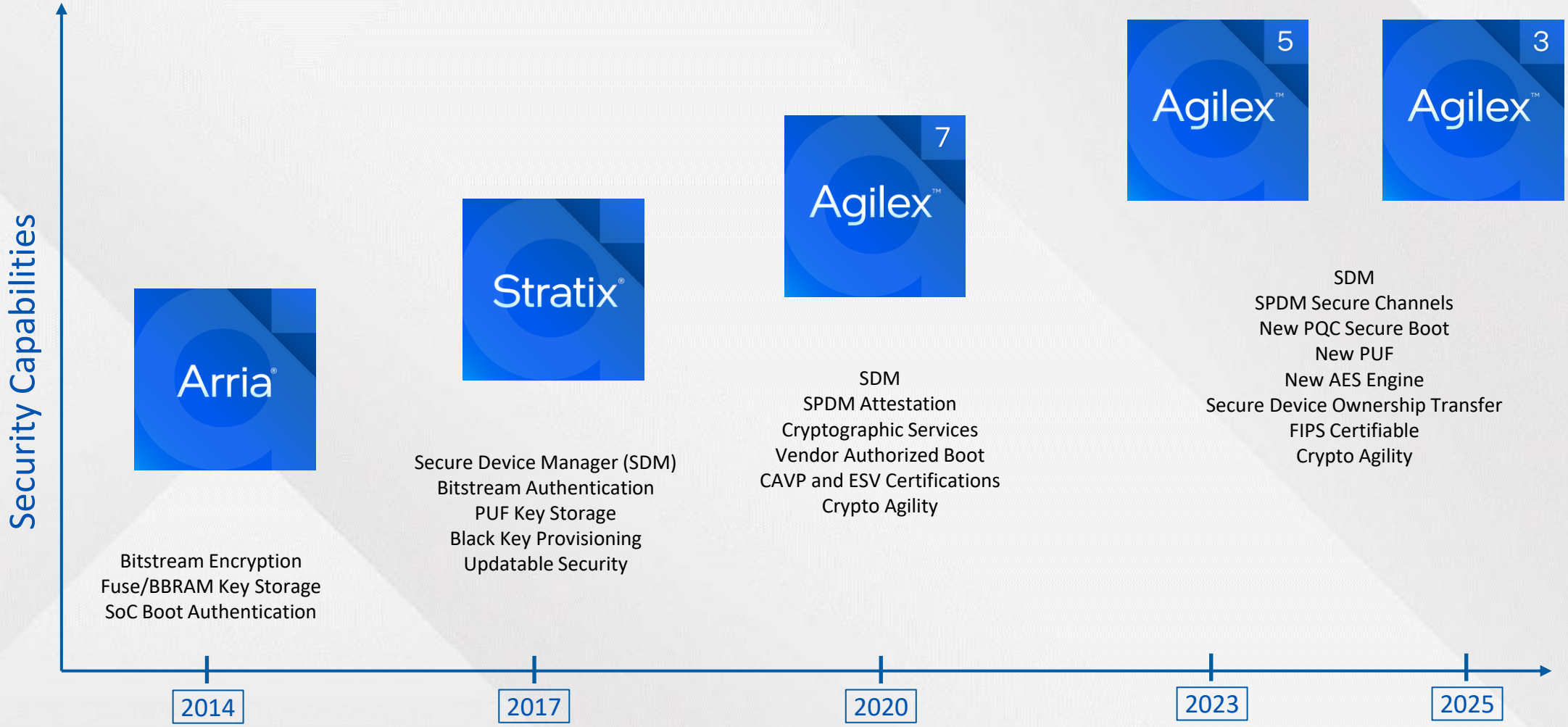
Embedded Arm Software and Tools

Altera® SoC FPGA Support

- New Altera software developers site on GitHub
  - More frequent releases with latest features and bug fixes
  - Single location for software developers: drivers, examples, etc.
- Choice of Linux kernels
  - Latest stable, long-term support
- Choice of bootloaders
  - U-Boot and Arm trusted firmware (ATF)
- Choice of Yocto Project based Linux* distributions
  - Smooth transition to commercial Linux vendors
- Bootstrap your project with maintained reference designs
  - PCIe rootport 3.0 reference design
  - QSPI boot, RSU reference designs
- Standard software development:
  - Arm* Development Studio for Altera SoC FPGA
  - Ashling RiscFree* IDE for Altera® FPGAs
- Comprehensive ecosystem
- Early software development with SoC Simics simulator

Advanced Security Features

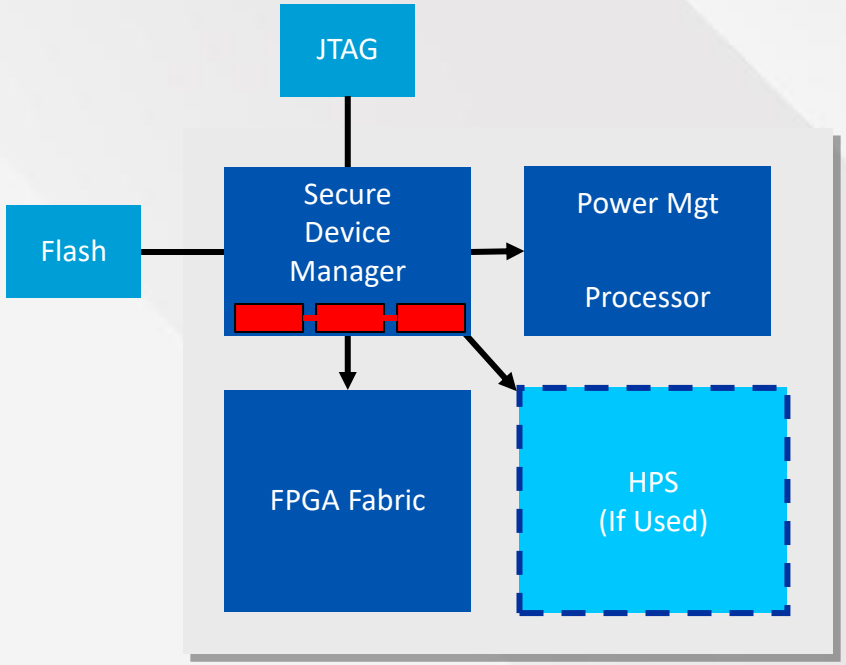
Agilex™ 3 FPGA Leverages our advanced Security roadmap



MAX® devices include 128 bit encryption
Cyclone® devices include 256 bit encryption and erasable keys

Secure Device Manager (SDM) Highlights

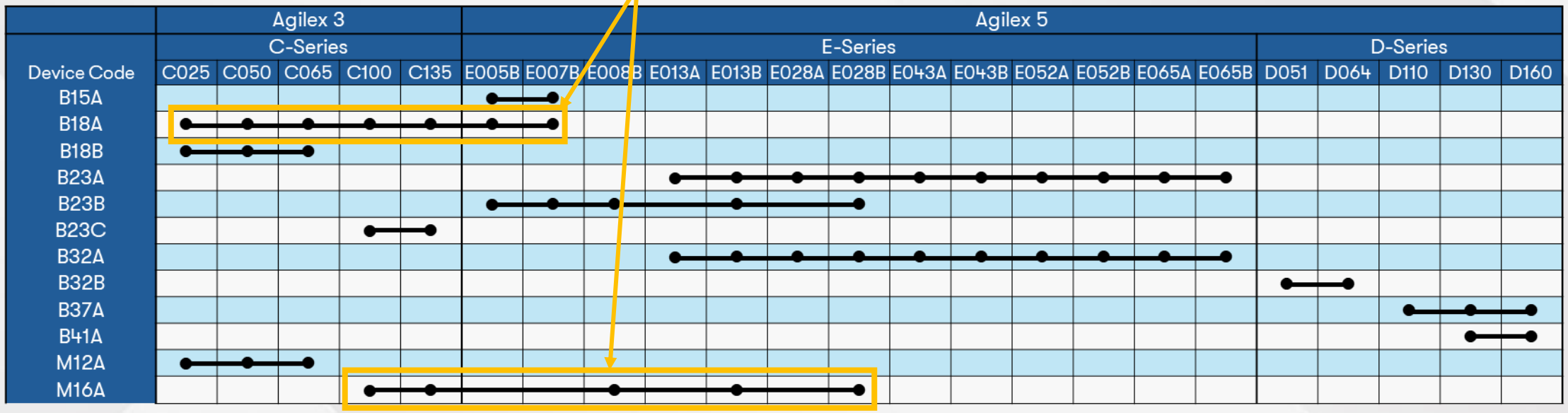
- Secure boot support:
  - PQC Secure boot
  - Private Key Root of Trust on FPGA
  - Public Key only on FPGA (external Root of Trust)
- Built-in error correction code (ECC) memory
- Operations priority over fabric and other µPs
- Manages tamper sensors, and scripted device erasure
- Manages boot process, encryption, authentication, and all keys



Dedicated Secure Device Manager and Firmware

Agilex™ 3 ↔ Agilex™ 5 package footprint compatibility

2 footprint compatible packages between the families



- Conditional migration between Agilex 3 and Agilex 5 on B18A and M16A packages
- Only footprint compatibility support
- No cross family migration support in Quartus
- Please take note the device resources, performance and specifications may vary between devices
- Please refer to appropriate product table, device overview and datasheet for details

Delivering a Resilient Supply Chain with Longevity

Strengthening our Supply Chain

Focused Investment

Increased capacity, redundancy, and inventory

Resilient Portfolio

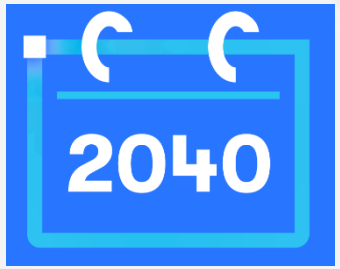
Considers product performance, features, and supply chain

Predictable Lead-time Guidance

16 weeks or better

Agile Prototyping

Over 80 devices ship in a few weeks for prototype quantities



Supply Longevity

Expected lifecycle

Diverse & Resilient Manufacturing

Strong partnerships with wafer, substrate, and assembly and test partners

altera™

For more information on Agilex 3

Thank You