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REGULAR PAPER

Memristor Based Full Adder Circuit for Better Performance

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Abstract
In this paper, we have designed memristor based AND, OR, and exclusive-OR (XOR) gates. With the help of these gates, memristor based full adder circuit has proposed. Simulation results of the proposed circuit including all above gates have been reported. Prominent improvement of the proposed circuit has been represented in power consumption 54.74%, delay 14.84%, and lesser transistor count with respect to conventional circuit.

Keywords Memristor · Full adder · Logic gates · Power consumption · Delay · Transistor count

1 Introduction

In 1971, Prof. Leon Chua presents the logical and scientific concept for the actuality of novel two-terminal circuit element called the memristor (memory resistor) [1]. In 2008, HP Labs realized practical memristor that consists of titanium dioxide (TiO_2) thin film sandwiched between two metallic (Pt) electrodes on both sides [2]. As we know that, it is too difficult to overcome various physical limitations of the traditional CMOS technology. Further, it is to improve in speed, power dissipation, and size. This improvement is also so difficult. Hence, the researchers' attention attracted these points. However, researchers found that alternate device are preferred for higher performance as Memristor (Resistor with Memory). The logic bits are stored as resistance states in memristors, so it can be used for memory implementation [3]. Numerous applications have been proposed by researchers recently that comprises neuromorphic applications as synapse and use in analog circuits and digital domain (the logic computation) [4–6]. One of the potential applications of memristor is the logic computation. Researchers have been proposed different approaches of logic computation [7]. One of the approaches of logic computation is the material implication using memristor. Moreover, other approaches have been proposed integration with CMOS logic to compute various logical operations. Material implication logic appearances promising outcomes but it need more computational steps in performing logic [8]. In this methodology, AND and OR logic can be implemented using the memristors only. For better performance of these gates, Memristor Ratioed Logic (MRL) should be integrated with CMOS inverter circuit [9]. MRL approach is used in our proposed circuit and this proposed circuit included integrated CMOS technology.

The rest of the paper is structured as follow: Section 2 illustrates memristor modeling. Section3 introduces the memristor based AND and OR logic computation. Section 4 reported proposed memristor based XOR gate. Section 5 discussed proposed memristor based adder circuits which include the half adder and full adder circuit. Section 6 summarizes simulation Results and Discussion. Finally, Sect. 7 concludes this paper.

2 Memristor Modeling

Chua and Kang introduced physical memristive devices in (e.g., ionic systems and discharge tubes), the topic of memristors and memristive devices have not attracted

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much attention for more than 35 years. After long time, in 2008, Hewlett Packard linked memristive devices's theory and this theory has been implimented to TiO_2 resistive switches. Hewlett Packard has been proposed a device and stated that this device is similar to ideal memristor. Initially, Hewlett Packard claimed that their device is similar to ideal memristors, the proposed model for the structure and behavior of their device. The proposed structure is shown in Fig. 1 and its equivalent electrical circuit of memristor (Fig. 2). Voltage and current with time relationship are represented [10]:

$$v(t) = R(t) \cdot i(t) \tag{1}$$

$$R(t) = \frac{R_{on} w(t)}{D} + R_{off}\left(1 - \frac{w(t)}{D}\right) \tag{2}$$

$$\frac{dw(t)}{dt} = \frac{\mu v R_{on}}{D} i(t) \tag{3}$$

where R_{on} represents the resistance when $x(t)$ is equal to D, and R_{off} indicates the resistance when $x(t)$ is equal to 0. $x(t)$ is the state variable and its interval [0, D].

All of the different devices that can be considered as memristive devices share several characteristics: they are fabricated as oxides sandwiched between two metals (metal–insulator–metal structure, also named MIM), and their size is relatively small. Additionally, as described by the definition of memristive devices, these devices have varying resistance and are non-volatile (i.e., no voltage is applied to retain the resistance). Due to these characteristics and their relatively low switching time, high endurance, and low switching energy (typically 0.1–1 PJ), memristive technologies are primarily investigated as memory applications [11–14].

The symbol of the memristor has been shown in Fig. 3. When current flows into black strip (black strip in the Fig. 3) the memristance decreases. When current flows out of the black strip the memristance increases [15]. However, if we plot a graph of the current flowing in the memristor with respect to the voltage across it, we will obtain a pinched hysteresis loop, as shown in Fig. 4. The loop will always be pinched at the origin.

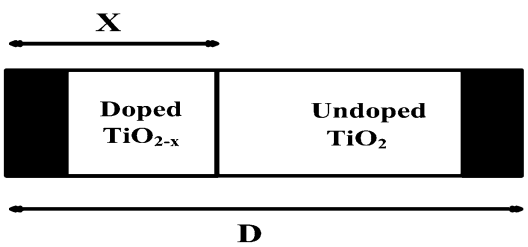

Fig. 1 Hewlett Packward original device model

Fig. 2 Equivalent circuit of memristor [28]

Physics Behind the Hysteresis Loop The hysteresis occurs due to the sinusoidal current $i(t)$ has maxima and minima value and it does not happen at same time as the corresponding memristor voltage $v(t)$. The pinching occurs because both $i(t)$ and $v(t)$ become zero at the same time. It must also be noted that the loop shrinks and tends to a straight line (similar to resistance) as the frequency increases. When the memristor starts from origin and voltage increases, the conductivity rises. It reaches to the normalized maximum value of the voltage. Then the voltage starts decreasing and the conductivity continues to increase, passing from the origin to the minimum value of resistance. And then the voltage decreases to decrease the conductivity. The memristor can reach a maximum value of R_{off} and minimum value to R_{on}. The amplitude of input parameters defines the maximum resistances.

Several mathematical models of memristor have been proposed by scientists [16–20] but a nonlinear dopant drift memristor model is used for simulation of proposed circuits [10].

3 Memristor Based AND and OR Logic Circuits

By using memristors, we can analyze the basic Boolean logic operations such as AND and OR logic gates. While, many researchers have stated the material implication logic using memristor but that is not compatible with present generation CMOS method. Material implication works on the state variable, the inputs and outputs are the states of memristors instead of the voltages that are required for signal propagation in CMOS process. Hence, memristor added with CMOS technology.

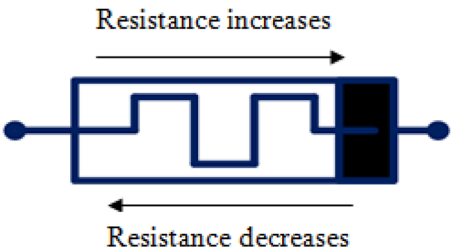

Fig. 3 Symbol of memristor

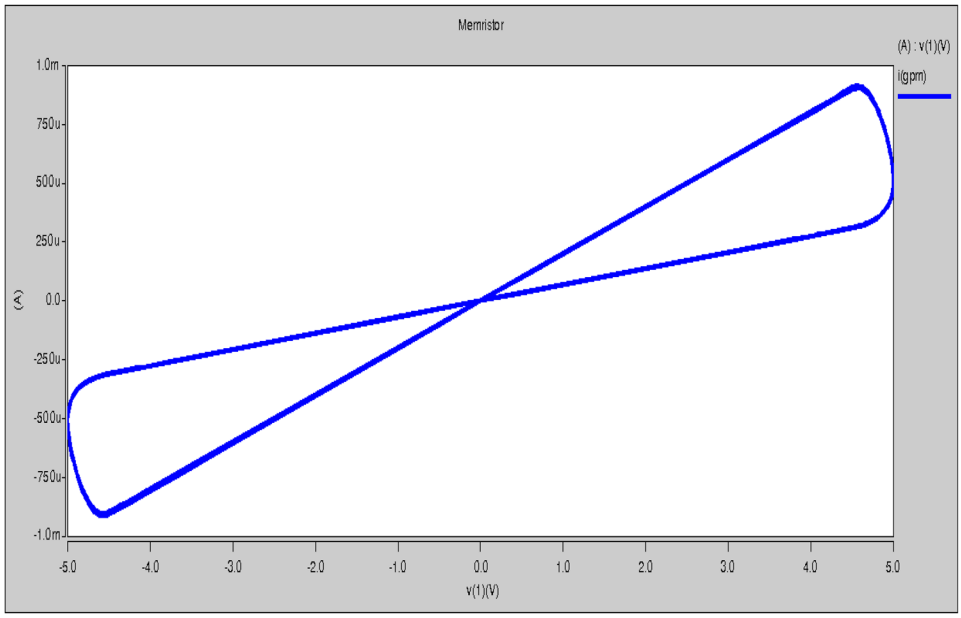

Fig. 4 Hysteresis curve of memristor model (current–voltage pinched hysteresis loop)

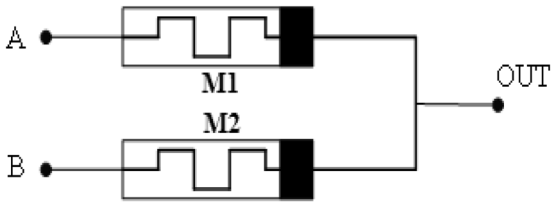

Fig. 5 Logical AND operation using memristor

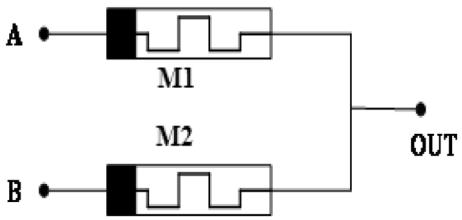

Fig. 6 Logical OR operation using memristor

The idea behind of using memristors for logic computation is its property, which is varying resistance with respect to the direction of current flow through this device. The resistance of memristor depends on the direction of current flow through the device. By using these phenomena, we can generate a voltage divider circuit. Figure 5 shows the schematic of memristor based two input AND gate circuit.

When the polarity of the memristors M1 and M2 is reversed, the circuit behaves as OR gate. Figure 6 shows the memristor based two input OR gate circuit.

Table 1 Truth table of AND Gate and OR gate

A	B	OUT_{AND}	Memresistance (AND)	OUT_{OR}	Memresistance (OR)
0	0	0	R_{off} (100 kΩ)	0	R_{off} (1 kΩ)
0	1	0	R_{off} (100 kΩ)	1	R_{on} (1 kΩ)
1	0	0	R_{off} (100 kΩ)	1	R_{on}(1 kΩ)
1	1	1	R_{on} (1 kΩ)	1	R_{on} (100 kΩ)

Table 1 indicates truth table of AND, OR gate and their values resistances.

For AND gate, when any input is logic 1 and other is logic 0 that means A = 1 and B = 0, A = 0 and B = 1. For this type case, A = 1 and B = 0, the current flows through higher potential to lower potential i.e. V_{dd} to G_{nd}. When current passes from memristor (M1), the resistance of that memristor (M1) increases to R_{OFF}, the resistance of memristor (M2) decreases to R_{ON} and current leave through GND node. Resistance of memristors M1 and M2 are R_{OFF} and R_{ON}, respectively. In this way, we develop two resistors R_{OFF} and R_{ON}, whose values is different. Therefore, by using the voltage divider rule, we get output OUT = 0.

Similarly, input A = 0 and B = 1 are applied on this circuit, output comes out zero.

$$\mathrm{OUT} = \frac{R_{on}}{R_{on} + R_{off}} \times V_{dd} \ll V_{dd} \approx G_{nd} \tag{4}$$

Both inputs are same (A = 0, B = 0 or A = 1, B = 1), its output of the circuit becomes applied as inputs. Calculate by this deveining concept can be defined as:

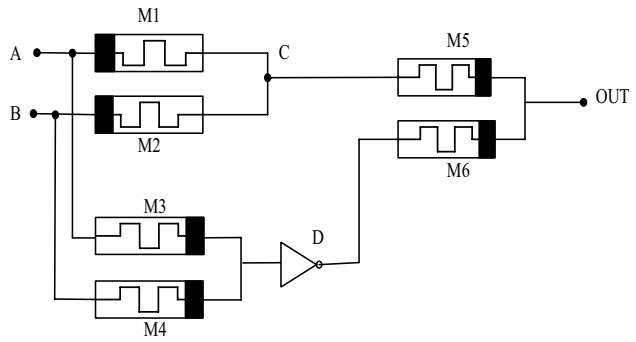

Fig. 7 Proposed memristor based XOR logic gate

Table 2 Truth table of XOR gate

A	B	OUT	Memresistance
0	0	0	R_{off} (100 kΩ)
0	1	1	R_{on} (1 kΩ)
1	0	1	R_{on} (1 kΩ)
1	1	0	R_{off} (100 kΩ)

$$OUT = \frac{R_{on}}{R_{off} + R_{off}} \times V_{dd} \tag{5}$$

Similar, operation of OR gate can be understood operation of AND gate [21].

4 Proposed Memristor Based XOR Gate

To get the complete logic family, we should add CMOS inverter at the output of OR gate to get NOR operation and similarly at the output of AND gate to get NAND operation. The operating voltage is kept at same level of 1.8 V for all the designed gates. By using the NAND gate XOR gate can be designed using these approaches as shown in Fig. 7.

Table 2 indicates truth table of XOR gate [22–24] and Thiers memristance values. When, both the inputs (A = 1 and B = 1) are at V_{dd} (logic 1), which is applied on the proposed XOR circuit as shown in Fig. 7. No current flow through the OR gate which consist memristor M1 and M2 and the output of at node C is V_{dd} (logic 1). Memristor M3 and M4 and inverter formed the memristor based NAND gate, the output at node D is nearly ground (logic 0). Memristor M5 and M6 forms the AND gate, so the output of XOR gate is nearly ground (logic 0). Similarly, when both the inputs (A = 0 and B = 0) are at logic 0, there is no current flow through the circuit. The output at node C is nearly ground, the output at node D is V_{dd} so, the output of XOR gate is nearly ground. When any of inputs is at logic 1 and other at logic 0, the output at node C and node D is V_{dd}. The output of XOR gate is V_{dd}. When current passes from memristor M5, the resistance of that memristor increases to R_{OFF}, the resistance of memristor M6 decreases to R_{ON} and current leave through nearly ground node. Resistances of memristors are R_{OFF} and R_{ON}. In this way, we develop two resistors R_{OFF} and R_{ON} whose values are different. Therefore, by using the voltage divider rule, we get output OUT = 1 that completes the logic for XOR gate. This working operation is verified and its memresistance values of memristors have been indicating in Table 2.

5 Proposed Memristor Based Adder Circuit

Conventional adder circuits are classified into two parts first is known as half adder circuit and other as full adder circuit. Conventional adder circuit is built by CMOS technology. However, market demands less power, less delay (fast speed) and lesser transistor count. Therefore, we proposed memristor based half and full adder circuit.

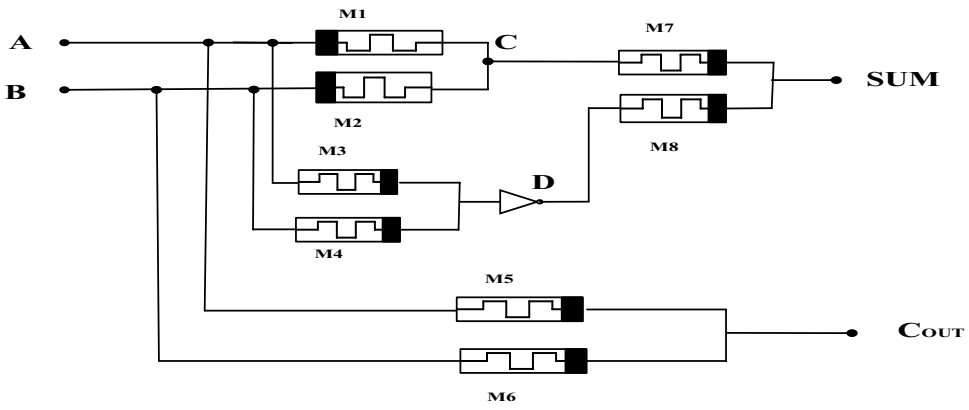

Fig. 8 Proposed memristor based half adder circuit

Table 3 Truth table of half adder

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

5.1 Proposed Memristor Based Half Adder Circuit

Figure 8 has shown half adder circuit that includes one memristor based AND gate and XOR gate. Working operation is similar as working operation of conventional half adder circuit. All inputs, Sum, and carry are shown in Table 3. Implementation of sum is XOR circuit, which has already been discussed in above section. Implementation of carry is AND circuits, which is also discussed. These inputs are applied on this circuit and outputs of this circuit have formed in sum and carry, successfully. Simulation results have shown in results and discussion part.

5.2 Proposed Memristor Based Full Adder Circuit

Full adder circuit using memristor has shown in Fig. 9. This full adder circuit have two XOR, two AND, and one OR gates. Working operation of this proposed circuit depends on assembled all components such as XOR, AND and OR logic circuit. Working operation of these all components has already been discussed. Working operation of this proposed circuit indicated in tabular form in Table 4.

Table 4 Truth table of full adder

A	B	C	Sum	Carry
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1
0	0	1	1	0
0	1	0	1	0

6 Simulation Results and Discussion

6.1 AND Gate, OR Gates, XOR Gates, Half, and Full Adder Circuit

In this section, SPICE simulator has been used to simulate the proposed XOR circuit and full adder circuit. The basic memristor model [10, 25–28] is employed in this simulation. The parameters for simulation of proposed circuit are set as $R_{on} = 1\ k\Omega$, $R_{off} = 100\ k\Omega$, $V_t = 2\ V$ and $V_{dd} = 1.8\ V$.

The simulation result of the AND and OR gate is shown in Figs. 10 and 11, respectively. Both inputs v(1) and v(2) are applied on AND and OR gates and its output is V (3).

Figure 12 shows simulation result of the XOR circuit for four possible input combinations. Both inputs v(1) and v(2) are applied on XOR gates and its output is v(9). The simulation result of half adder shown in Fig. 13. In the simulation result, node v(1) and v(2) represent the input wave A and B. Node v(10) shown the sum of half adder circuit, whereas node v(8) has shown the output carry of the half adder.

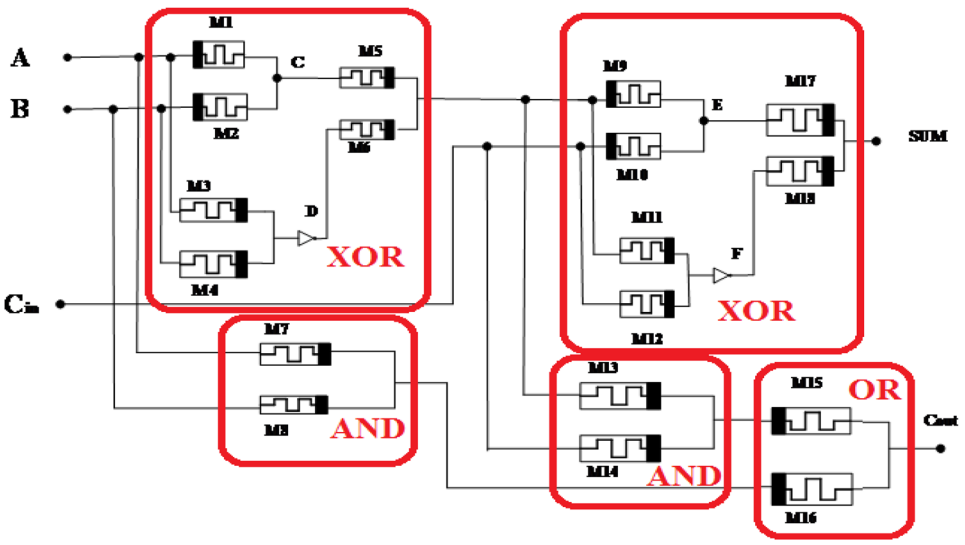

Fig. 9 Proposed memristor based full-adder circuit

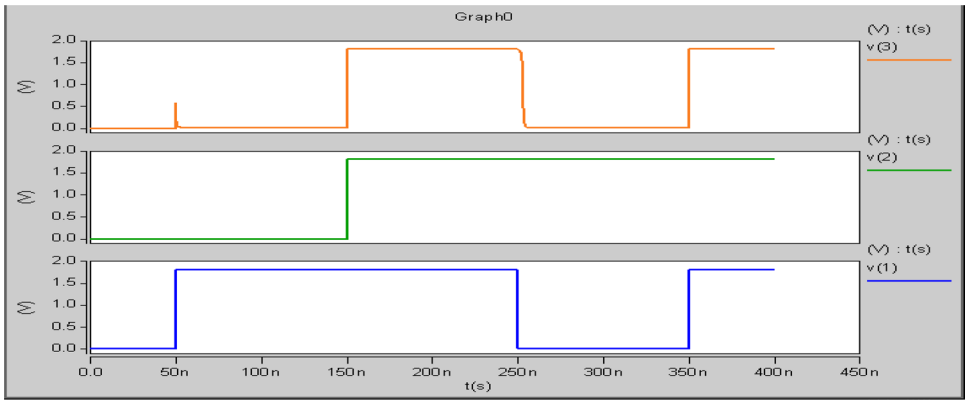

Fig. 10 Simulation result of AND logic gate

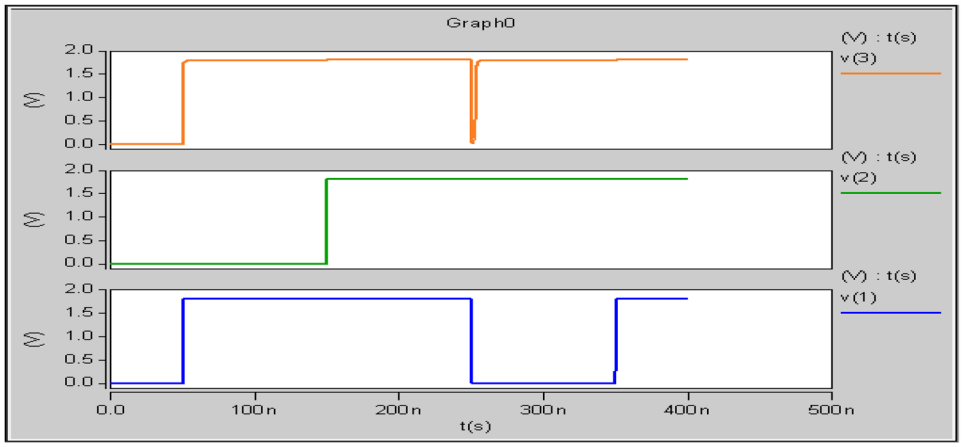

Fig. 11 Simulation result of OR logic gate

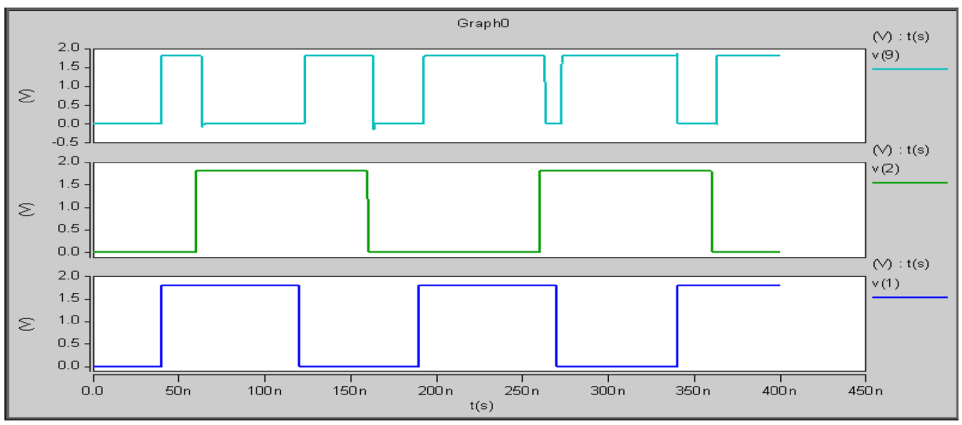

Fig. 12 Simulation result of XOR logic gate

The simulation result of the full adder circuit is shown in Fig. 14. In the simulation result, node v(1) and node v(2) shown the inputs A and B, whereas node (3) represents the input carry. Node v(22) shown the sum of the full adder circuit and node v(20) shown the output carry of the full adder circuit.

6.2 Comparison Between CMOS and Memristor Based Full Adder Circuit

1. *Speed* In general, the total calculation time for any logic computation of Memristor based logic is less than CMOS logic. From the considerations like rise time, fall time, Memristor logic looks conspicuous than CMOS logic. From Table 5, we can see delay of memristor based full adder circuit has improved ~ 15% as compared to conventional CMOS circuit.

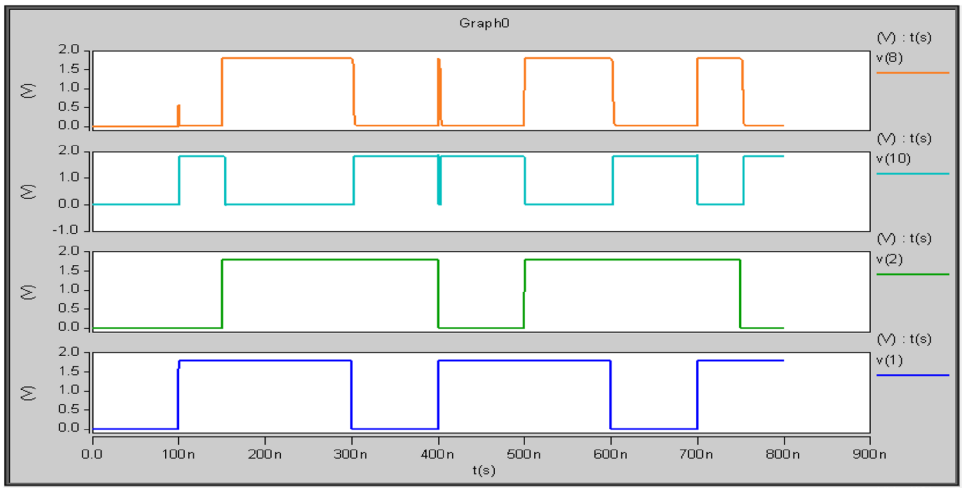

Fig. 13 Simulation result of half adder circuit

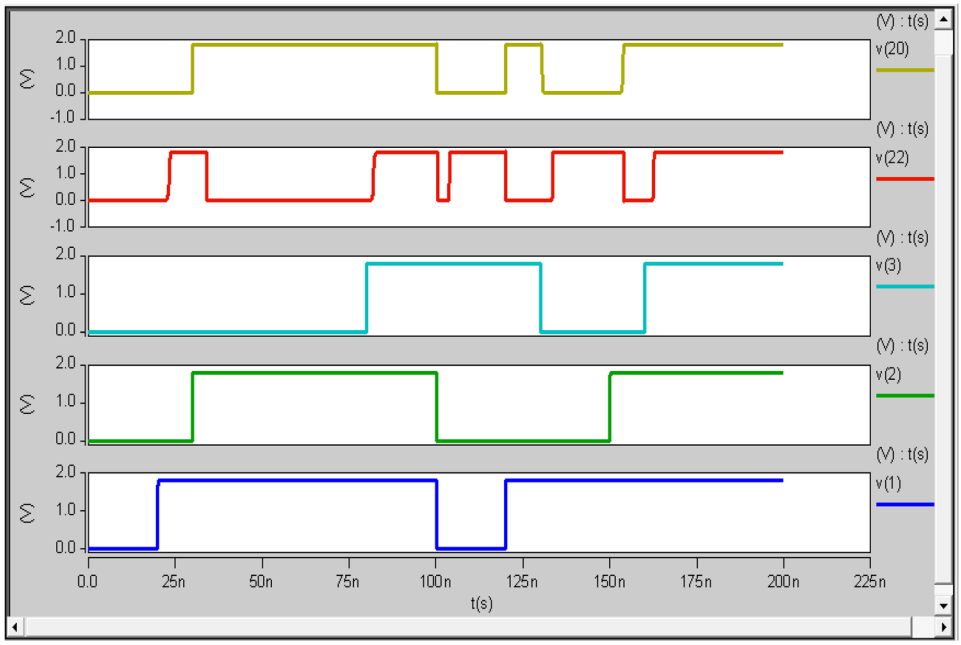

Fig. 14 Simulation result of full adder circuit

Table 5 Comparison of CMOS and memristor based full adder circuit

Parameters	CMOS based full adder	Memristor based full adder
No. of transistor	34	24
Rise time delay	96.4 ps	73.5 ps
fall time delay	54.2 ps	51.3 ps
Total delay	75.3 ps	62.4 ps
Power consumption	117.3 µW	53.08 µW

2. *Area utilization* For the theory that memristors are smaller than MOSFETs, so the area utilization memristor logic is less than the CMOS logic. These new logic consumers in the area saving because the width of memristors considered 3 nm which is smaller than width of a MOSFET which is considered 180 nm. Memristors can possibly be implemented on the polysilicon layer of a MOSFET, thus a single MOSFET can be a stock for many memristors. From the Table 5, we can say that the Memristor technology used only 24 transistors while CMOS technology used 34 transistors.
3. *Power dissipation* Commonly, current generation CMOS process chomps more power due to the constant connection of supply voltage produce static leakage. From the analysis of power consumption memristor consumes less power than CMOS logic. Static power dissipation can be further reduced by well known methods like clock gating or multi threshold CMOS. Static power dissipation is

not a main unease for the average power; the maximum power dissipation is the dynamic power that is due to the transitions. Power is figured out for signal that has thoroughgoing transitions. From Table 5, power dissipation of memristor based full adder circuit has reduces power ~ 55% as compared to conventional CMOS based full adder circuit.

7 Conclusion

In this paper, Logic gates are designed with CMOS 180 nm technology. A memristor based XOR gate with six memristors, which can execute XOR operation. Furthermore, the proposed full adder circuit is compared to other basic logic gate and basic full adder, the proposed circuits advantages simpler architecture, higher speed (~ 15% reduce delay), lower power consumption (~ 55% reduces), and lesser transistor count (in proposed circuit 24 transistor as compare to 34 transistor in conventional CMOS based circuit). This paper opens the possibility of newly developed memristor for logic circuits.

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