Digital Design

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Chapter 1, 2 and half of 3

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Week 8

Recap of topics

and discussion on issues

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Parity – Error Detection

Don't Care

Universal Gates

Confusion (F and F')

K-Maps

Boolean Algebra

Etc.

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Universal gates

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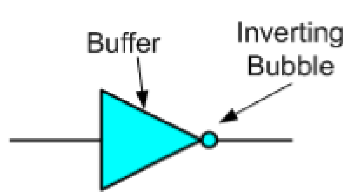
Universal Gates

- NAND and NOR are universal gates.
- Universal gate because they can be used to implement any logic gate

- The small circle (bubble) at the output of the graphic symbol of a NOT gate is formally called a negation indicator and designates the logical complement.



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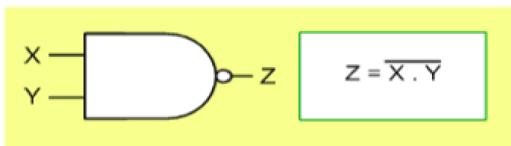
NAND Gate

- Complement of AND

X	Y	NAND
0	0	1
0	1	1
1	0	1
1	1	0



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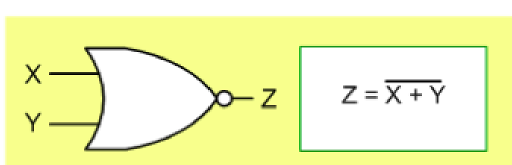
NOR Gate

- Complement of OR

X	Y	NOR
0	0	1
0	1	0
1	0	0
1	1	0



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Universal Gates

- NAND and NOR gates are economical, easy to fabricate and used as the basic gates used in all IC digital logic families.
- AND is implemented as an NAND gate followed by inverter (Not the other way Round)
- OR is implemented as a NOR gate followed by inverter (Not the other way Round)

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Universal Gates

- To prove that any Boolean function can be implemented using only NAND gates, it can be shown that the AND, OR, and NOT operations can be performed using only these gates.

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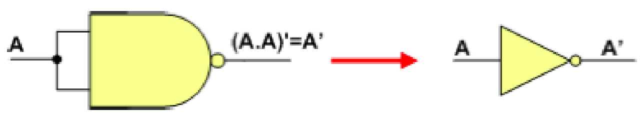
Inverter using only NAND Gate

- First Method



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Inverter Using only NAND Gate

- Second method

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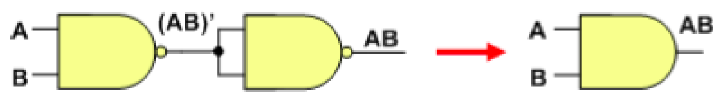
AND Using only NAND Gates

- Using NAND as AND



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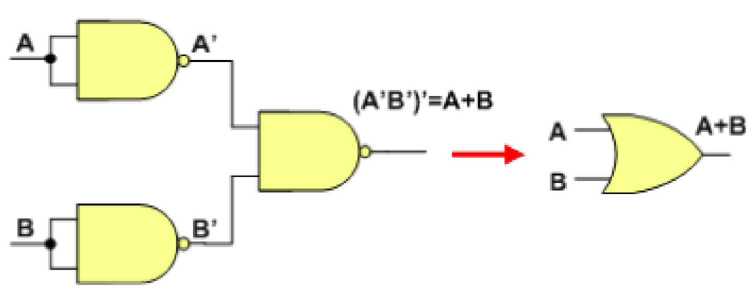
OR Using only NAND Gates

- Using NAND implementing equivalent OR



- Thus, the NAND gate is a universal gate since it can implement the AND, OR and NOT functions.

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NOT, AND, OR Using NOR

- To prove that any Boolean function can be implemented using only NOR gates, it can be shown that the AND, OR, and NOT operations can be performed using only these gates.

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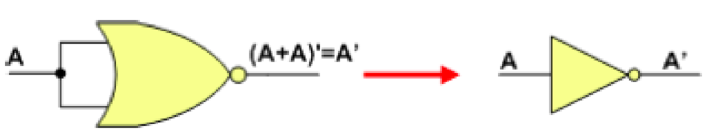
Inverter Using only NOR Gate

- First Method:



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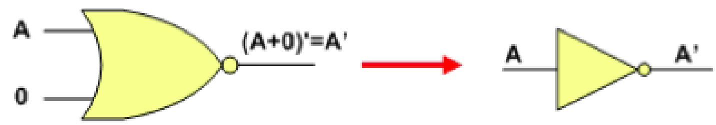
Inverter Using only NOR Gate

- Second Method



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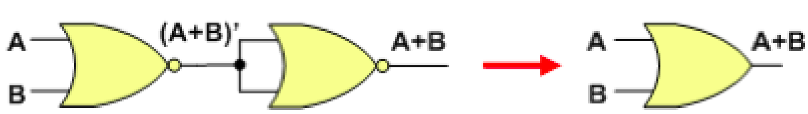
OR Using only NOR Gates



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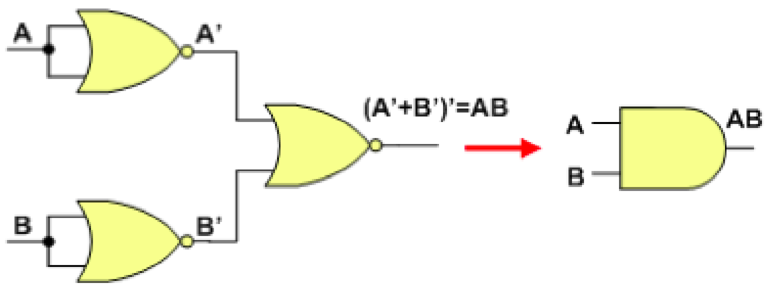
AND Using only NOR Gates



- Thus, the NOR gate is a universal gate since it can implement the AND, OR and NOT functions.

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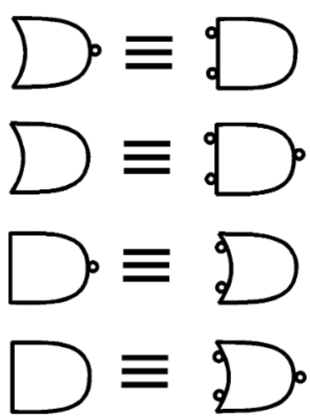
Equivalent Gates - Summary



AND Gate and OR Gate Equivalents

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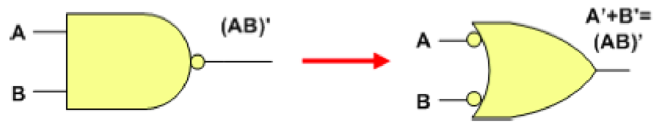
Equivalent Gates (1)

- Some important cases of gate equivalence
- A NAND gate is equivalent to an inverted-input OR gate.



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NAND Gate

AND-Invert

Invert-OR

F = (xyz)'

F = x'+y'+z'

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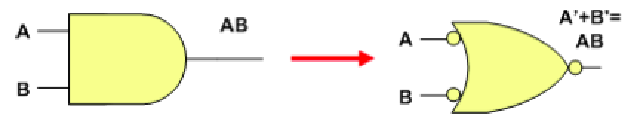
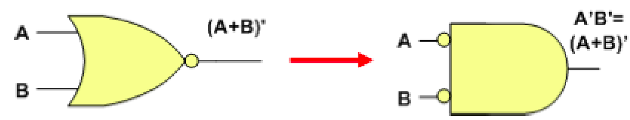
Equivalent Gates (2)

An AND gate is equivalent to an inverted-input NOR gate.



A NOR gate is equivalent to an inverted-input AND gate.



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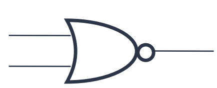
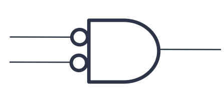
NOR Gate



OR-Invert

$F = (x+y+z)'$



Invert-AND

$F = x'y'z'$

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Equivalent Gates (3)

An OR gate is equivalent to an inverted-input NAND gate.

Two NOT gates in series are same as a buffer because they cancel each other as A'' = A.

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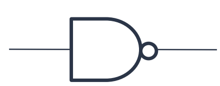
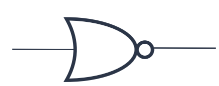
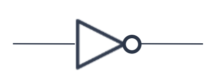
NOT Gate



AND-Invert



OR-Invert



Buffer-Invert

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Two-Level Implementations - Recall

- Boolean functions in either SOP or POS forms can be implemented using 2-Level implementations.
- For SOP forms AND gates will be in the first level and a single OR gate will be in the second level.
- For POS forms OR gates will be in the first level and a single AND gate will be in the second level.
- **Note that using inverters to complement input variables is not counted as a level.**

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Two-Level Implementations

- SOP forms can be implemented using only NAND gates, while POS forms can be implemented using only NOR gates.

Example 1: Implement the following SOP function using only universal gates.

$$F = XZ + Y'Z + X'YZ$$

  - Being an SOP expression, it is implemented in 2-levels as shown in the figure.

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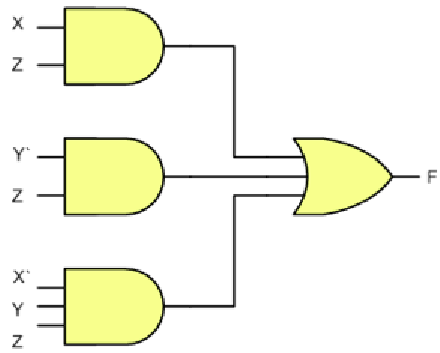
Example 1

- SOP → NAND
- F = XZ + Y'Z + X'YZ
- First implement with AND/OR
- should have only two-levels.



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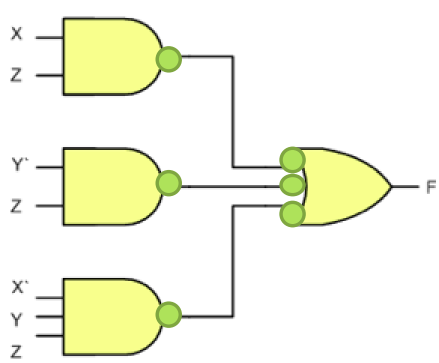
Example 1

- For NAND:
- Put bubbles at input of OR and output of AND



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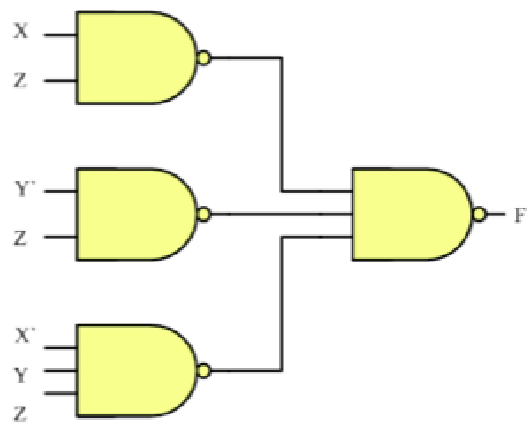
Example 1



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Example 2

- Implement the following POS function

$$F = (X+Z)\,(Y'+Z)\,(X'+Y+Z)$$

- It should be implemented in 2-levels
- POS → NOR

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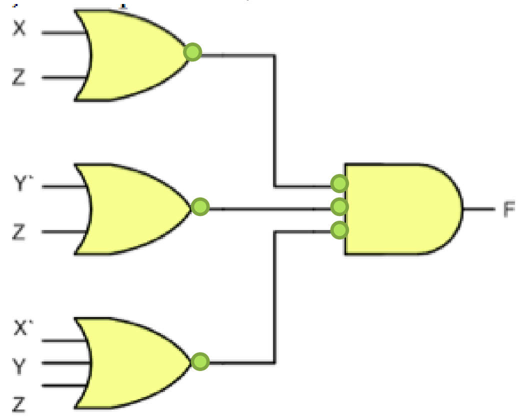
Example 2

- Do it your self !
- For NOR: Output of OR and input of AND



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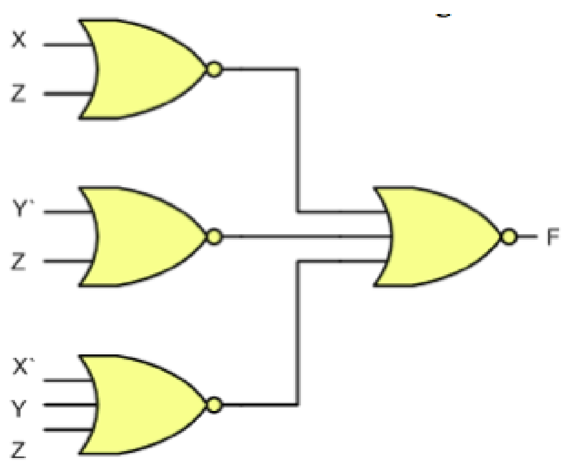
Answer!!!



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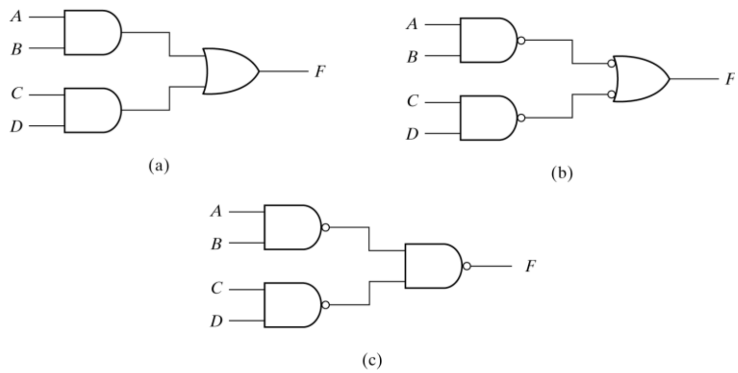
Two-Level NAND Implementation - Example

- $F = AB+CD$



Three ways to implement F=AB+CD

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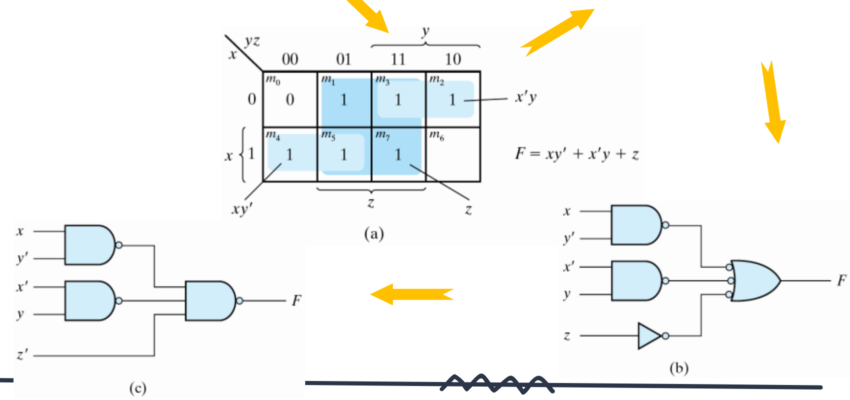
Two-Level NAND Implementation - Example

$$F(x,y,z)=\sum(1,2,3,4,5,7)$$

$$F(x,y,z)=xy'+x'y+z$$



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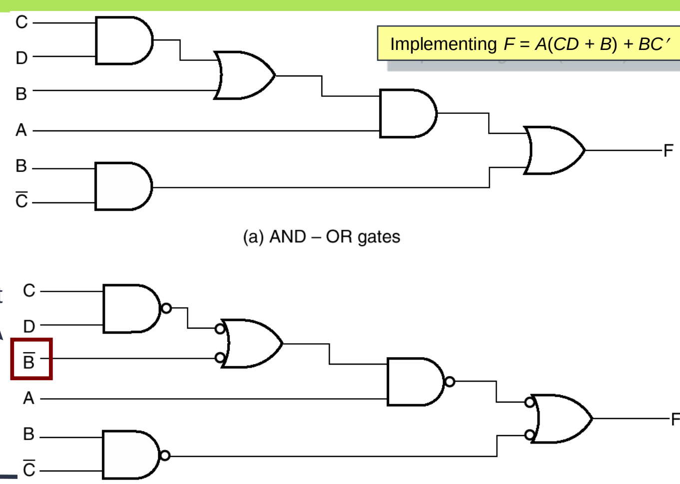
Multilevel Circuits – Convert to NAND

Implementing $F = A(CD + B) + BC'$

Bubbles cancel each other

Note this complement



(a) AND – OR gates

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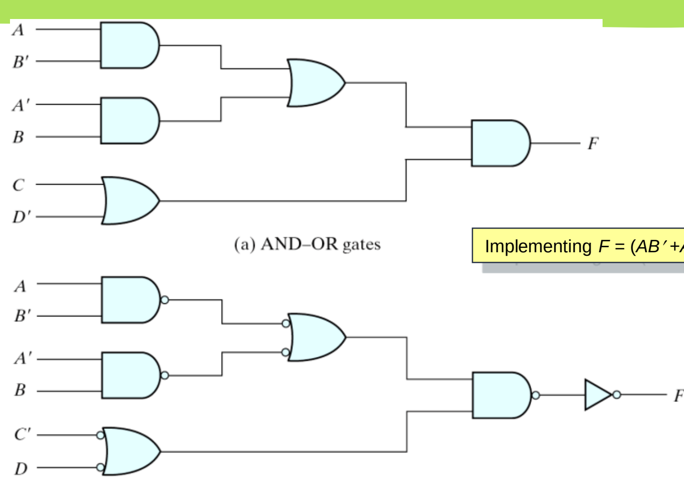
Multilevel Circuits – Convert to NAND

Implementing $F = (AB' + A'B)(C + D')$



(a) AND–OR gates

(b) NAND gates

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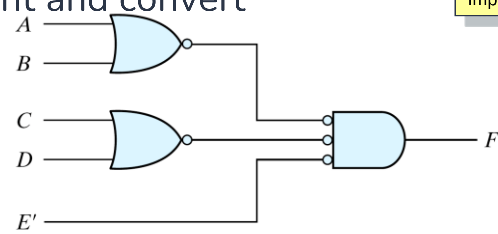
Two-Level NOR Implementation - Convert

- Implement and convert

Implementing $F = (A + B)(C + D)E$



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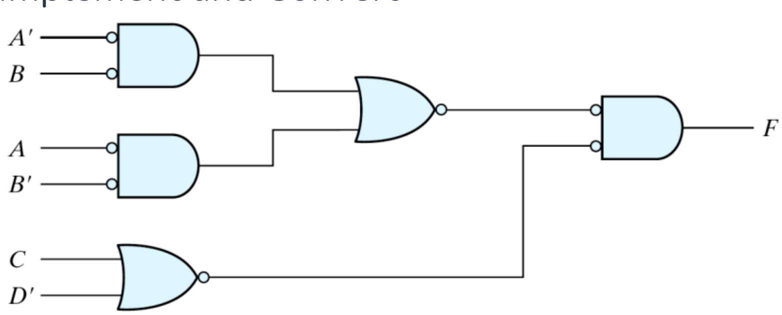
Multilevel NOR Circuit

Implementing $F = (AB' + A'B)(C + D')$

- Implement and Convert



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