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Assignment-2

Ques1) Location of memory block in cache = block % number of cache blocks.

Since, it is a direct mapped cache no replacement policy is required. As, we can see in the table, 8 is further replaced by 82 in the 2nd cache block whereas 3, 20 and 30 are all present in the cache till the end. Therefore, Answer is B.

Memory block	Blocks
0	8, 0, 16, 24
1	9, 17, 25, 63, 17
2	2, 18, 2, 82
3	3
4	20
5	55
6	30
7	63, 63

∴ memory block 18 is not in cache while 3, 20 and 80 are in cache.

Ques2) 4 way set associative so 16 blocks will divided in 4 sets of 4 blocks each.
We apply (address mod 4) function to decide set.

set 0	0	48	0	mod 4 = 0 *
	4	32	255	mod 4 = 3 *
	8	8	1	mod 4 = 1 *
	216	92	4	mod 4 = 0 *

Set 1	1	1	3	mod 4 = 3	*
	133	133	8	mod 4 = 0	*
	129	129	133	mod 4 = 1	*
	73	73	159	mod 4 = 1	*

Set 2	216	mod 4 = 0	*
	129	mod 4 = 1	*
	63	mod 4 = 3	*
	8	mod 4 = 0	*

Set 3	255	155	96	mod 4 = 0	*
	3	3	32	mod 4 = 0	*
	159	159	73	mod 4 = 1	*
	63	63	92	mod 4 = 0	*
			155	mod 4 = 3	*

All ~~sta~~ "*" are misses S1 in first stage and S2 in the second. In the second stage. 216 is not present in cache.

∴ (D) → 216 → (4) Ans.

Ques 5) Types of Parallelism :→

(1) Available and utilized parallelism →

Architectures, compilers and operating frameworks have been striving for more than two decades to extract and use as much parallelism as available to speed up computation.

(2) Data Parallelism →

It is inherent only in a restricted set of problems, such as scientific or engineering calculations or image processing. It provides growth to massively execution for the data parallel element of the computation.

(3) Functional Parallelism →

It is that type of parallelism that raise from the logic of a problem solution. It occurs in all formal descriptions of problem solutions, such as flow diagram, data flow graphs etc.

Fixed grained are actually detailed description which deals with the much smallel components which are in actual composed by the much large components.

Coarse grained systems are consisting of fewer components which are obviously more than the original one but are much lesser than the fine-grained, but the size of components is much more (high/more) than the fine grained subcomponents of the system

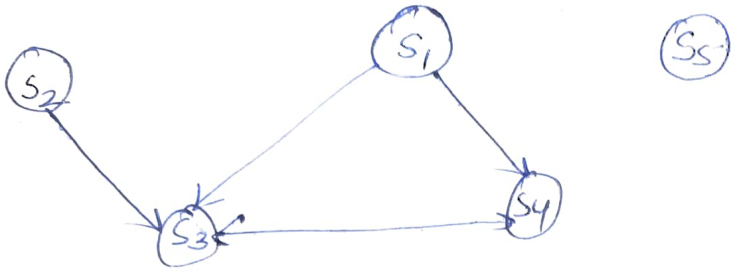
Examples of fixed are connection mechanism, J-machine etc.

Ques 4)

Dependencies →

S_1 to S_3	Statement 3 is output dependent on statement 1.
S_1 to S_2	No dependency
S_1 to S_4	Statement 4 is flow dependent on statement 1
S_1 to S_5	No dependency
S_2 to S_3	Statement 3 is flow dependent on statement 2
S_2 to S_4	No dependency
S_2 to S_5	No dependency
S_3 to S_3	Statement 3 is flow dependent on its elf
S_3 to S_4	statement 4 is flow dependent on statement 3.
S_3 to S_5	No dependency
S_4 to S_5	No dependency.

Dependency Graph ⟹



Ques 6) The main difference between multiprocessor and multicomputer is that the multiprocessor is a system with two or more CPUs that are capable of performing multiple tasks at the same time while a multicomputer is a system with multiple processors that are connected via an interconnection network to perform a task.

There are 2 types of multiprocessors called shared memory multiprocessor and distributed memory processor. The processors communicate with each other using reading and writing to the memory. It is called the symmetric multiprocessor system.

A multicomputer whereas can be used for distributed computing. It is easier and cost efficient to build a multicomputer than a multiprocessor. On the other hand, programming a multicomputer is difficult.

It is easier to program a multiprocessor compared to a multicomputer. Furthermore, it is easier and cost effective to build a multicomputer than a multiprocessor and, while multiprocessor supports distributed computing.

Ques 7)

S.NO	TOPIC	PIPE-LINED SYSTEM	NON-PIPELINED SYSTEM
(1)	working	In this, multiple instructions are overlapped during execution.	In this processes like decoding, fetching, execution and writing memory are merged into a single unit or a single step.
(2)	Execution Time	Many instructions are executed at the same time and execution time is comparatively less.	Only one instruction is executed at the same time is comparitively higher.
(3)	Dependency on CPU scheduler	The efficiency of the pipeing system depends upon the effectiveness of the CPU scheduler.	The efficiency is not dependent on the CPU scheduler
(4)	CPU cycles needed	Execution is done in fewer CPU cycles.	Execution requires more number of CPU cycles. Comparitively.

The maximum speedup comparing with non-pipelined processor is $3005 / (1 + 6 * 100) = 5$ times.

It means that all stages of 5-stage pipeline are always busy (no stalls) during the task segment execution

Ans 8Y

The three different types of hazards in computer architectural pipelining are :—

1. Structural
2. Data
3. Control

Structural Hazard →

Hardware resource among the instructions in the pipeline cause structural hazards. Memory, a GPR register, or an ALU all be used as resource here. When more than one instruction in the pipe requires access to the very same resource in the same clock cycle.

Data Hazard →

Data Hazards in pipelining emerge when the execution of one instruction is dependents on the results of another instruction that is still being processed in the pipeline.

Branch Hazard →

They are caused by branch instructions and are known as control hazards. The flow of program/instruction execution is controlled ~~control~~ converted into one of the branch instruction variations. As a result, the decision to execute one instruction is reliant on the result of another instruction, such as a conditional branch, which examines the conditions consequent value a conditional hazard develops.