Micro Controller: programming and Interfacing

	SAYS !					
	And the territory of the second					
.27	Micro Controller	Micro Processor.				
Def:		The thoughton .				
	- It is a chip optimized to	- It is a controlling unit of				
	Ontrol electronic devices.	a micro-computer wrapped				
2. 3		unside a small chip				
25-1-14	condition in the second se	the same in the sa				
Components						
	Contains a CPU, memory	- Only contains Central				
	and I/O all integrated into	- Only contains Central perocessing Unit				
	one chip	Carlos Carlos Carlos				
	C .	District sommer from				
Usae	en in which is the formation is	the said of the said the				
	- Used in embedded systems	- Used in personal computers				
	atilities continued	a B was figures of a				
Bus	Structure	and a grilled the file				
	- Has an internal controlling	- Uses an external Bus.				
· ·	Bus	to interface with RAM, ROM,				
	fords; will the Mr to cold to in	months etc. was at something or				
100	of 1000					
Avel	ritecture used					
1	- Harvard architecture	- Von Neumann model				
1:0405	- Straight-forward with a	- Complicated with				
	lewer instructions to	a lot of instructions				
	Straight-forward, with & fewer instructions to process	- Complicated, with a lot of instructions to process				
	overe the city to for para	of weat one that with				
	-In expensine	* Expensine				
1	total total	and winder on a finite				
	Power Consumption - how	- high.				

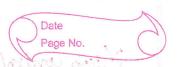
General RAM ROM 2/0 Time Serial com port Port Port

Perpose Address Bus

General purpose Micro processor

CPU	RAM	ROM
1/0 ADC	Times	Scrial COM port

Micro Paracesson Controller



8	Embedded System	1/ doogle
	An Embedded System is	
· ·	a combination of a computer processor,	computer memory
-	and input foutput, peripheral devices	-) that has a
	dedicated function within a larger	
The second	electrical system	The factor of the state of the
9	0	
	Criteria for choosing a micro-controller	// born kleter
		emperanto
î)	speed of the MC; does it meet the a	emanels required.
ü)	Speed of the MC; does it meet the a The type of packaging (eg. dual is	live, Grad flat etc).
w)	on chip RAM,/ROM.	
iv)	Power consumption.	
v)	No. of 2/0 pens; determines the v	o. of i/o devices it can cont
	Cost per unit.	
V(1)	Capability & ease of upgradation	, scalabilety.
VIII)	Availability of software & hardware	dw tools
5-7	Eg - Emulators, debuggers	Compuers etc.
×1	Wide availability and reliable sou adheres to current standards; will to	Les jor the Mic.
	davines is current sourceases, will to	hear future.
÷		Avointections were
1 21/22	Harvard and von Neumann architectus	Mazidi 1/ pg 37
	The state of the s	
	Every we/wil must has memory space	e to store program Code
- Lagrage	and data. While code provides	instructions to the CPU,
2 F	Every pic/pil must has memory space and data. While code provides data provides the information to be	proussed.
	The CPU uses buses to access the co	de ROM & data RAM
	memory to access both code and da	ters used the same
	bus to access both code and da	ta.



Such an architecture is commonly referred to as von Neumann (princeton) architecture. This meant that, the process of accessing the code & data would cause them to get in each other's way & slow down the processing of the CPU, because each had to wait for the other to finish fetching.

To speed up processing, some CPUS use what is called thanked architecture. In this architecture, there are I separate buses for code and data memory. Thus there is a need for four sets of buses:

ii) a set of data-buses to carry data infout of the CPU iii) a set of address-buses for accessing data momory. iii) a set of puses to carry code into the CPU.

iv) a address-bus to access code.

This is easy to impliment inside an IC thip such as a piC where both data RAM and Code ROM are on-Chip and distances are on micron /millimeter scale. But implimenting this for systems such as X86 IBM PC-type computers is very expensive because the RAM and ROM that hold the data and code are external to the CPU. Seperate wire traces for code and data will make it the motherboard large and expensive. (more refer)

CPU Cole Data

Peo
P9

P9

Non Neumann

Architecture

Memory

Nemory



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		all the same	Harvard	Architectur			
26t	CPU	aid on 8 bit in	CARRY STATE	54 T			
	Ao.	- Code	- 6-134010				
memory Arg	19 A19	Ais memory	K STATE OF THE STA				
14 1 10 10 14	Solla Do	B () 0	7	3			
	D ₂ D ₇						
2.110 10 to 10 101	V - 11/4 V	mod fill home	-74				
2 man 1 h	ns diagra	codle data		1775			
Code + data	Jano si	mem mem	add	b			
data bus 1 Taddbu	s add	data buses	ana	рссу			
UPD DAT & CRU AND	MAN ST	CPU	/38				
	N 2 34 ANN	2/0 devices					
210 deries	500 LUIG	10 desites	<u> </u>				
Conference 14 m		Harvard.					
Von Neumann		Flawasi	0	- 10 l			
n in in it is all a	T AT STA	EM data star AM	1	337 1			
a KOM are elicoting	100 <u>(001</u> 100 - (001	N NOW YOUR WAY WAS	The state				
AVR and Avduina	M Manage	1 1200an \$180 40	1				
- Advanced	Mis bus	& Wolfen RISC MC	· vi vi	v 63			
Advanced	Voque	The state of the s		And the			
Cover to Cos AVR3	Except for AVR32 (a 32 bit µC), AVRS are all 8 bit µ?						
magning the	CPU can	work on onl	y 8 bits	of data			
at a time		V	0	U			
	1						
Classifications	(Broad)		tures				
i) Mega			RISC single				
ii) Ting	1-12	3 Harve	erd archite	turl			
in Speeld purpe	se	7 on chap	code ROM,	data RAM,			
iv) Classic				mes, 2/0 p			
		3 some	additional ;	features like			
		ADC,	PWM & SU	ial interface			
	<u> </u>	such a	OSART CA	N, USB etc			