F] Machine Control instⁿs :

(1) EI
(2) DI
(3) SIM
(4) RIM
} Hardware interrupts

(5) HLT ; [Halt the processor]

[NAM] [I-BI] [NFAC]

Sequence of operation :

5173	X
5174	HLT
5175	Y

mem.

fig. (1)

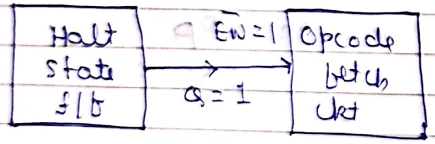


fig (2)

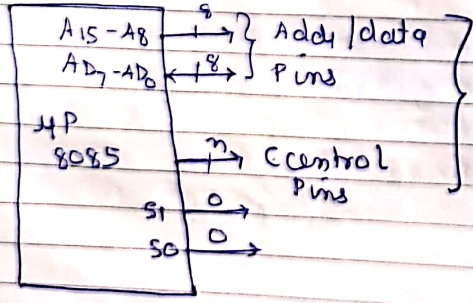
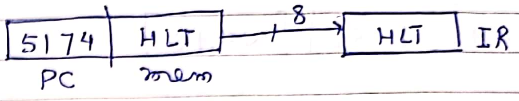
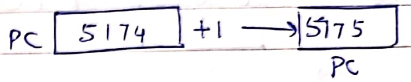


fig (3)

(i) Opcode fetch and decode :-





The opcode of HLT instⁿ is transferred from IR to ID & HLT instⁿ unit is selected (decoded)

(ii) Execution :

a) When µP execute HLT instⁿ, then HLT state flf is set (fig 2). As Q=1, so $\overline{EN}$=1 and opcode fetch ckt. is disabled. Hence, after HLT inst µP will not read opcode of any other instⁿ.

b) In HLT state µP will keep address, data, control pins floating i.e µP will not use external address, data, control buses.

c) In HLT state µP will O/P status signals S_1S_0 = 00 to inform external device that µP is in HLT state. Hence any external device can use byte address, data, control buses if required.

µP can be made to exit from Halt state by giving any of the following 3 signals :
a) Reset signal
b) Interrupt signal
c) HOLD signal.

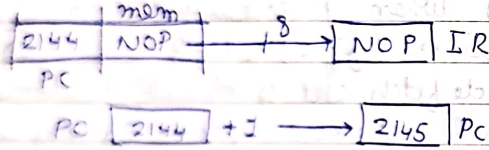
(6) NOP ; [No operation]

[NAM] [1-BI] [NFAC]

Sequence of operation of NOP :

2143	X
2144	NOP
2145	Y
	mem

(i) Opcode fetch and decode :



The opcode of NOP inst^n is transferred from IR to ID and NOP inst^n unit is selected (decoding).

(ii) Execution NOP inst^n does not perform any operation

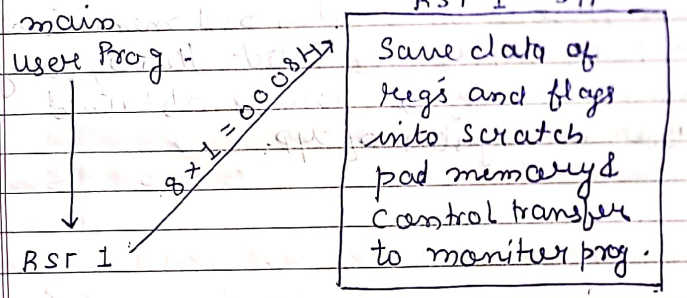
For opcode fetch & decode of NOP inst^n, four clock cycles time is reqd. but as NOP inst^n does not perform any operation, so four clk cycles of time of 4P is wasted. NOP inst^n is used in delay programs to waste four clk cycles time of 4P.

[4] Input and Output Instructions

(1) IN Port Address } Refer Interfacing of
(2) OUT Port address } IO device with 4P

Difference bet^n RST 1 and HLT as Interrupting inst^n :

1. RST 1 / RST 5 (Break point technique)



If RST 1 inst^n is given as a last inst^n of main user program, then after executing user program, 4P execute inst^n RST 1.

When 4P execute RST 1, then 4P will branch from main user prog. to standard sub prog of RST 1. This sub prog. is used to save the results obtained in different registers of 4P into reserved mem. loc^{n}s and it is called scratch pad memory.

If REG key is pressed, then the results of different registers present in scratch pad memory is displayed on 7-Seg. display connected. Hence

user can verify the results obtained in different registers of µP.

2. HLT : If HLT instn is given in the last of user prog. then after executig user prog, in the last µP will execute HLT instn. After HLT instn µP will not execute any other instn. Hence, the results obtained in different regs of µP are not saved into scratch pad memory so, scratch pad mem will contain garbage value. If REG key is pressed, then the garbage value present in scratch pad mem is displayed on 7-seg display connected. Hence, programmer cannot verify the results obtained in different registers of µP.