LECTURE 8,9: INSTRUCTION CYCLE & THEIR TIMING DIAGRAMS

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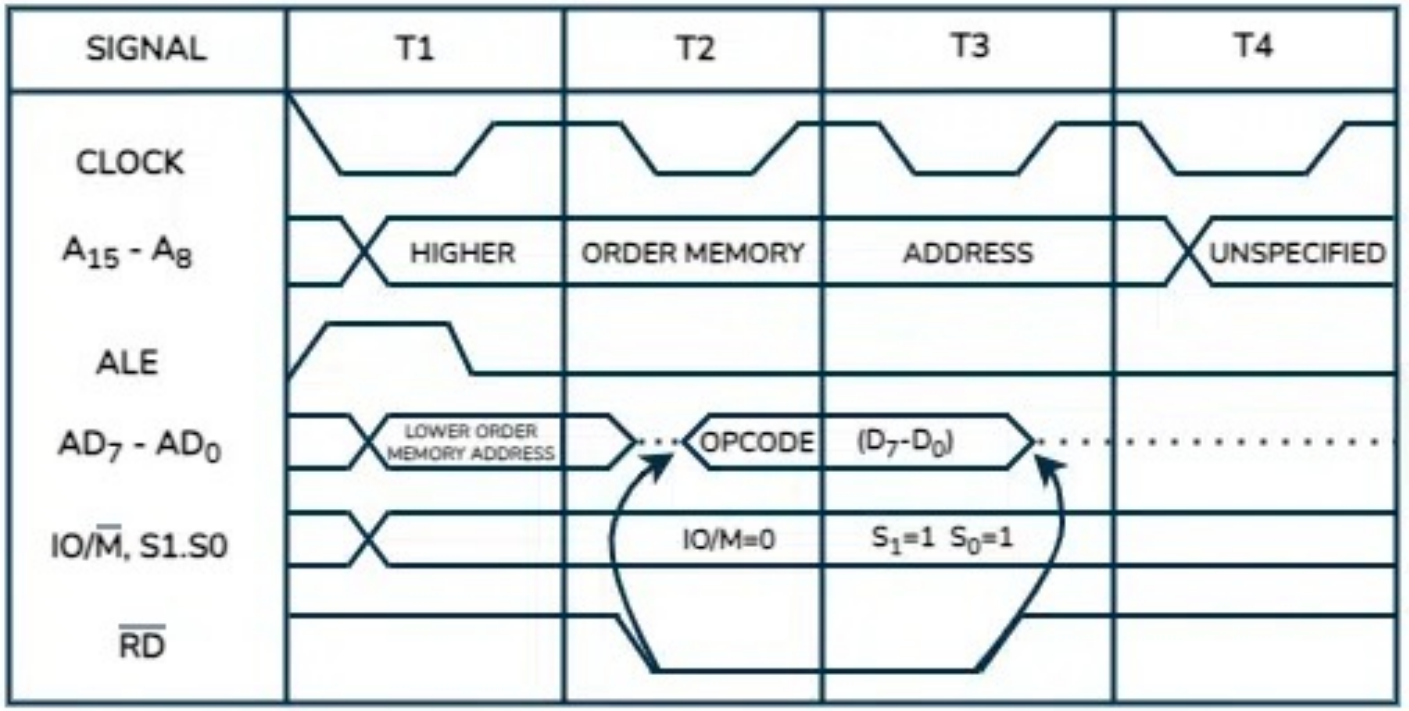
OPCODE FETCH

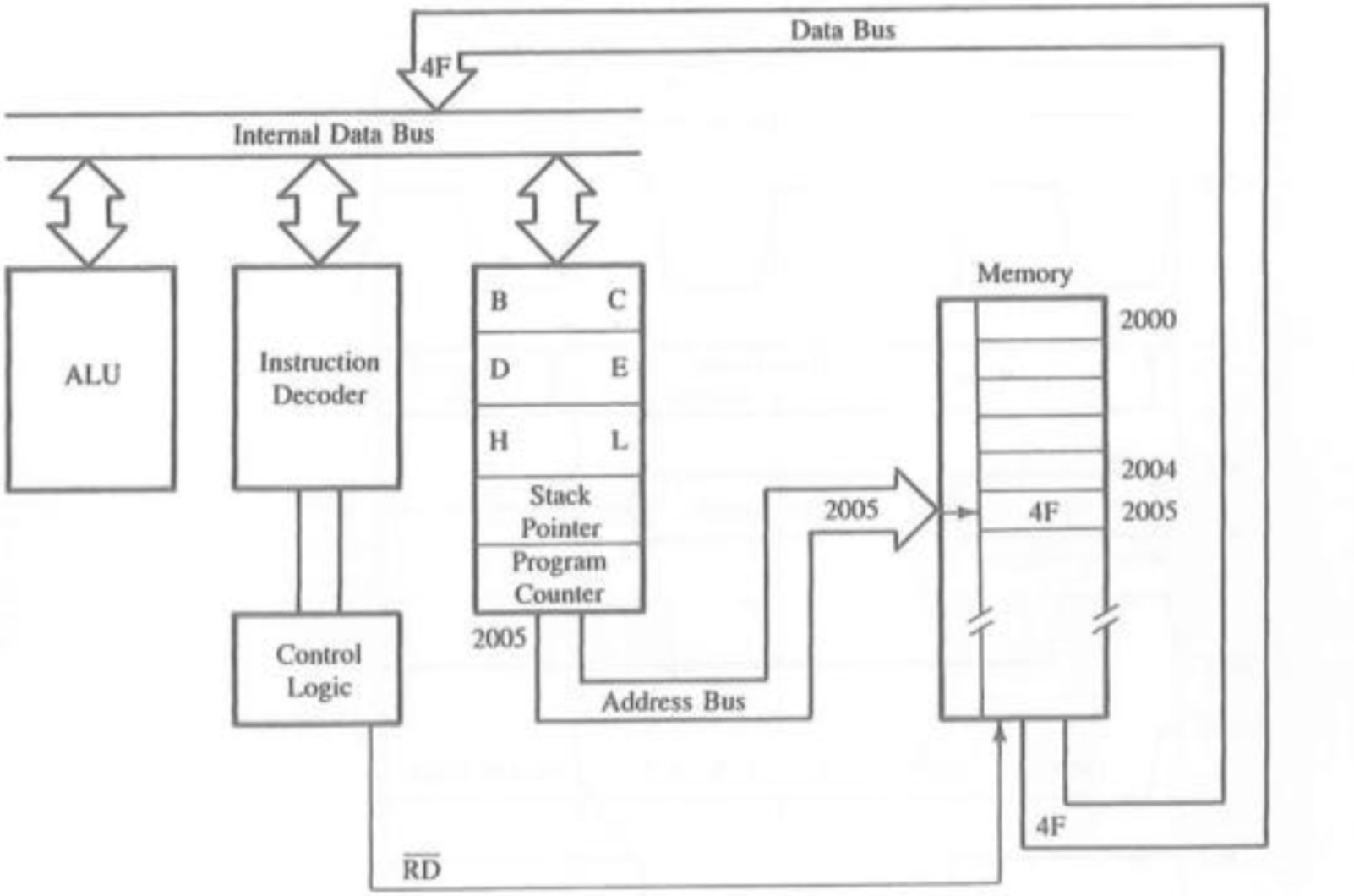
TABLE 4.1
8085 Machine Cycle Status and Control Signals

Machine Cycle	Status IO/$\overline{M}$	Status S_1	Status S_0	Control Signals
Opcode Fetch	0	1	1	$\overline{RD} = 0$
Memory Read	0	1	0	$\overline{RD} = 0$
Memory Write	0	0	1	$\overline{WR} = 0$
I/O Read	1	1	0	$\overline{RD} = 0$
I/O Write	1	0	1	$\overline{WR} = 0$
Interrupt Acknowledge	1	1	1	$\overline{INTA} = 0$
Halt	Z	0	0	$\overline{RD}$, $\overline{WR}$ = Z and $\overline{INTA}$ = 1
Hold	Z	X	X	
Reset	Z	X	X	

NOTE: Z = Tri-state (high impedance)
X = Unspecified



Q: Illustrate the steps and timing diagram of data flow when the instruction code 01001111 (4F---MOV C,A), stored at location 2005 is being fetched

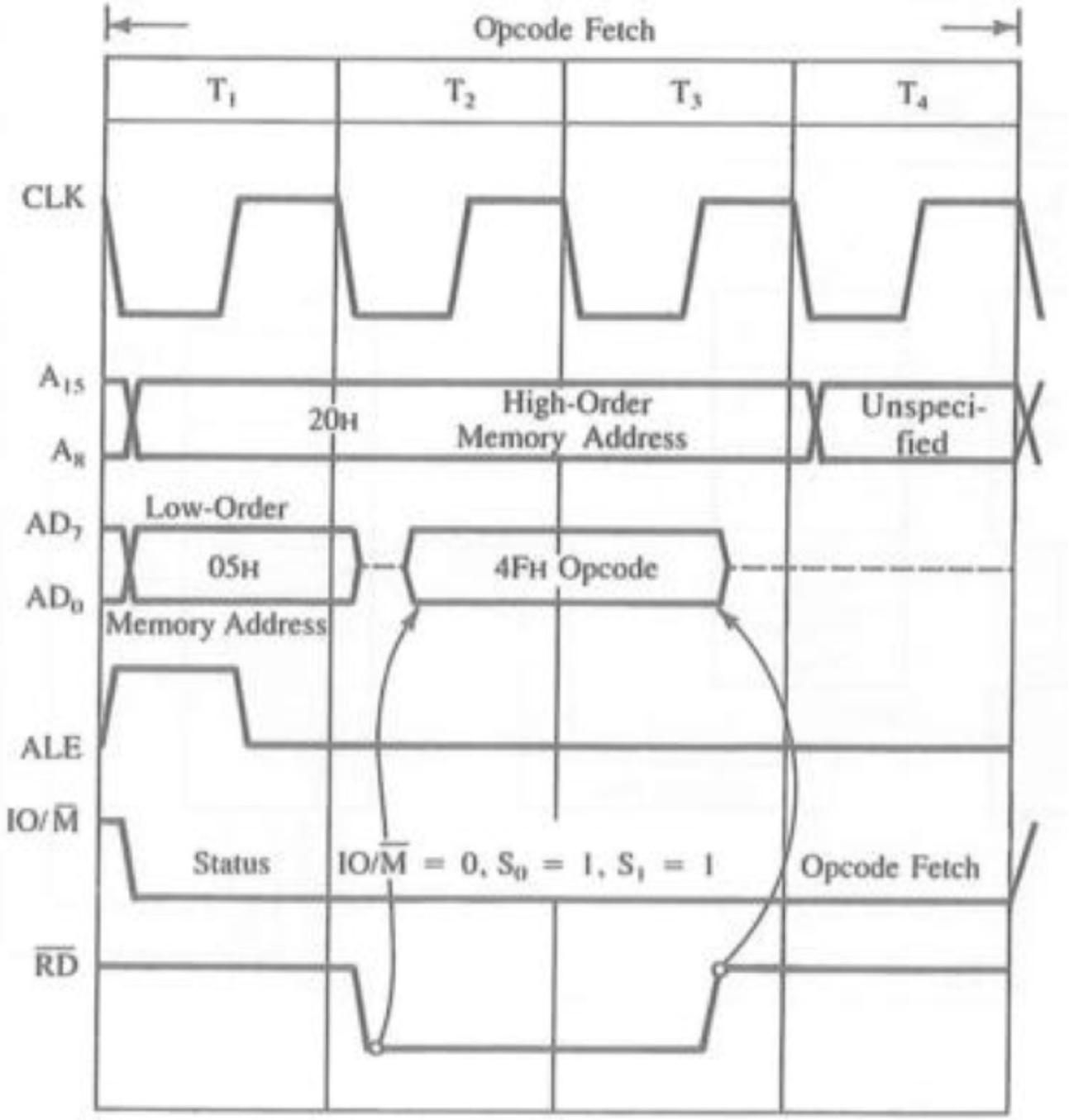


Step1: Up places 16-bit address from PC to address bus (1 clock period)

Step2: Control unit sends RD* signal (2 clock periods)

Step3: Byte from memory is placed on data bus

Step4: The byte is placed on instruction decoder (1 clock period)



Observations:

1. Machine code 4F H is a one-byte instruction. It copies the content of accumulator into register C.
2. 8085 up requires 1 external operation – fetching the machine code* from the memory
3. The entire operation -- fetching, decoding, executing --requires 4 clock periods

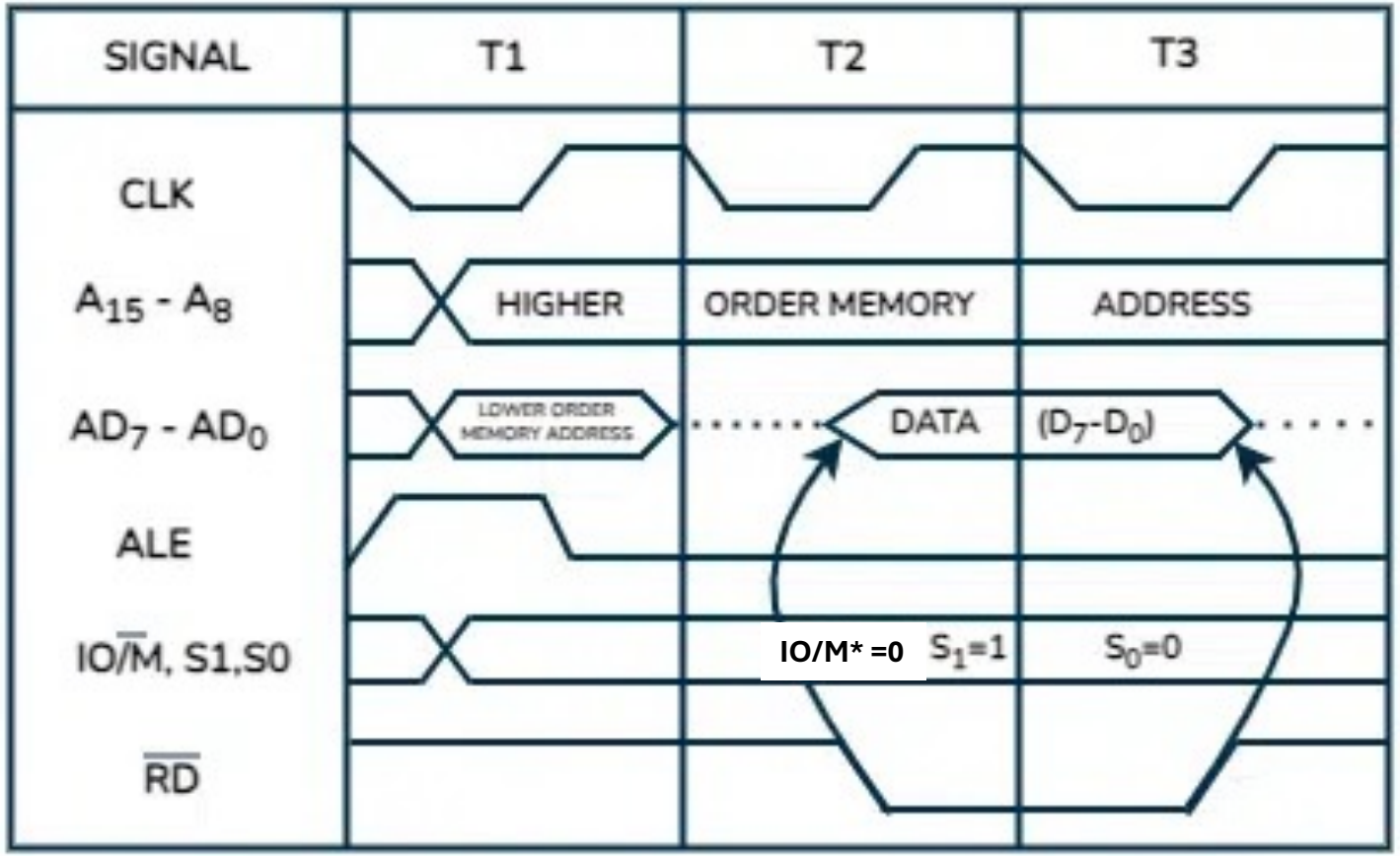
Definitions

Instruction cycle: is defined as the time required to complete the execution of an instruction. The 8085-instruction cycle consists of 1 to 6 machine cycles.

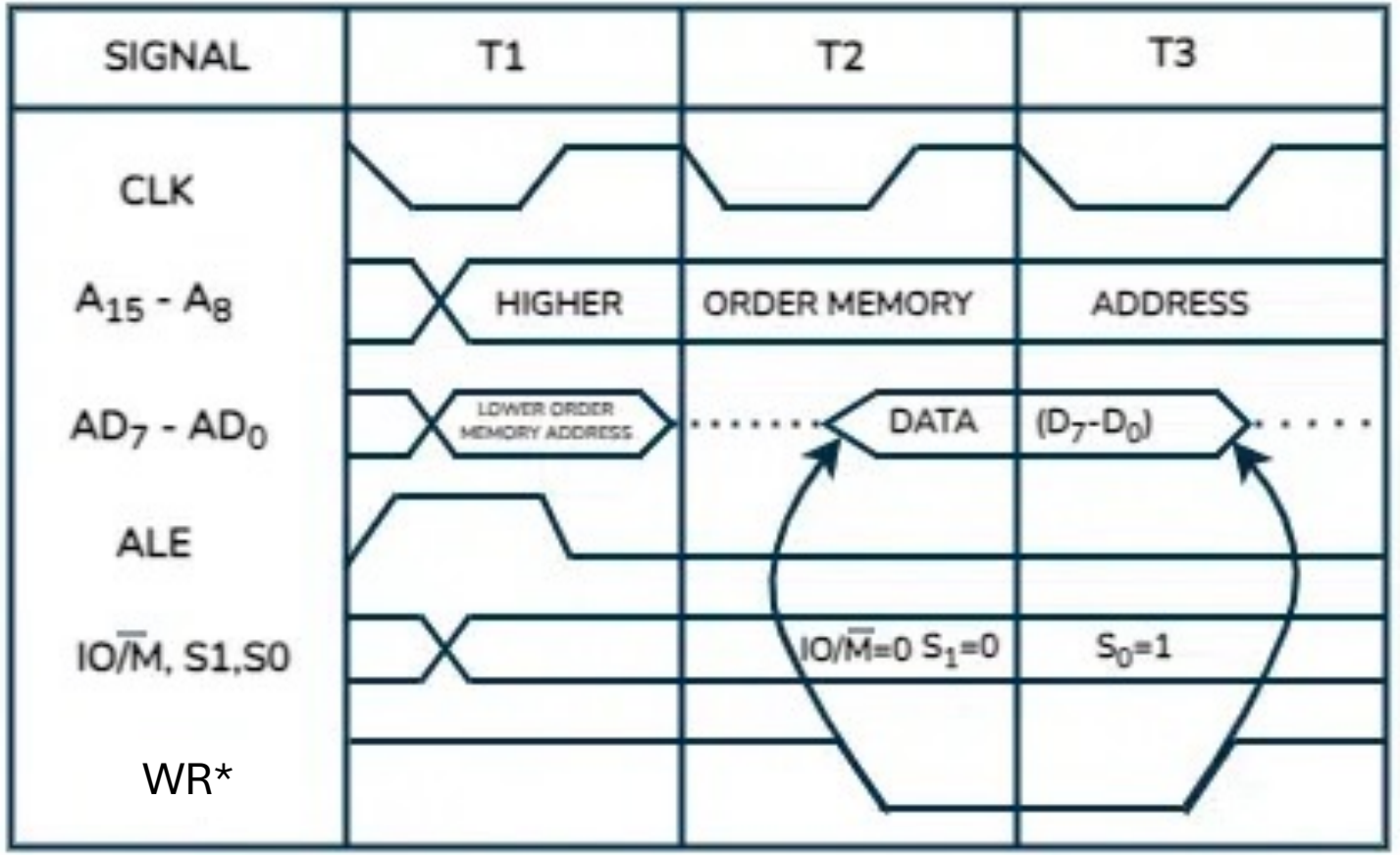
Machine cycle: is the time required to complete one operation of accessing memory, I/O devices or acknowledging an external request. This cycle may consist of 3 to 6 T-states.

T-state: is defined as one subdivision of the operation performed in one clock period. The term T-state and clock period are used interchangeably.

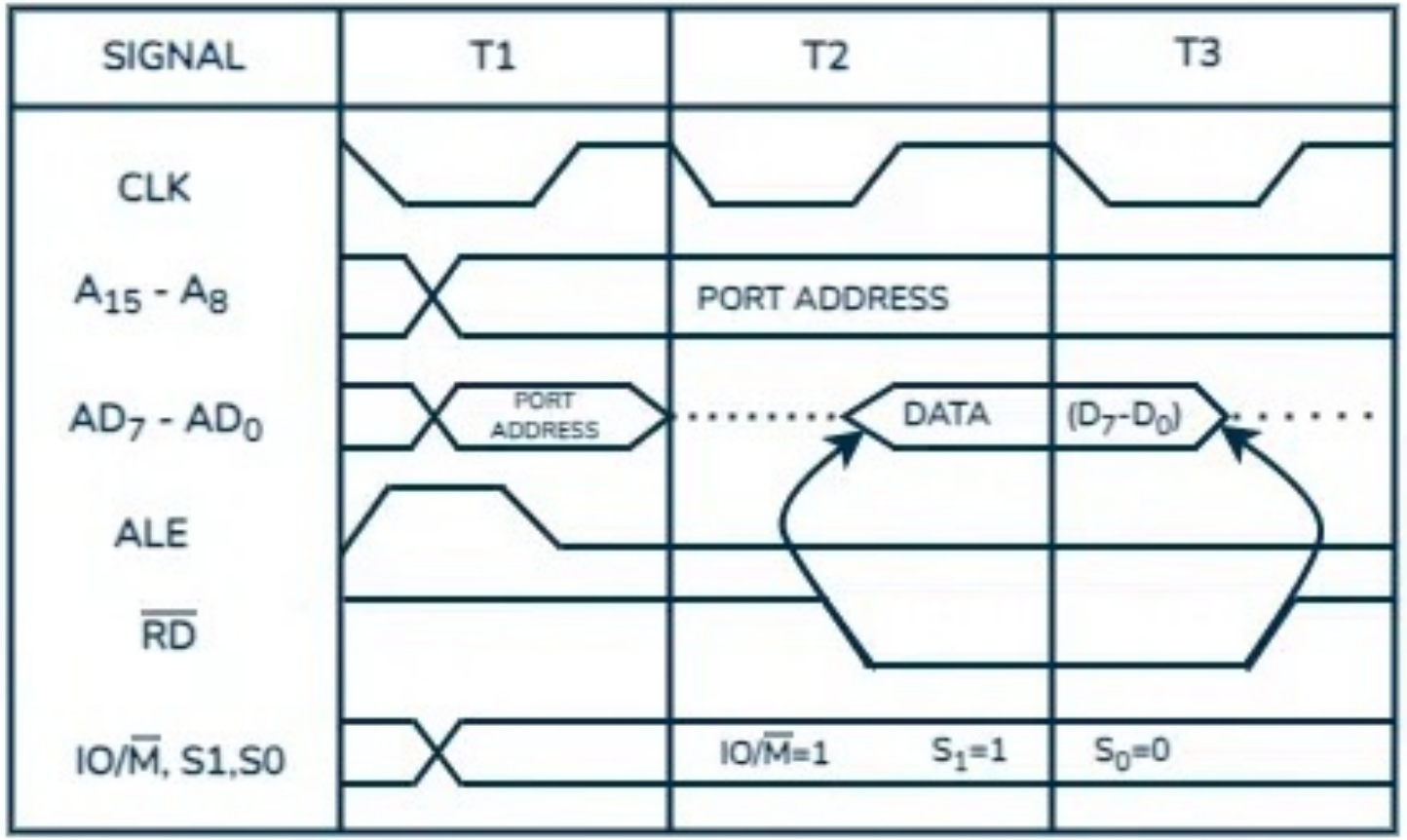
MEMORY READ


SIGNAL
T1
T2
T3
CLK
A15 - A8
HIGHER
ORDER MEMORY
ADDRESS
AD7 - AD0
LOWER ORDER MEMORY ADDRESS
DATA
(D7-D0)
ALE
IO/M, S1,S0
IO/M* =0
S1=1
S0=0
RD

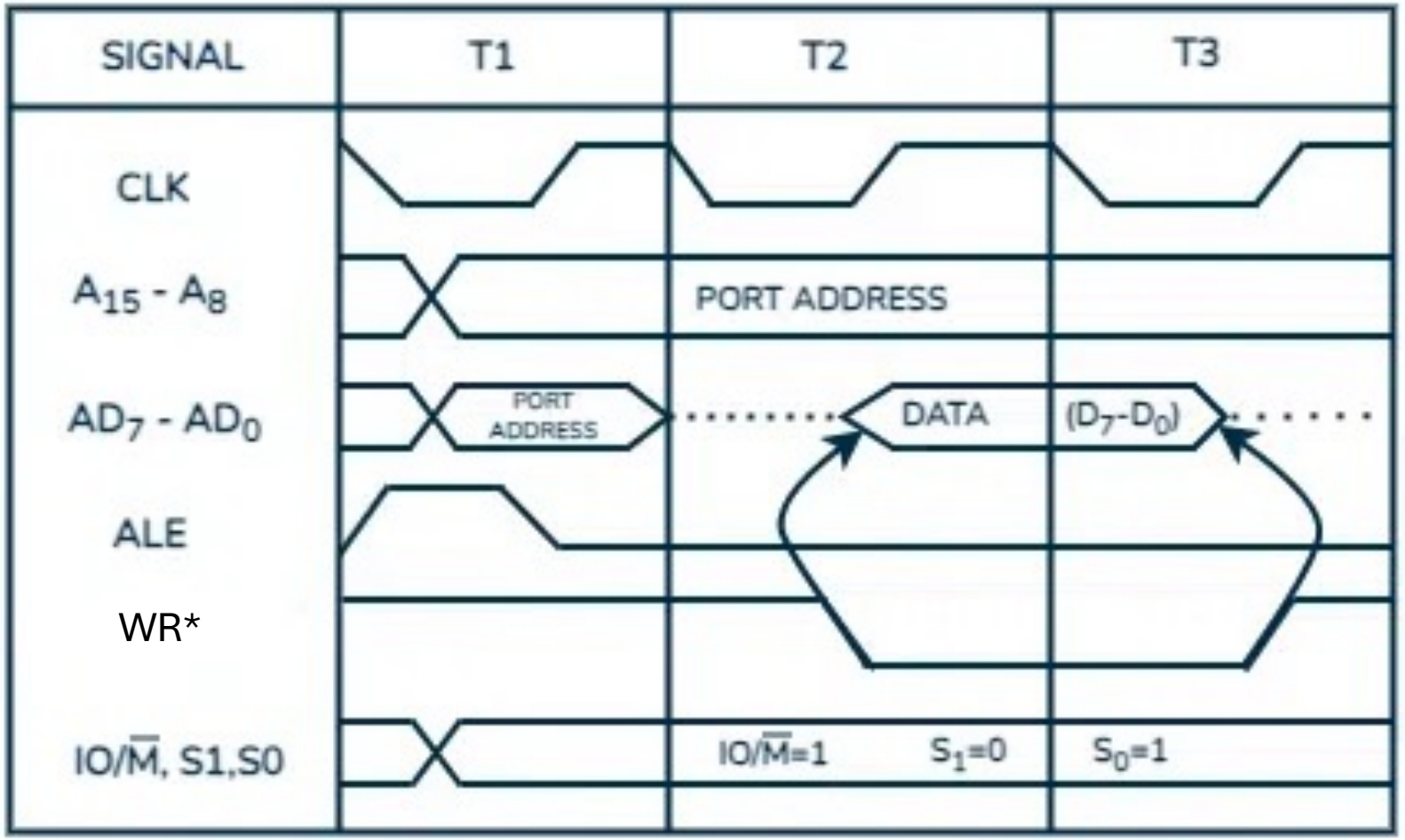
MEMORY WRITE



I/O READ


SIGNAL
T1
T2
T3
CLK
A15 - A8
PORT ADDRESS
AD7 - AD0
PORT ADDRESS
DATA
(D7-D0)
ALE
RD
IO/M, S1,S0
IO/M=1
S1=1
S0=0

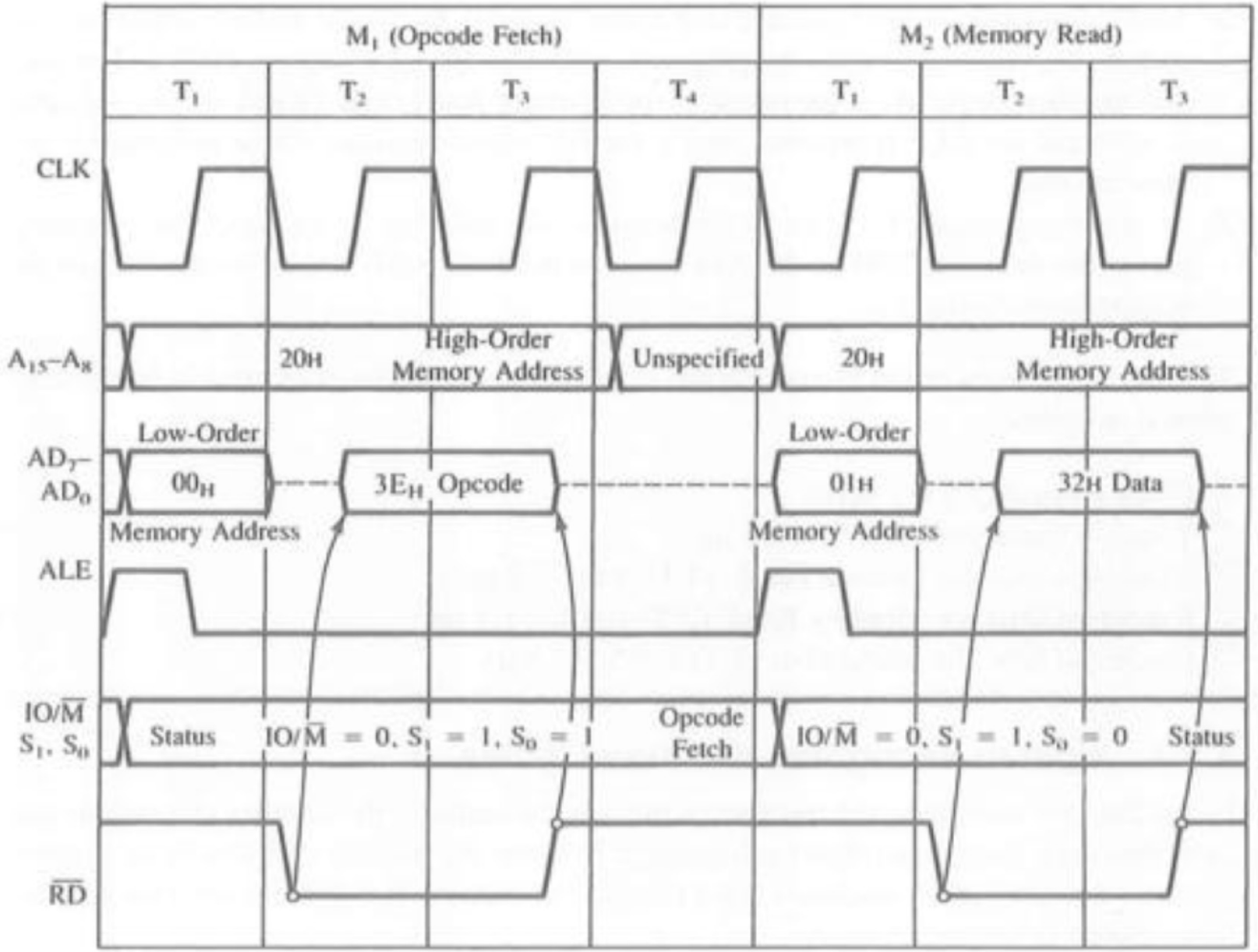
I/O WRITE


SIGNAL
T1
T2
T3
CLK
A15 - A8
PORT ADDRESS
AD7 - AD0
PORT ADDRESS
DATA
(D7-D0)
ALE
WR*
IO/M, S1,S0
IO/M=1
S1=0
S0=1

Timing Diagram of MVI A, 32 H

- Loading opcode 3EH from memory 2000H. (Operation Code Loading Machine Cycle)
- Read (move) data 32H from memory 2001H. (memory reading).

Address	Mnemonics	Opcode
2000H	MVI A,32H	3EH
2001H		32H

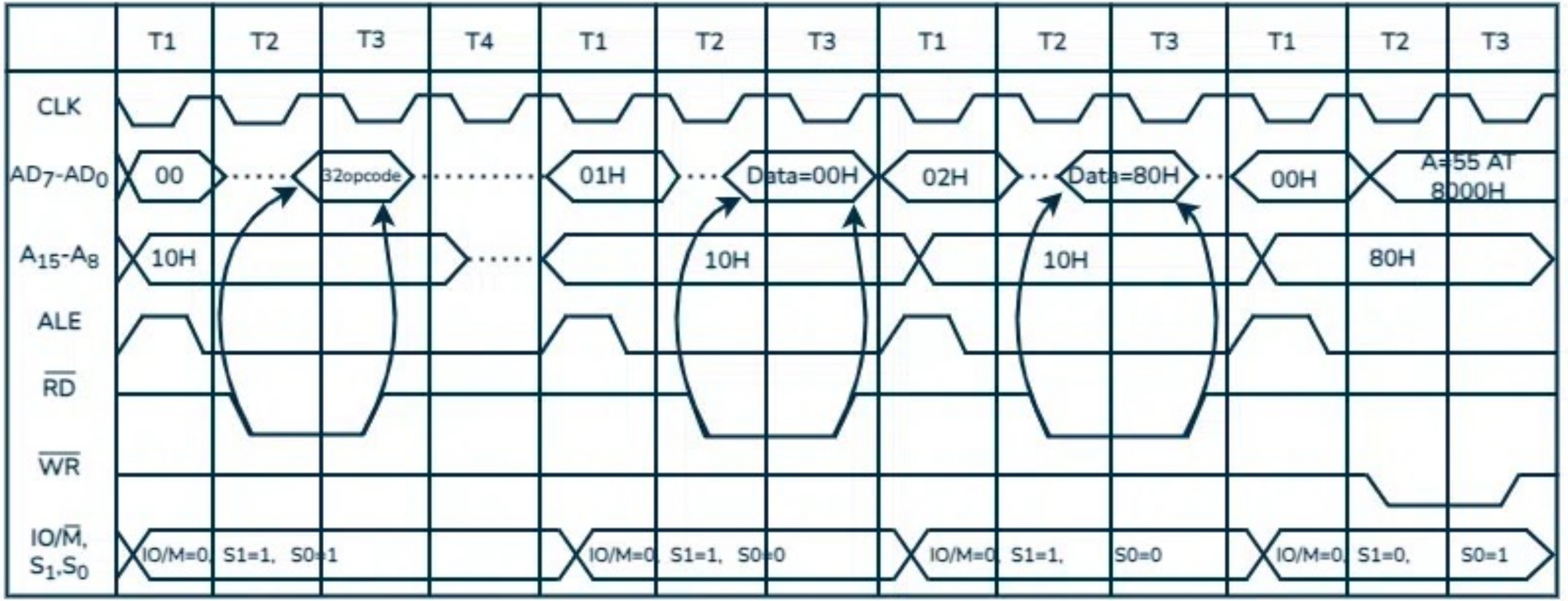

M1 (Opcode Fetch)
M2 (Memory Read)
T1
T2
T3
T4
T1
T2
T3
CLK
A15–A8
20H
High-Order Memory Address
Unspecified
20H
High-Order Memory Address
Low-Order
AD7–AD0
00H
3EH Opcode
01H
32H Data
Memory Address
Memory Address
ALE
IO/M
S1, S0
Status
IO/M = 0, S1 = 1, S0 = 1
Opcode Fetch
IO/M = 0, S1 = 1, S0 = 0
Status
RD

Timing Diagram of STA 8000H

Address	Mnemonics	Opcode
1000H	STA 8000H	32H
1001H		00H
1002H		80H

Let, A = 55H

Machine Cycle 1	Place address 1000H on address bus and fetch the opcode 32H
Machine Cycle 2	Memory Read. Places address 1001H on address bus and gets low order byte 00H
Machine Cycle 3	Memory Read. Places address 1002H on address bus and gets high order byte 00H
Machine Cycle 4	• **Memory Write. 8085 place address 8000H on address bus and identifies the operation as memory write.** • **Places the contents of accumulator on data bus and asserts WR* signal.** • **During the last T-state, the contents of data bus are placed in memory location 8000H.**


T1
T2
T3
T4
T1
T2
T3
T1
T2
T3
T1
T2
T3
CLK
AD7-AD0
00
32opcode
01H
Data=00H
02H
Data=80H
00H
A=55 AT
8000H
A15-A8
10H
10H
10H
80H
ALE
RD
WR
IO/M,
S1,S0
IO/M=0, S1=1, S0=1
IO/M=0, S1=1, S0=0
IO/M=0, S1=1,
S0=0
IO/M=0, S1=0,
S0=1

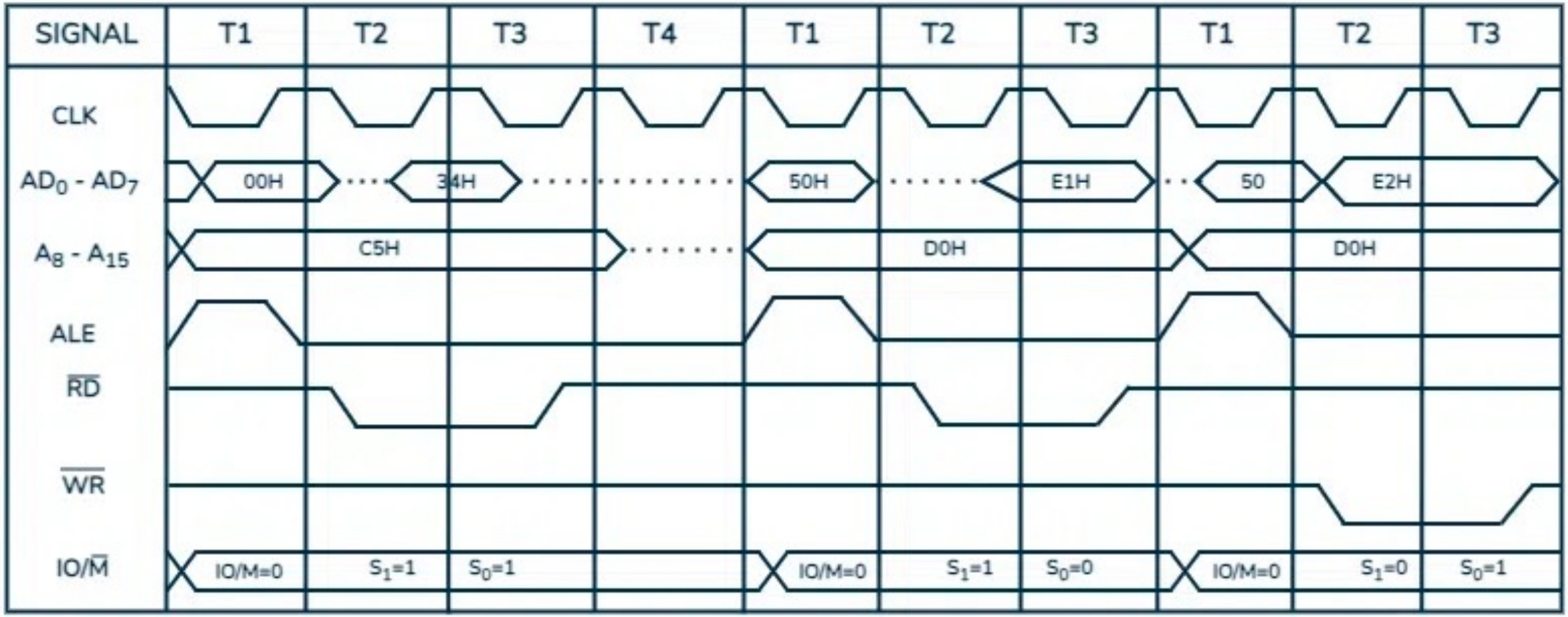
Timing Diagram of INR M

Address	Mnemonics	Opcode
C500H	INR M	34H

H	L
D0	50

MEMORY

D04F	01
D050	E1
D051	32


SIGNAL
T1
T2
T3
T4
T1
T2
T3
T1
T2
T3
CLK
AD0 - AD7
00H
34H
50H
E1H
50
E2H
A8 - A15
C5H
D0H
D0H
ALE
RD
WR
IO/M
IO/M=0
S1=1
S0=1
IO/M=0
S1=1
S0=0
IO/M=0
S1=0
S0=1

Questions for Practice:

1. Draw the timing diagram of the instruction MOV B,M. Assume necessary data.

2. Identify all the machine cycles and draw the last machine cycle of the instruction: LDA 2050H. Assume necessary data.

3. If the clock frequency is 5 MHz, how much time is required to execute an instruction of 18 T-states?

Note: Any operations which are performed inside the uP, does not require any machine cycle.

1. MVI B,15H

Machine Cycle	Address Bus	Data Bus	T-state
OF	PC	OPCODE	4
MR	PC+1	15	3

2. LXI B, 2000H

Machine Cycle	Address Bus	Data Bus	T-state
OF	PC	OPCODE	4
MR	PC+1	00	3
MR	PC+2	20	3

3. LDA 2000H

Machine Cycle	Address Bus	Data Bus	T-state
OF	PC	OPCODE	4
MR	PC+1	00	3
MR	PC+2	20	3
MR	2000	[2000]	3

4. STA 2000H

Machine Cycle	Address Bus	Data Bus	T-state
OF	PC	OPCODE	4
MR	PC+1	00	3
MR	PC+2	20	3
MW	2000	A	3

5. LHLD 2000H

Machine Cycle	Address Bus	Data Bus	T-state
OF	PC	OPCODE	4
MR	PC+1	00	3
MR	PC+2	20	3
MR	2000	[2000]	3
MR	2001	[2001]	3

5. SHLD 2000H

Machine Cycle	Address Bus	Data Bus	T-state
OF	PC	OPCODE	4
MR	PC+1	00	3
MR	PC+2	20	3
MW	2000	L	3
MW	2001	H	3

7. LDAX B

Machine Cycle	Address Bus	Data Bus	T-state
OF	PC	OPCODE	4
MR	BC	[BC]	3

8. STAX D

Machine Cycle	Address Bus	Data Bus	T-state
OF	PC	OPCODE	4
MW	DE	A	3

9. MOV B,C

Machine Cycle	Address Bus	Data Bus	T-state
OF	PC	OPCODE	4

10. ADD B

Machine Cycle	Address Bus	Data Bus	T-state
OF	PC	OPCODE	4

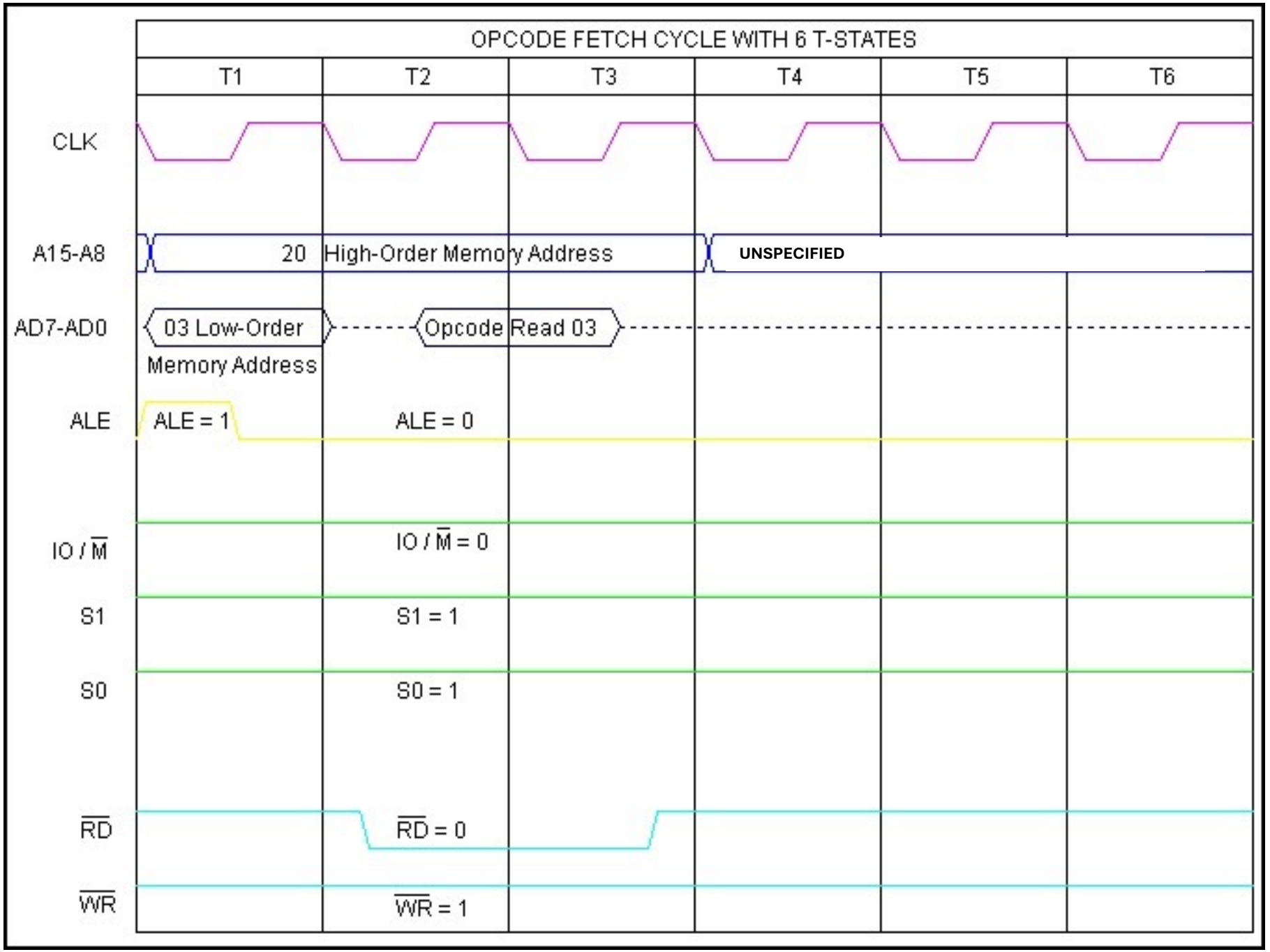
11. INR B

Machine Cycle	Address Bus	Data Bus	T-state
OF	PC	OPCODE	4

12. INX B

Machine Cycle	Address Bus	Data Bus	T-state
OF	PC	OPCODE	6

- **NOTE: If the opcode fetch consist of incrementing or decrementing of any register pair, then the opcode fetch for that instruction will be 6 T states.**
- **During T5 and T6 , 8085 performs stack write, internal 16 bit; and conditional return operations depending upon the type of instruction.**
- **One-byte instructions those operate on sixteen-bit data (16-bit operand) are executed in T5 and T6. For example, DCX H, PCHL, SPHL, INX H, etc.**


OPCODE FETCH CYCLE WITH 6 T-STATES
T1
T2
T3
T4
T5
T6
CLK
A15-A8
20
High-Order Memory Address
UNSPECIFIED
AD7-AD0
03 Low-Order Memory Address
Opcode Read 03
ALE
ALE = 1
ALE = 0
IO / M
IO / M = 0
S1
S1 = 1
S0
S0 = 1
RD
RD = 0
WR
WR = 1

Instruction involving memory pointer

13. MVI M,15H

Machine Cycle	Address Bus	Data Bus	T-state
OF	PC	OPCODE	4
MR	PC+1	15	3
MW	HL	15	3

14. MOV B,M

Machine Cycle	Address Bus	Data Bus	T-state
OF	PC	OPCODE	4
MR	HL	[M]	3

15. MOV M,B

Machine Cycle	Address Bus	Data Bus	T-state
OF	PC	OPCODE	4
MW	HL	B	3

16. INR M

Machine Cycle	Address Bus	Data Bus	T-state
OF	PC	OPCODE	4
MR	HL	M	3
MW	HL	M+1	3

17. ADD M

Machine Cycle	Address Bus	Data Bus	T-state
OF	PC	OPCODE	4
MR	HL	M	3

18. PUSH B

Machine Cycle	Address Bus	Data Bus	T-state
OF	PC	OPCODE	4
MW	SP-1	B	3
MW	SP-2	C	3

19. POP D

Machine Cycle	Address Bus	Data Bus	T-state
OF	PC	OPCODE	4
MR	SP	[SP]	3
MR	SP+1	[SP+1]	3

20. JMP 2000H

Machine Cycle	Address Bus	Data Bus	T-state
OF	PC	OPCODE	4
MR	PC+1	00 (Z)	3
MR	PC+2	20 (W)	3

21. JC 2000H

Machine Cycle	Address Bus	Data Bus	T-state
OF	PC	OPCODE	4
MR	PC+1	00 (Z)	3
MR	PC+2	20 (W)	3

If condition is TRUE, i.e. CF=1

Machine Cycle	Address Bus	Data Bus	T-state
OF	PC	OPCODE	4
Read memory (idle)	---	---	3

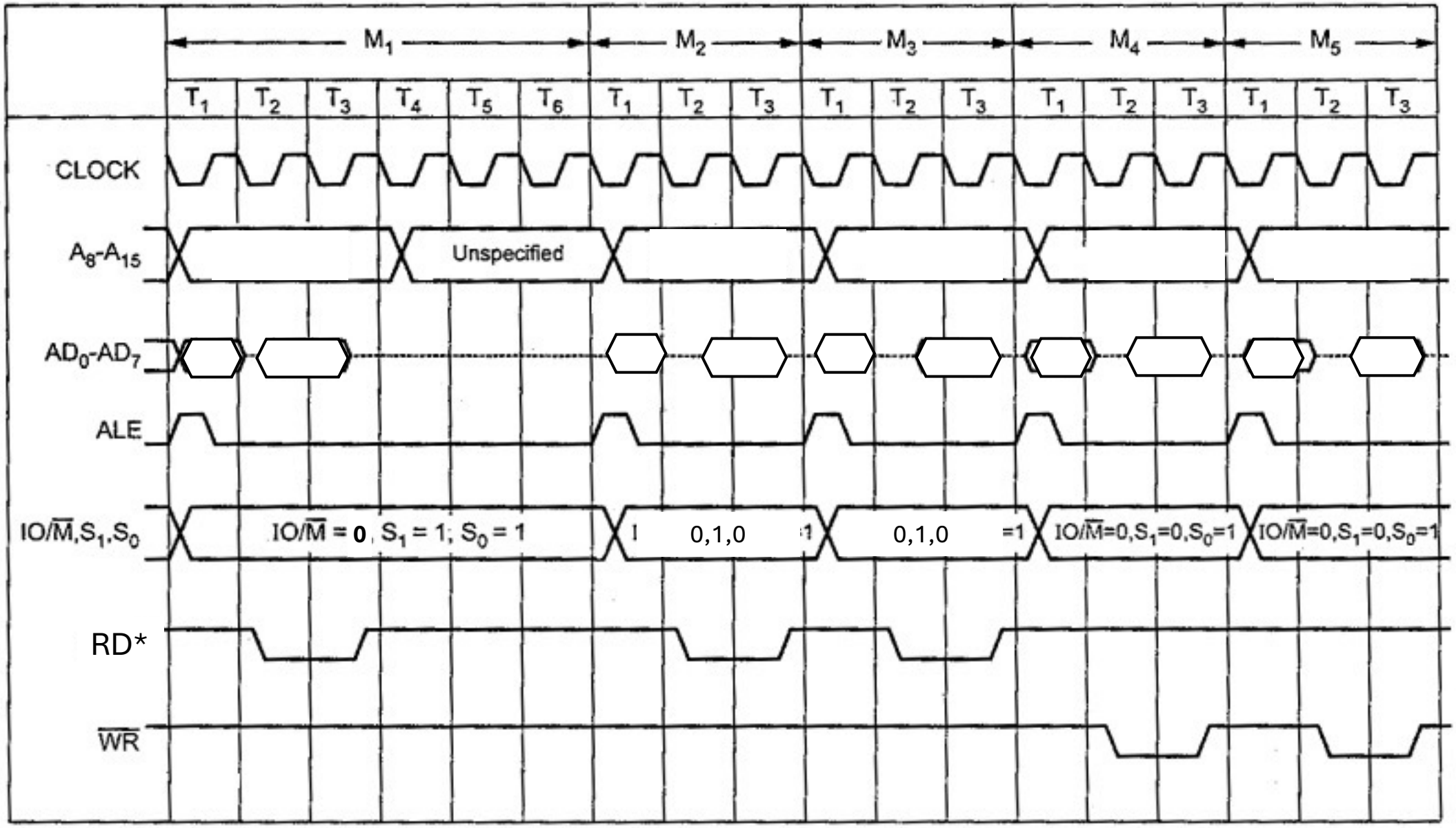
If condition is FALSE, i.e. CF=0

22. CALL 2000H

Machine Cycle	Address Bus	Data Bus	T-state
OF	PC	OPCODE	6
MR	PC+1	00 (Z)	3
MR	PC+2	20 (W)	3
MW	SP-1	PCH	3
MW	SP-2	PCL	3

23. RET

Machine Cycle	Address Bus	Data Bus	T-state
OF	PC	OPCODE	4
MR	SP	[SP]	3
MR	SP+1	[SP+1]	3



Timing Diagram of CALL Instructions

Fill in the missing entries

24. IN 20H

Machine Cycle	Address Bus	Data Bus	T-state
OF	PC	OPCODE	4
MR	PC+1	20	3
IOR	20H	[20H]	3

25. OUT 20H

Machine Cycle	Address Bus	Data Bus	T-state
OF	PC	OPCODE	4
MR	PC+1	20	3
IOW	20H	A	3

Machine Cycles:

1. Opcode Fetch
2. Memory Read
3. Memory Write
4. I/O Read
5. I/O Write

6. Interrupt Acknowledge Cycle:
• This cycle is executed when the microprocessor acknowledges an interrupt.
• It consists of 6 T-states and is initiated when the microprocessor responds to an interrupt request.

7. Bus Idle Cycle:
• In this cycle, the microprocessor's buses are not in use for memory or I/O operations.
• The buses remain idle while internal operations take place, such as in instructions that only modify internal registers.

26. DAD D

Machine Cycle	Address Bus	Data Bus	T-state
OF	PC	OPCODE	4
Bus idle	-----	----	3
Bus idle	-----	----	3

27. HLT

Machine Cycle	Address Bus	Data Bus	T-state
OF	PC	OPCODE	4+1

28. XCHG

Machine Cycle	Address Bus	Data Bus	T-state
OF	PC	OPCODE	4

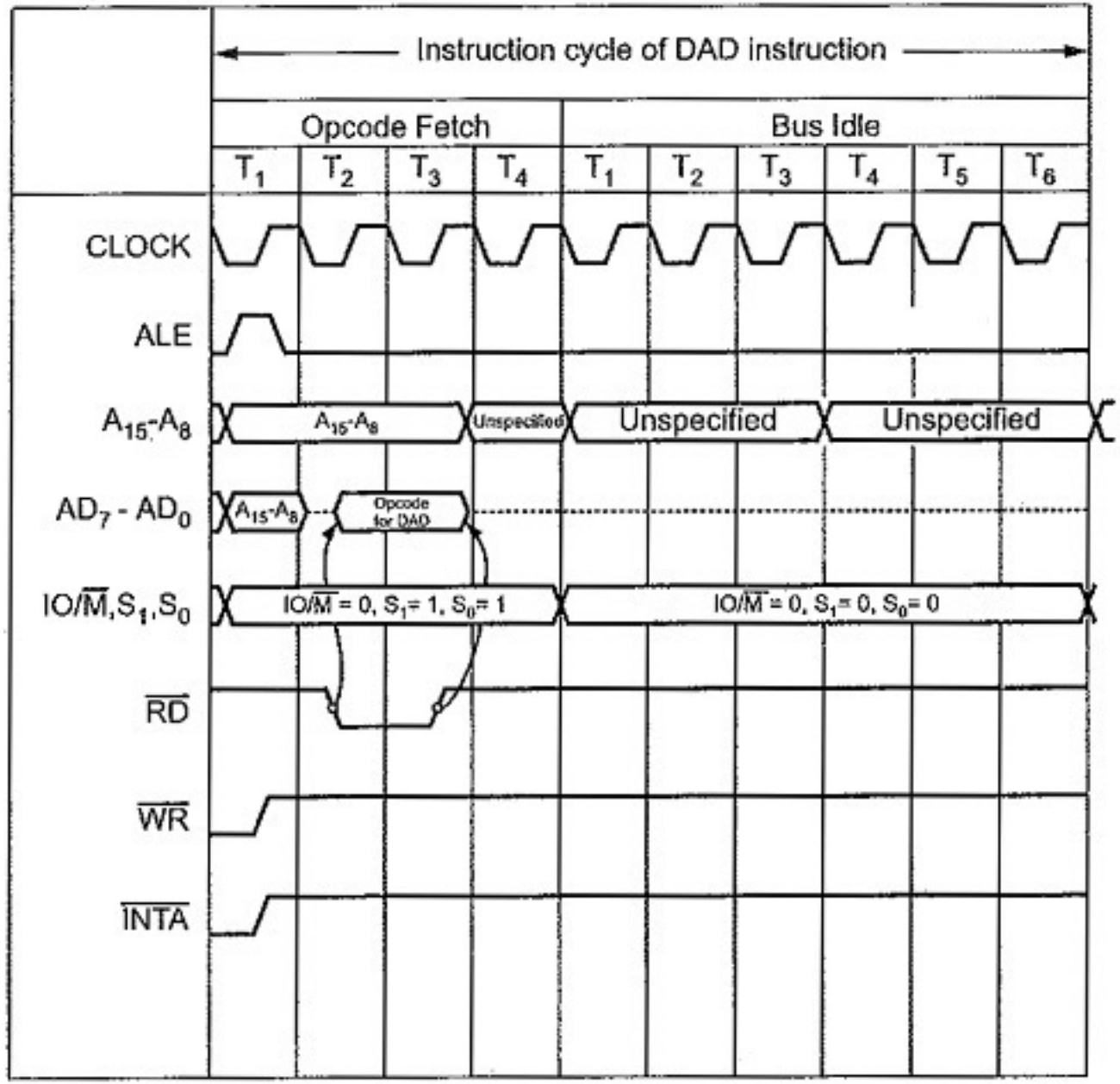


Fig. 1.22 Timing diagram for DAD instruction

29. XTHL (exchange Top of stack with HL)

Machine Cycle	Address Bus	Data Bus	T-state
OF	PC	OPCODE	4
MR	SP	[SP]	3
MR	SP+1	[SP+1]	3
MW	SP+1	[SP+1]	3
MW	SP	[SP]	3