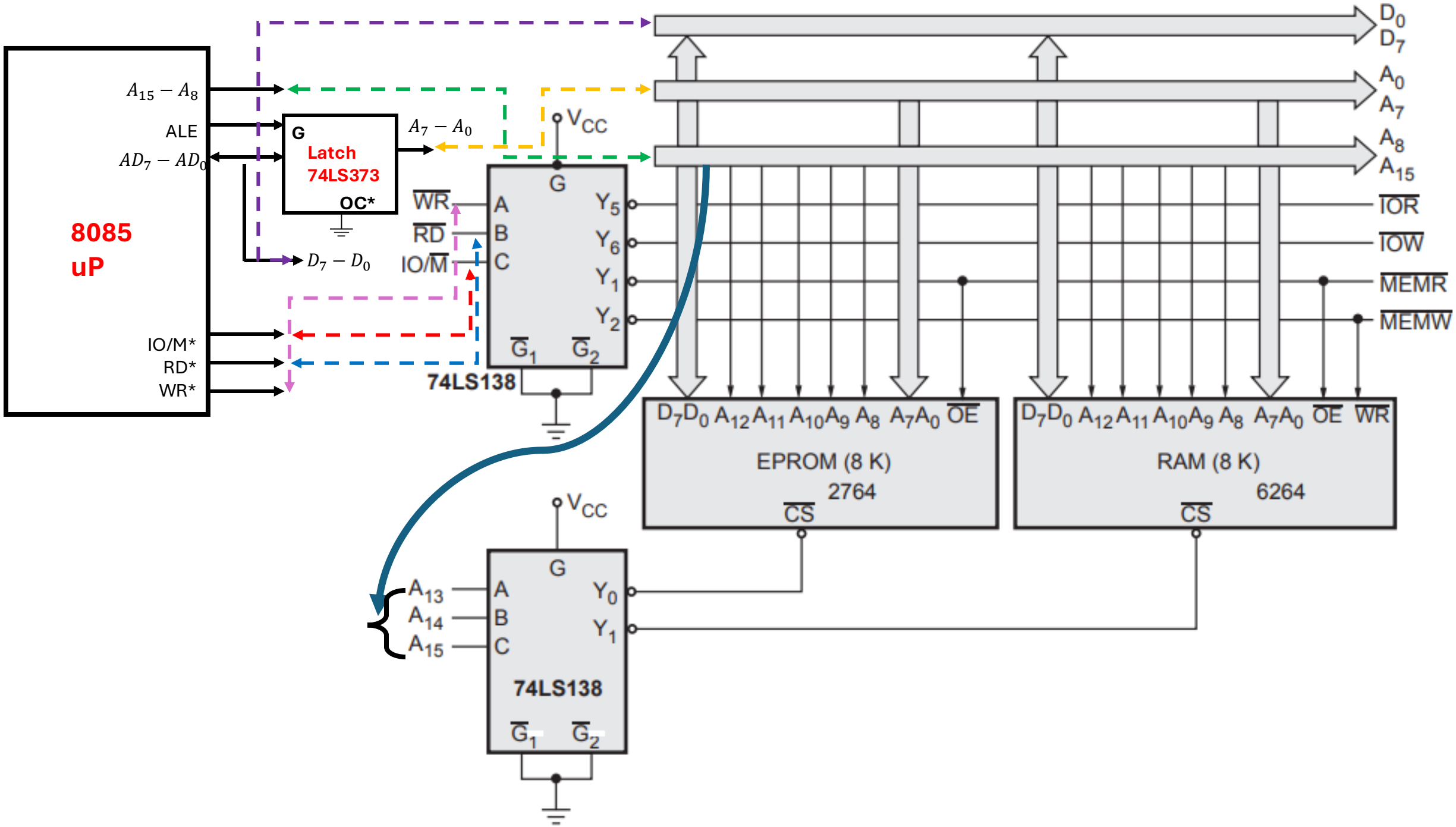
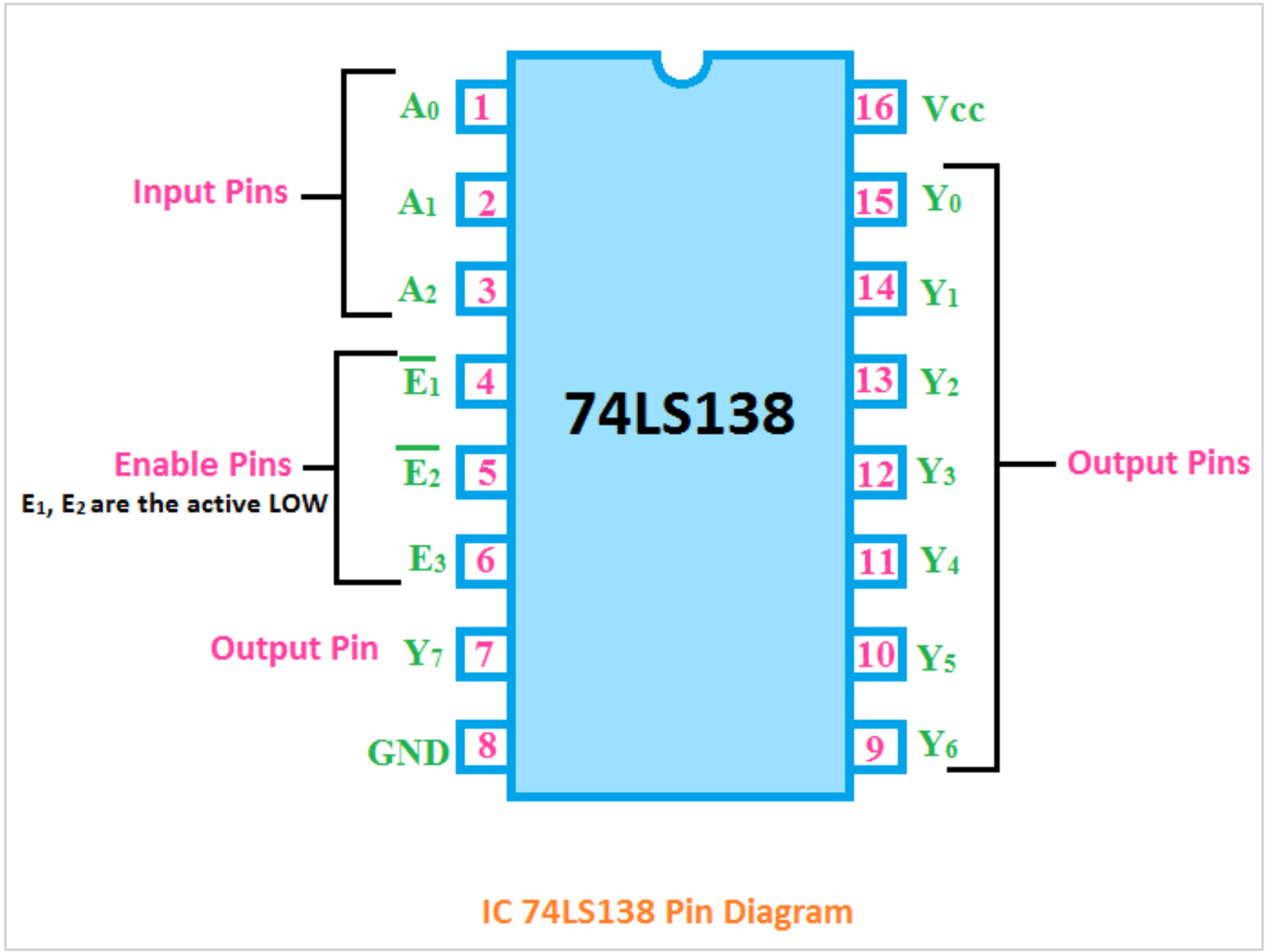
ADDITIONAL PRACTICE PROBLEMS ON MEMORY INTERFACING

COURSE INSTRUCTOR: DR. DEVYANI GUPTA

Q: Design memory system for the 8085 microprocessor such that it should contain 8 kbyte of EPROM (Erasable Programmable Read Only Memory) and 8 kbyte of RAM (Read/Write Memory).

Memory ICs	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Address
Starting address of EPROM	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000H
End address of EPROM	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1FFFH
Starting address of RAM	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	2000H
End address of RAM	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	3FFFH


8085
uP
$A_{15} - A_8$
ALE
$AD_7 - AD_0$
IO/M*
RD*
WR*
G
Latch
74LS373
OC*
$A_7 - A_0$
$D_7 - D_0$
V_{CC}
G
A
B
C
Y_5
Y_6
Y_1
Y_2
$\overline{G_1}$
$\overline{G_2}$
WR
RD
IO/M
74LS138
D_0
D_7
A_0
A_7
A_8
A_{15}
IOR
IOW
MEMR
MEMW
D_7D_0 $A_{12}A_{11}A_{10}A_9$ A_8 A_7A_0 OE
EPROM (8 K)
2764
CS
D_7D_0 $A_{12}A_{11}A_{10}A_9$ A_8 A_7A_0 OE WR
RAM (8 K)
6264
CS
V_{CC}
G
A
B
C
A_{13}
A_{14}
A_{15}
Y_0
Y_1
74LS138
$\overline{G_1}$
$\overline{G_2}$



IC 74LS138 Pin Diagram

Q: Design a microprocessor system for the 8085 microprocessor such that it should contain 2 KB of EPROM and 2 KB of RAM with starting addresses 0000H and 6000H respectively.

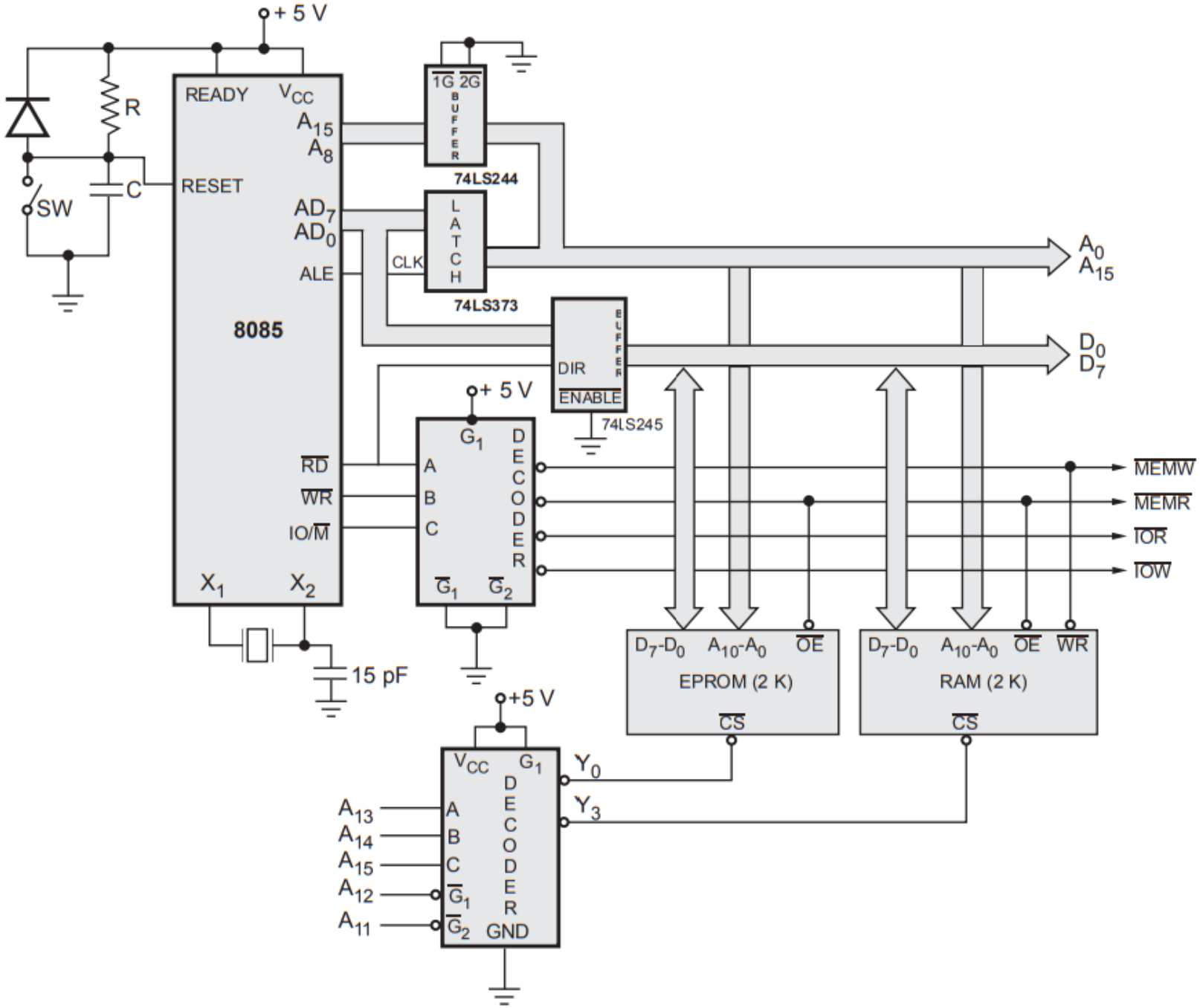
2K EPROM

Address Lines = 2K = $2^1 \times 2^{10} = 2^{11}$ = 11 lines
Data Lines = 8 Lines
Control Signals = RD*
Chip Select = remaining address lines

2K RAM

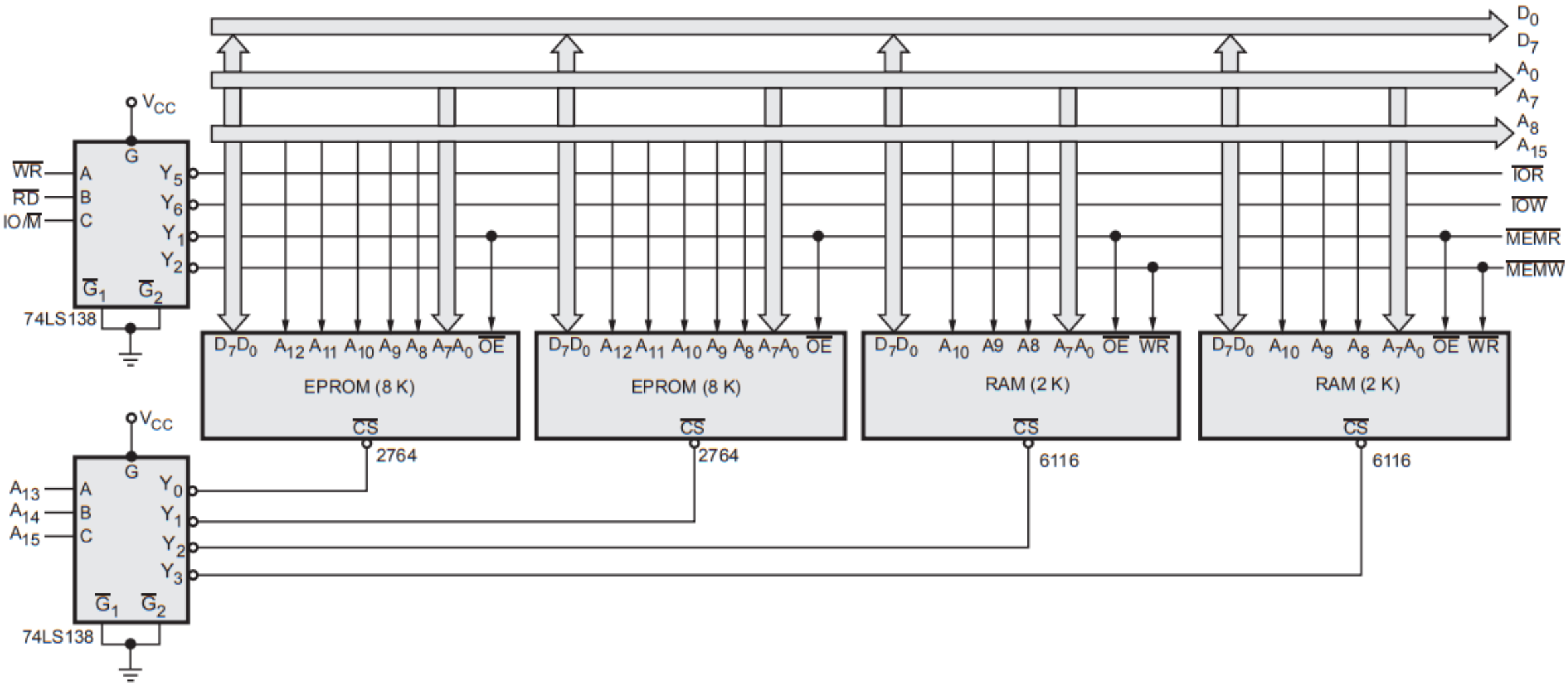
Address Lines = 2K = $2^1 \times 2^{10} = 2^{11}$ = 11 lines
Data Lines = 8 Lines
Control Signals = RD*, WR*
Chip Select = remaining address lines

Memory ICs	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Address
Starting address of EPROM	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000H
End address of EPROM	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	07FFH
Starting address of RAM	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	6000H
End address of RAM	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	67FFH

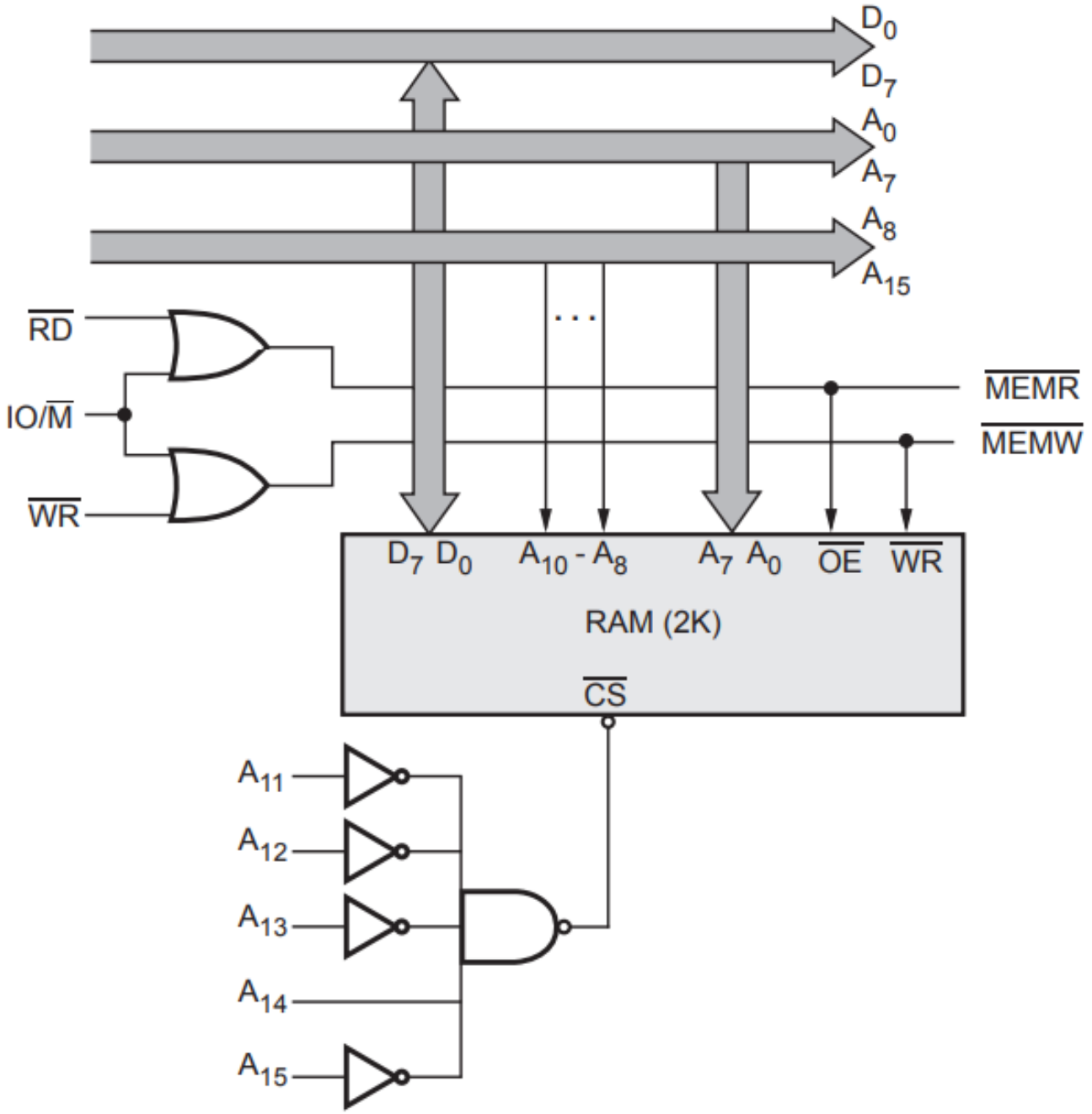

+ 5 V
R
SW
C
READY
RESET
V_{CC}
A_{15}
A_8
AD_7
AD_0
ALE
8085
X_1
X_2
15 pF
1G 2G
BUFFER
74LS244
LATCH
CLK
74LS373
DIR
ENABLE
BUFFER
74LS245
A_0
A_{15}
D_0
D_7
$\overline{RD}$
$\overline{WR}$
IO/$\overline{M}$
G_1
A
B
C
$\overline{G}_1$
$\overline{G}_2$
DECODER
$\overline{MEMW}$
$\overline{MEMR}$
$\overline{IOR}$
$\overline{IOW}$
D_7-D_0
A_{10}-A_0
$\overline{OE}$
$\overline{WR}$
EPROM (2 K)
RAM (2 K)
$\overline{CS}$
+5 V
V_{CC}
GND
Y_0
Y_3
A_{13}
A_{14}
A_{15}
A_{12}
A_{11}

Q: Design a microprocessor system for the 8085 microprocessor such that it should contain 16 kbyte of EPROM and 4 kbyte of RAM using two 8 kbyte EPROMs (2764) and two 2 kbyte RAMs (6116). Use a single 3:8 decoder for CS* for all ICs.

Memory ICs	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Address
Starting Address of EPROM 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000H
End Address of EPROM 1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1FFFH
Starting Address of EPROM 2	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	2000H
End Address of EPROM 2	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	3FFFH
Starting Address of RAM 1	0	1	0	X	X	0	0	0	0	0	0	0	0	0	0	0	4000H
End Address of RAM 1	0	1	0	X	X	1	1	1	1	1	1	1	1	1	1	1	47FFH
Starting Address of RAM 2	0	1	1	X	X	0	0	0	0	0	0	0	0	0	0	0	6000H
End Address of RAM 2	0	1	1	X	X	1	1	1	1	1	1	1	1	1	1	1	67FFH


D0
D7
A0
A7
A8
A15
IOR
IOW
MEMR
MEMW
VCC
G
WR
RD
IO/M
A
B
C
Y5
Y6
Y1
Y2
G1
G2
74LS138
D7D0 A12 A11 A10 A9 A8 A7A0 OE
EPROM (8 K)
CS
2764
D7D0 A12 A11 A10 A9 A8 A7A0 OE
EPROM (8 K)
CS
2764
D7D0 A10 A9 A8 A7A0 OE WR
RAM (2 K)
CS
6116
D7D0 A10 A9 A8 A7A0 OE WR
RAM (2 K)
CS
6116
VCC
G
A13
A14
A15
A
B
C
Y0
Y1
Y2
Y3
G1
G2
74LS138

Q: Without using any decoder, explain the interfacing of a RAM memory IC 6116 (2K × 8) with 8085.



Q: Connect one 2K x 8 EPROM and two 2K x 8 RAM with 8085 microprocessor. Generate MEMR* and MEMW* using OR gate. Additionally, generate CS* logic using 3:8 decoder.

HOMEWORK