LECTURE 10: COUNTERS & DELAY IN 8085

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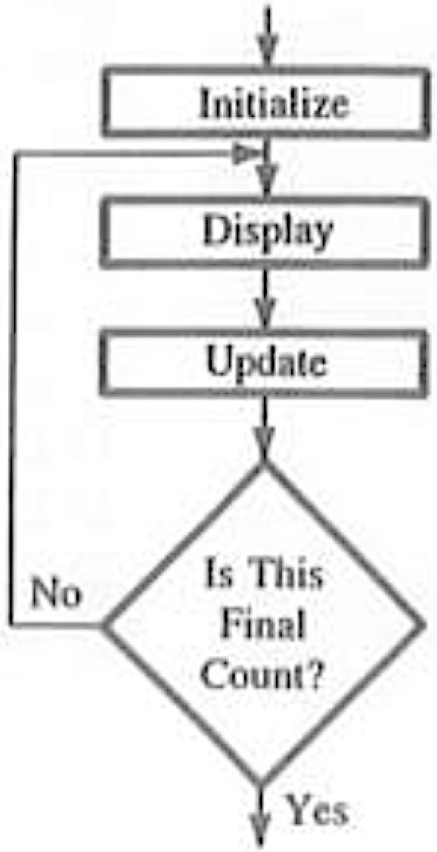
COUNTER

- A **counter** is a digital device or circuit used to count events, objects, or specific operations



TIME DELAY

A **time delay** refers to the intentional or unintentional pause between the initiation of an action and its result or output in a system

- Delay generation:
  1. Hardware delay – due to physical components
  2. Software delay – due to execution of instructions

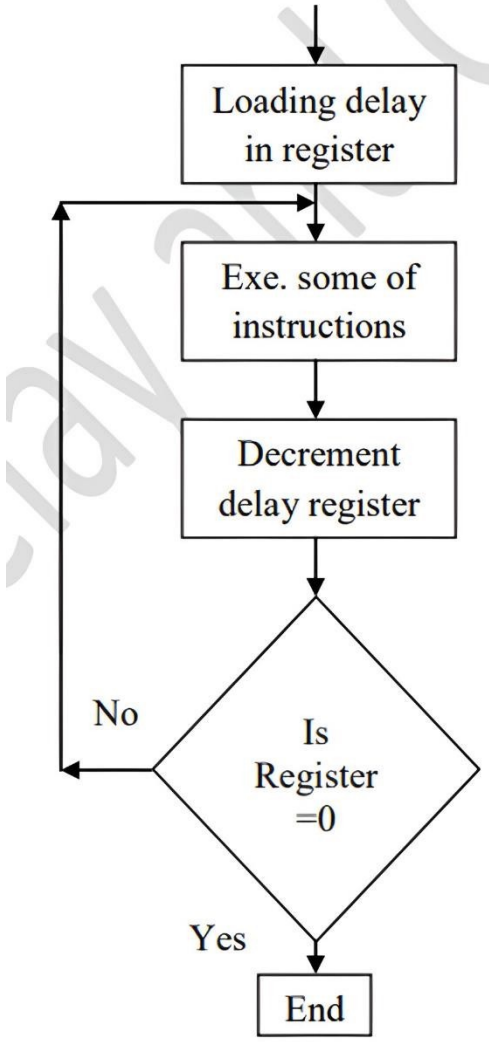


Figure (6-1): Example of time delay.

SOFTWARE DELAY

1. Using NOP instruction
2. Using Counter
   a) Using one 8-bit register
   b) Using one register pair
3. Using nested loop

1. USING 'NOP' INSTRUCTION

Eg: NOP;

1-byte instruction

Opcode fetch --- 4 T-states.

$T_D = 4T$.

$T = 1/(\text{Clk freq})$

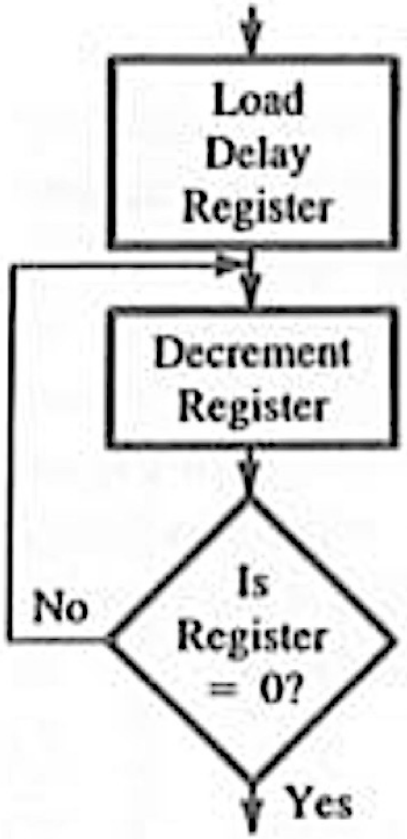
$\therefore$ assuming 8085 working at 3 MHz, $T = 1/(3\ \text{MHz}) = 0.333\ \mu$ sec.

$\therefore T_D = 4 \times 0.333 = 1.332\ \mu$ sec.

$\therefore$ **$T_D = 1.332\ \mu$ sec.**

This is the maximum delay that can be achieved by writing a NOP instruction.

2(a). USING 8-BIT REGISTER



Label	Opcode	Operand	Comments	T-states
	MVI	C,FFH	;Load register C	7
LOOP:	DCR	C	;Decrement C	4
	JNZ	LOOP	;Jump back to ; decrement C	10/7

Can you find the total delay?
Assume clock frequency = 2 MHz

2(b). USING REGISTER PAIR

Label	Opcode	Operand	Comments	T-states
	LXI	B,2384H	;Load BC with 16-bit count	10
LOOP:	DCX	B	;Decrement (BC) by one	6
	MOV	A,C	;Place contents of C in A	4
	ORA	B	;OR (B) with (C) to set Zero flag	4
	JNZ	LOOP	;If result ≠ 0, jump back to LOOP	10/7

Can you find the total delay?
Assume clock frequency = 2 MHz

3. Nested Loop

```
        MVI B,38H     7T
LOOP2:  MVI C,FFH     7T
LOOP1:  DCR C         4T
        JNZ LOOP1     10/7T
        DCR B         4T
        JNZ LOOP2     10/7T
```

Can you find the total delay?
Assume clock frequency = 2 MHz

Problems

- Calculate the time delay to programs shown below (program 6.4, 6.5 and 6.6), (let the microprocessor frequency is 1MHz).

Program 6.4

```
        MVI C,37
LOOP1   MVI A, 33
        RAR
        DCR C
        JNZ LOOP1
        HLT
```

Problems

- Calculate the time delay to programs shown below (program 6.4, 6.5 and 6.6), (let the microprocessor frequency is 1MHz).

Program 6.5

```
        LXI B,234B
LOOP1   MVI A, 33
        RAR
        DCX B
        MOV A,C
        ORA B
        JNZ LOOP1
        HLT
```

Program 6.6

```
        MVI B,37
LOOP 2  MVI D,FF
LOOP1   MVI A, 33
        RAR
        DCR D
        JNZ LOOP1
        DCR B
        JNZ LOOP2
        HLT
```

Solutions

Program 6.4

$T_t = T_o + T_i$

$T_o = [7T_{state}$ **(MVI C,37)** $+ 7T_{state}$ **(JNZ loop1)** $+ 6T_{state}$ **(HLT)]***t

$= 20\ T_{state} * 1\ \mu S = 20\ \mu S$

$T_i = [7T_{state}$ **(MVI A,33)** $+ 4T_{state}$ **(RAR)** $+ 4T_{state}$ **(DCR C)** $+ 10T_{state}$ **(JNZ loop1)]*t*55**

$= [25T_{state}] * t * 55$

$= [25\ \mu S] * 55 = 1375\ \mu S$

$T_t = 20\ \mu S + 1375\ \mu S = 1395\ \mu S = 1.395\ mS$

Verify these answers!

Program 6.5

$T_o = [10T_{state}$ **(LXI B,234B)** $+ 7T_{state}$ **(JNZ loop)** $+ 6T_{state}$ **(HLT)]** $= 23\ \mu S$

$T_i = [7T_{state}$ **(MVI A,33)** $+ 4T_{state}$ **(RAR)** $+ 4T_{state}$ **(DCX B)** $+ 4T_{state}$ **(MOV A,C)** $+ 4T_{state}$ **(ORA B)** $+$

$10T_{state}$ **(JNZ loop1)]*9035** $= (33\ T_{state}) * 9035 = (33\ \mu S) * 9035 = 298155\ \mu S$

$T_t = 23\ \mu S + 298155\ \mu S = 298178\ \mu S = 298.178 ms$

Solve it

Write ALP to make the microprocessor working as up/down counter mod (32) with time delay 2ms between each two counting states. Assume, the operating frequency is 2 MHz.