LECTURE:15-17 MEMORY INTERFACING IN 8085

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Recall…

- uP does not have any memory, it needs to be interfaced
- External memory support in 8085:
  - Address bus size = 16 bits
  - Max. number of address = 2^{16} = 64kb
  - Every location can store 1 byte
  - Max. memory that can be interfaced with 8085 = 64KB
- We can interface a memory chip with max size 64KB or several memory chips with combined size not exceeding 64KB

MEMORY

1. Primary Memory:

Also called **main memory**, it is directly accessible by the CPU. It includes:

- **RAM (Random Access Memory):**
  - **Volatile memory**, meaning data is lost when the power is turned off.
  - Used to store data that the CPU needs to access quickly for ongoing tasks.
  - Types:
    - **SRAM (Static RAM)**: Faster and more expensive; used for cache memory.
    - **DRAM (Dynamic RAM)**: Slower and less expensive; used for system memory.
- **ROM (Read-Only Memory):**
  - **Non-volatile** memory that holds data permanently, even when the power is off.
  - Contains critical boot-up programs (firmware) for the system.
  - Types:
    - **PROM (Programmable ROM)**: Can be programmed once.
    - **EPROM (Erasable Programmable ROM)**: Can be erased using UV light and reprogrammed.
    - **EEPROM (Electrically Erasable Programmable ROM)**: Can be erased and reprogrammed electronically, making it more flexible.

2. Secondary Memory:

Also known as **auxiliary memory** or **storage**, it is used to store data and programs long-term. It is slower than primary memory but can store much larger amounts of data.

MEMORY ICs

SIZE	EPROM	RAM
1KB	2708	6108
2KB	2716	6116
4KB	2732	6132
8KB	2764	6164
16KB	27128	61128
32KB	27256	61256

FUNCTIONAL PIN DIAGRAM OF MEMORY CHIPS

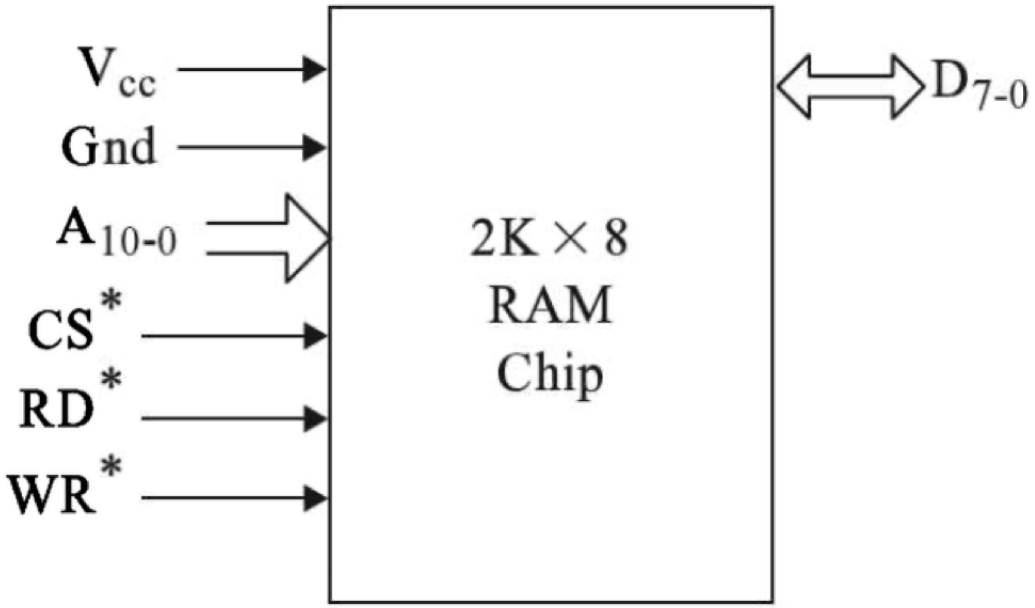


Fig. 11.1
Functional pin diagram of
2K × 8 RAM chip

What is the starting address of this chip?

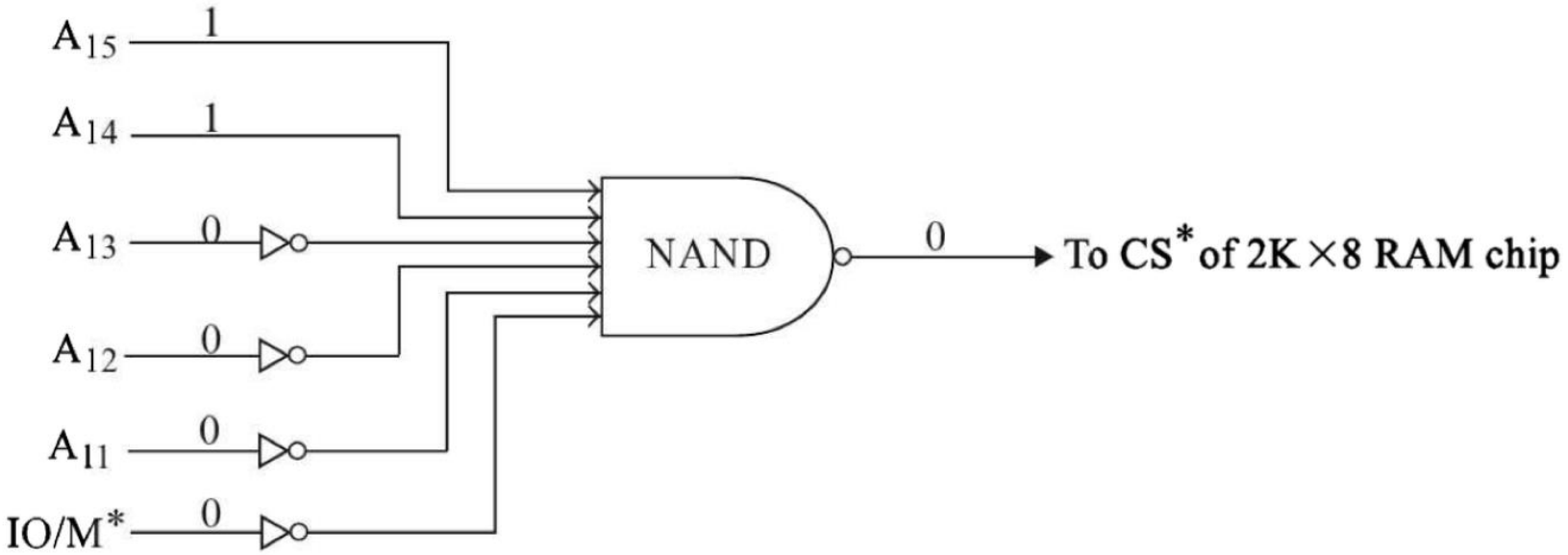


Fig. 11.2
Chip selection circuit to provide 2K × 8 RAM with starting address as C000H

Note that there is nothing like a unique chip select circuit. The chip select circuit shown in Fig. 11.3 also serves to give the same address range, C000H–C7FFH.

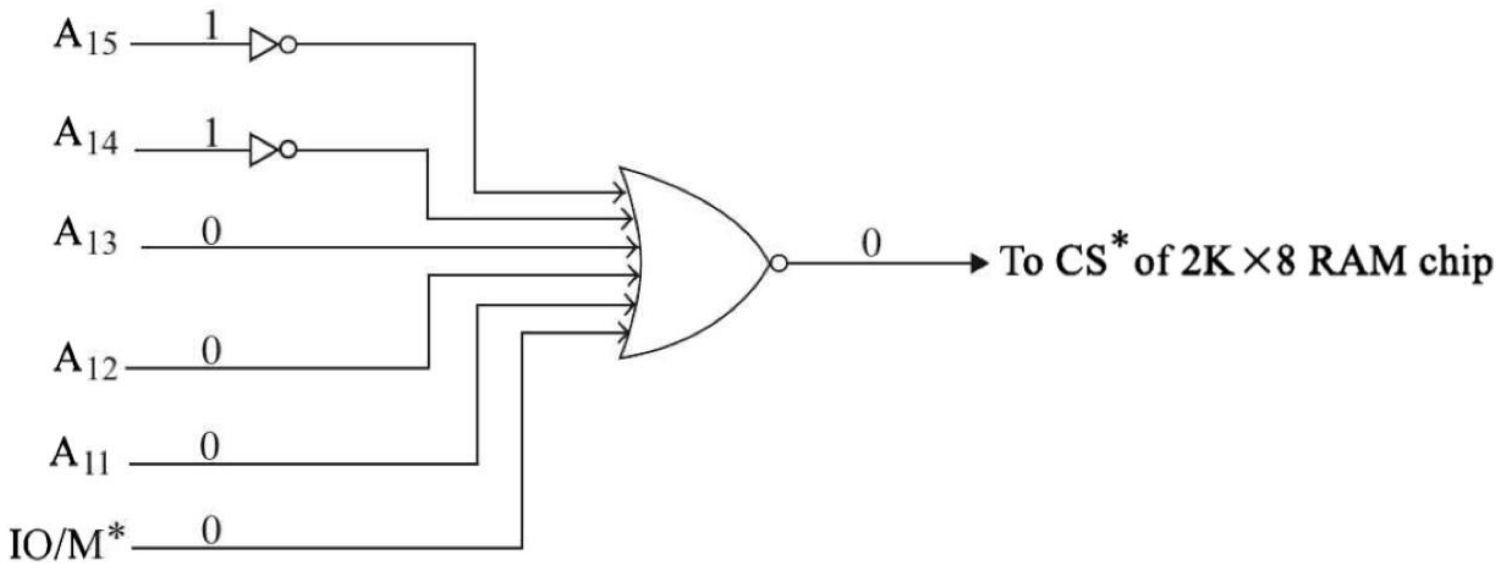


Fig. 11.3
Another equivalent chip select circuit

MULTIPLE MEMORY ADDRESS RANGE

Suppose we have the chip select circuit as shown in Fig. 11.4, then what is the address range for the RAM?

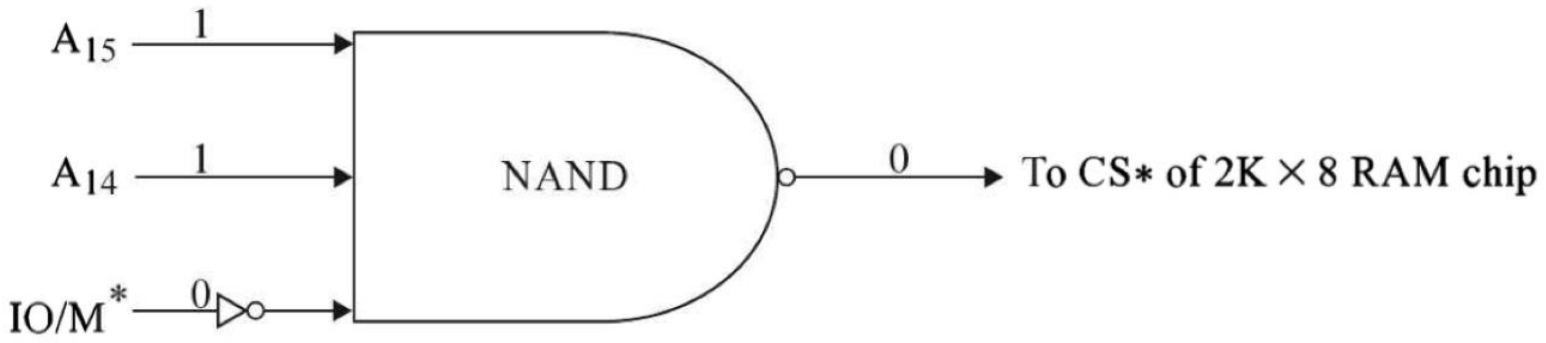


Fig. 11.4
Chip selection that results in multiple address range

There are eight possible values for $A_{13\text{-}11}$, and as such we will have eight different address ranges possible for the RAM. The address range for the RAM for different values of $A_{13\text{-}11}$ will be as shown in the following table.

$A_{13\text{-}11}$	*Range for RAM*
0 0 0	C000H–C7FFH
0 0 1	C800H–CFFFH
0 1 0	D000H–D7FFH
0 1 1	D800H–DFFFH
1 0 0	E000H–E7FFH
1 0 1	E800H–EFFFH
1 1 0	F000H–F7FFH
1 1 1	F800H–FFFFH

ADDRESS DECODING TECHNIQUES

- PARTIALLY DECODED ADDRESSING
  - some address lines are in ‘don’t care’ state for CHIP SELECT
- FULLY DECODED ADDRESSING
  - All address lines are used for CHIP SELECT

Q: If the starting address is 0351 H. Find the ending address of 1KB memory when interfaced with 8085 uP.

Total number of address Lines for $2^{10} memory = 10$

If the starting address = 0000 H
Then, the ending address = 03FF H

If starting address = 0351 H
Then, ending address = 0351 H + 03FF H = 0750 H

Q: If the ending address is BABF H. Find the starting address of 4KB memory when interfaced with 8085 uP.

Total number of address Lines for $2^2 \times 2^{10} memory = 12$

If the starting address = 0000 H
Then, the ending address = 0FFF H

If ending address = BABF H
Then, ending address = BABF H – 0FFF H = AAC0 H

Q: Draw an interfacing of a 4K EPROM having starting address 2000H with 8085 uP. Use demultiplexed address/data lines and 3-to-8 decoder (74LS138)

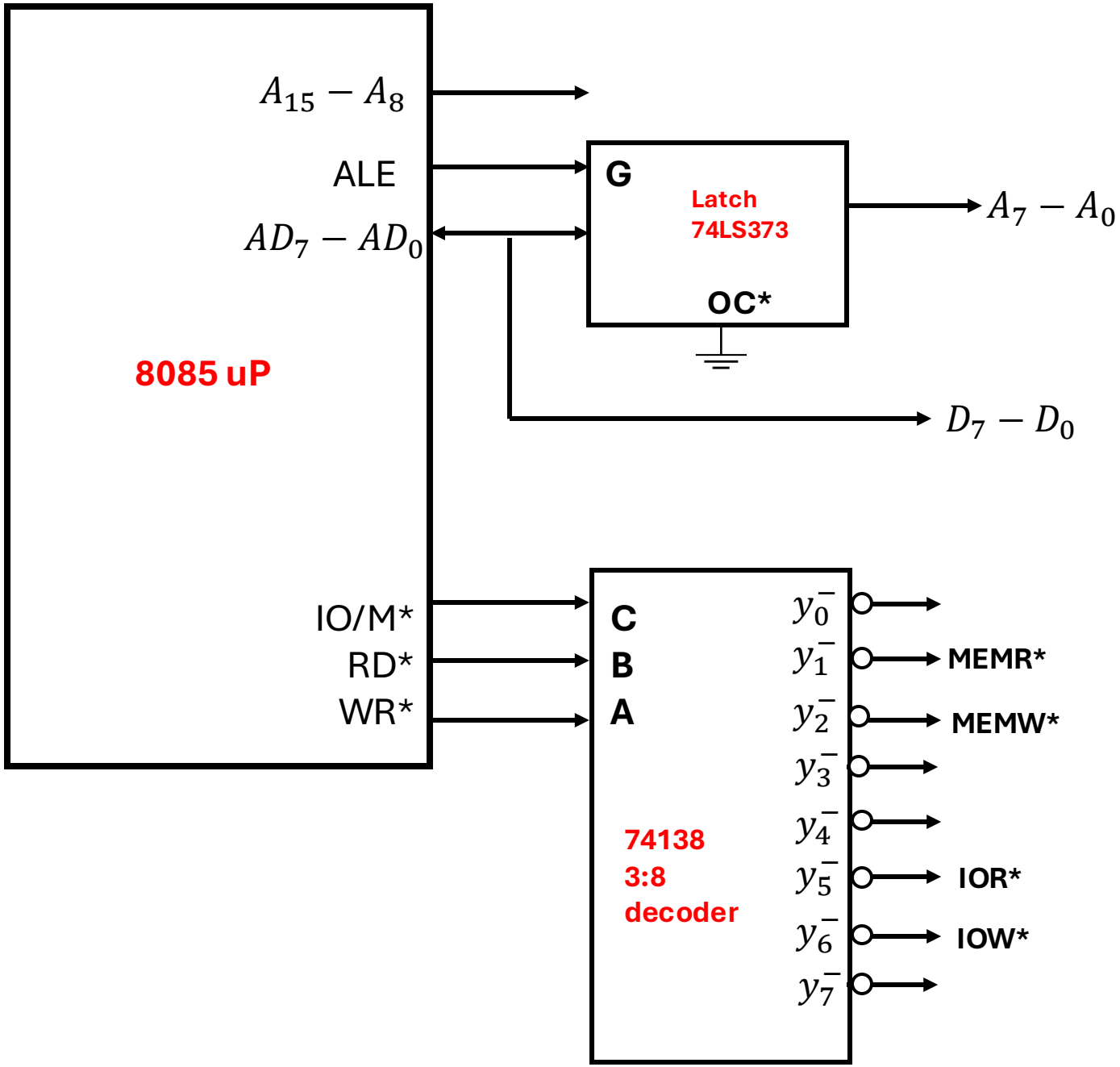
For memory interfacing, 4 types of signals are required:

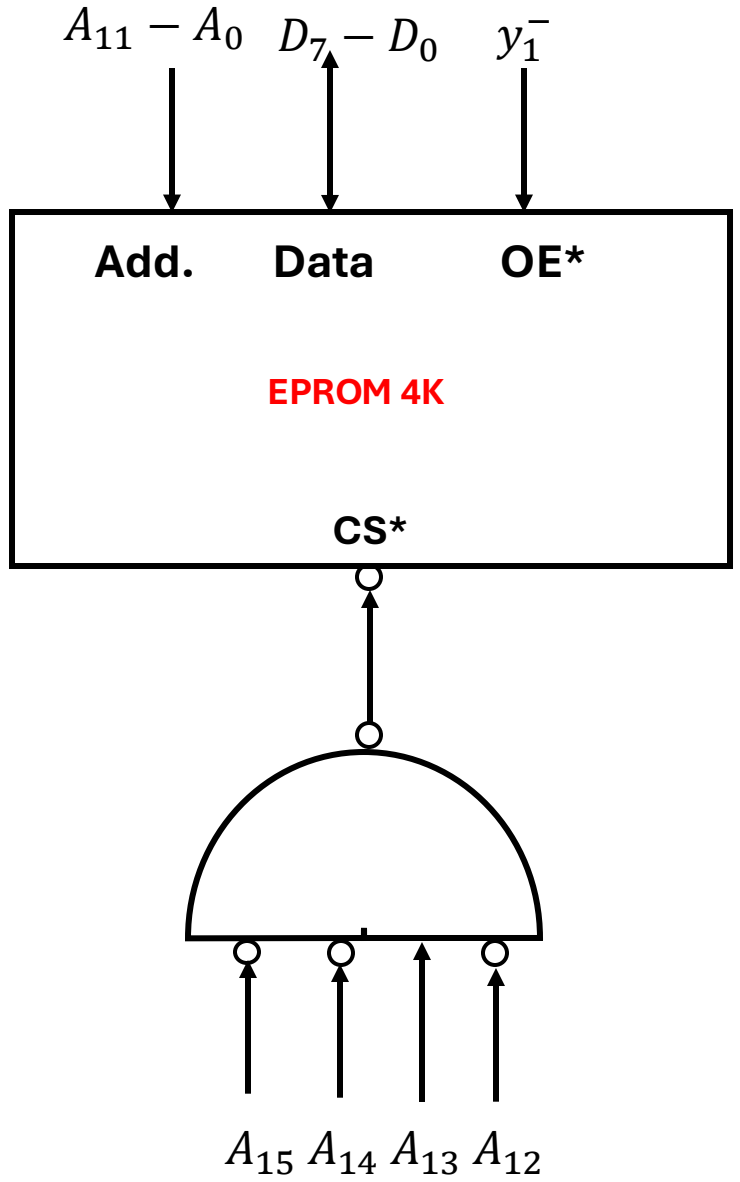
1. Address Lines
2. Data Lines
3. Control Lines
4. Chip Select

Address Lines = 4K = $2^2 \times 2^{10} = 2^{12}$ = 12 lines
Data Lines = 8 Lines
Control Signals = RD*
Chip Select = remaining address lines

Memory Mapping

Memory Chip	$A_{15}\ A_{14}\ A_{13}\ A_{12}$	$A_{11}\ A_{10}\ A_9\ A_8$	$A_7\ A_6\ A_5\ A_4$	$A_3\ A_2\ A_1\ A_0$	Memory Address
4K EPROM	0 0 1 0	0 0 0 0	0 0 0 0	0 0 0 0	2000 H
	0 0 1 0	1 1 1 1	1 1 1 1	1 1 1 1	2FFF H


$A_{15} - A_8$
ALE
$AD_7 - AD_0$
8085 uP
G
Latch
74LS373
OC*
$A_7 - A_0$
$D_7 - D_0$
IO/M*
RD*
WR*
C
B
A
74138
3:8
decoder
y_0^-
y_1^-
y_2^-
y_3^-
y_4^-
y_5^-
y_6^-
y_7^-
MEMR*
MEMW*
IOR*
IOW*


$A_{11} - A_0$
$D_7 - D_0$
y_1^-
Add.
Data
OE*
EPROM 4K
CS*
A_{15} A_{14} A_{13} A_{12}

Q: Interfacing 4K EPROM and 16K RAM with 8085 uP. Write the address range for both the memory chips and also the address decoding logic.

For memory interfacing, 4 types of signals are required:

1. Address Lines
2. Data Lines
3. Control Lines
4. Chip Select

4K EPROM

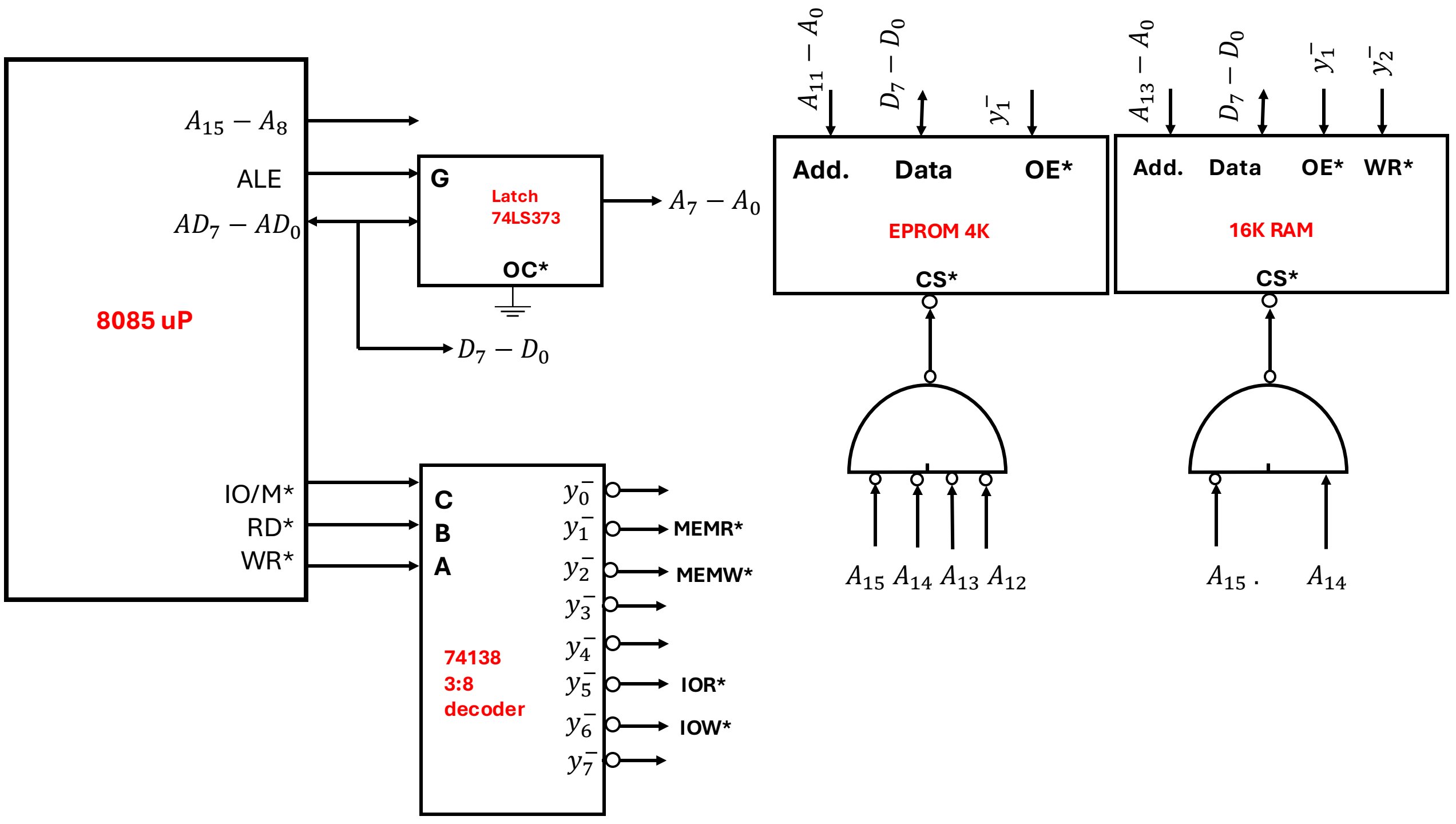
Address Lines = 4K = $2^2 \times 2^{10} = 2^{12}$ = 12 lines
Data Lines = 8 Lines
Control Signals = RD*
Chip Select = remaining address lines

16K RAM

Address Lines = 16K = $2^4 \times 2^{10} = 2^{14}$ = 14 lines
Data Lines = 8 Lines
Control Signals = RD*, WR*
Chip Select = remaining address lines

Memory Mapping

Memory Chip	$A_{15}\ A_{14}\ A_{13}\ A_{12}$	$A_{11}\ A_{10}\ A_9\ A_8$	$A_7\ A_6\ A_5\ A_4$	$A_3\ A_2\ A_1\ A_0$	Memory Address
4K EPROM	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0000 H
	0 0 0 0	1 1 1 1	1 1 1 1	1 1 1 1	0FFF H
16K RAM	0 1 0 0	0 0 0 0	0 0 0 0	0 0 0 0	4000 H
	0 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	7FFF H


$A_{15} - A_8$
ALE
$AD_7 - AD_0$
8085 uP
IO/M*
RD*
WR*
G
Latch
74LS373
OC*
$A_7 - A_0$
$D_7 - D_0$
C
B
A
74138
3:8
decoder
y_0^-
y_1^-
y_2^-
y_3^-
y_4^-
y_5^-
y_6^-
y_7^-
MEMR*
MEMW*
IOR*
IOW*
$A_{11} - A_0$
$D_7 - D_0$
y_1^-
Add.
Data
OE*
EPROM 4K
CS*
A_{15} A_{14} A_{13} A_{12}
$A_{13} - A_0$
$D_7 - D_0$
y_1^-
y_2^-
Add.
Data
OE*
WR*
16K RAM
CS*
A_{15} .
A_{14}

Q: Interface 8K EPROM and 16K RAM with 8085 uP using chips of 4K EPROM and 8K RAM. Show decoding of IC with 74LS138 Decoder.

4K EPROM

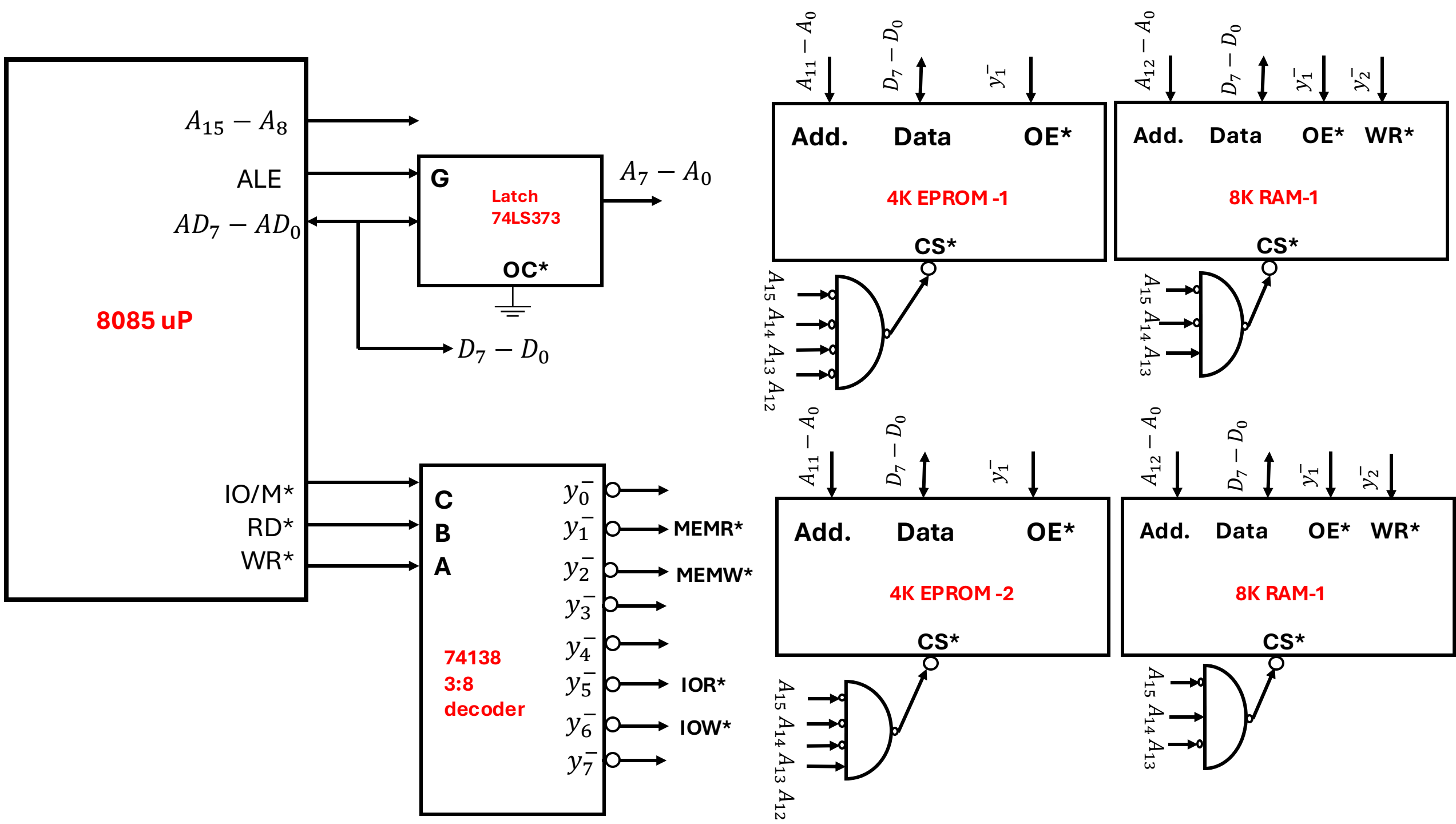
Address Lines = 4K = $2^2 \times 2^{10} = 2^{12}$ = 12 lines
Data Lines = 8 Lines
Control Signals = RD*
Chip Select = remaining address lines

8K RAM

Address Lines = 8K = $2^3 \times 2^{10} = 2^{13}$ = 13 lines
Data Lines = 8 Lines
Control Signals = RD*, WR*
Chip Select = remaining address lines

Memory Mapping

Memory Chip	$A_{15}\ A_{14}\ A_{13}\ A_{12}$	$A_{11}\ A_{10}\ A_9\ A_8$	$A_7\ A_6\ A_5\ A_4$	$A_3\ A_2\ A_1\ A_0$	Memory Address
4K EPROM-1	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0000 H
	0 0 0 0	1 1 1 1	1 1 1 1	1 1 1 1	0FFF H
4K EPROM-2	0 0 0 1	0 0 0 0	0 0 0 0	0 0 0 0	1000 H
	0 0 0 1	1 1 1 1	1 1 1 1	1 1 1 1	1FFF H
8K RAM-1	0 0 1 0	0 0 0 0	0 0 0 0	0 0 0 0	2000 H
	0 0 1 1	1 1 1 1	1 1 1 1	1 1 1 1	3FFF H
8K RAM-2	0 1 0 0	0 0 0 0	0 0 0 0	0 0 0 0	4000 H
	0 1 0 1	1 1 1 1	1 1 1 1	1 1 1 1	5FFF H

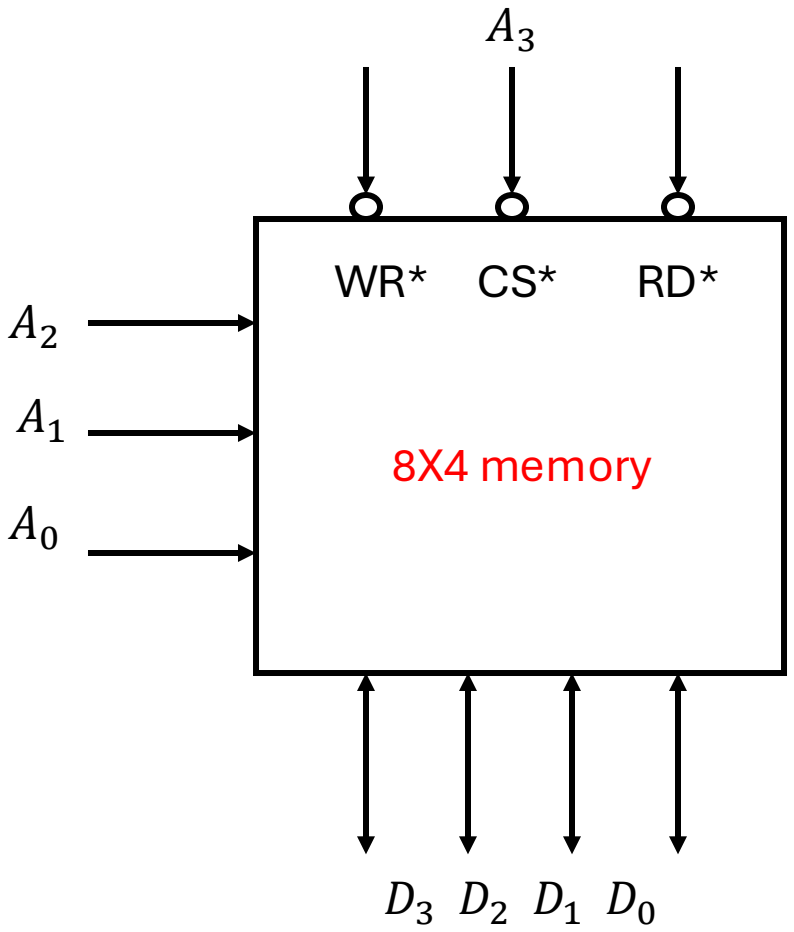

$A_{15} - A_8$
ALE
$AD_7 - AD_0$
8085 uP
IO/M*
RD*
WR*
G
Latch
74LS373
OC*
$A_7 - A_0$
$D_7 - D_0$
C
B
A
74138
3:8
decoder
y_0^-
y_1^-
y_2^-
y_3^-
y_4^-
y_5^-
y_6^-
y_7^-
MEMR*
MEMW*
IOR*
IOW*
$A_{11} - A_0$
$D_7 - D_0$
y_1^-
Add.
Data
OE*
4K EPROM -1
CS*
A_{15} A_{14} A_{13} A_{12}
$A_{12} - A_0$
y_2^-
WR*
8K RAM-1
4K EPROM -2
8K RAM-1

MEMORY ICs (with 8-bit Data)

SIZE	EPROM	RAM
1KB	2708	6108
2KB	2716	6116
4KB	2732	6132
8KB	2764	6164
16KB	27128	61128
32KB	27256	61256

Q: Interface 8X4 bits memory with 8085 uP.

Data size = 4 bits
Number of address =8
Number of address lines required = 3 (from 2^3)



OBSERVATIONS

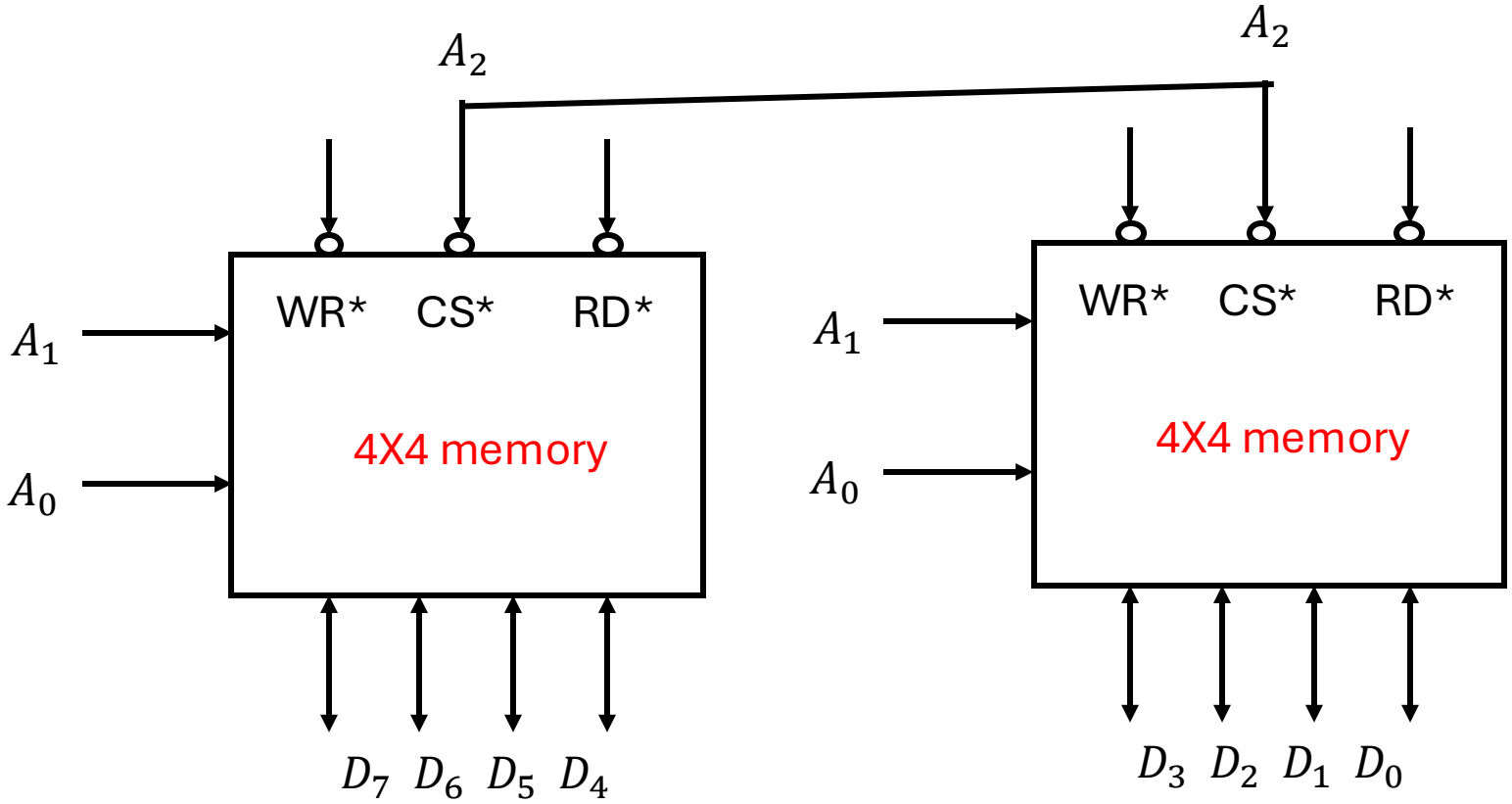
- This is an example of partially decoded addressing
- Only 4 data lines has been connected

Q: Interface two 4X4 bits memory with 8085 uP such that the two memories form the lower and upper nibble of data of 8085.

Data size = 4 bits
Number of address per memory =4
Number of address lines required = 3 (from 2^2)

OBSERVATIONS

- This is an example of partially decoded addressing



PRACTICE QUESTIONS

Q1: Interface 12KB RAM with 8085 uP using IC 6232. Use IO/M* in CS* logic generation

Q2: Interface 1KB RAM with 8085 uP using 1K X 4 RAM (IC 2114/2142).

Q3: Interface 4KB RAM with 8085 uP using 1K X 4 ICs. Allot addresses starting from 4000H, 4800H, C400H and CC00H. Use IO/M* in CS* generation

Q4: Interface 2KB EPROM and 2KB RAM with 8085 uP such that there is 2K gap in between addresses.