

Assignment 1 Report

CIS-350

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Github Link:

All circuit files mentioned in this report are stored in the following github location:

<https://github.com/ajakhtar/CIS-310/tree/e3727c07ca29fdc6af963940a678bf837b2db97c/Assignment%201>.

General Purpose Register

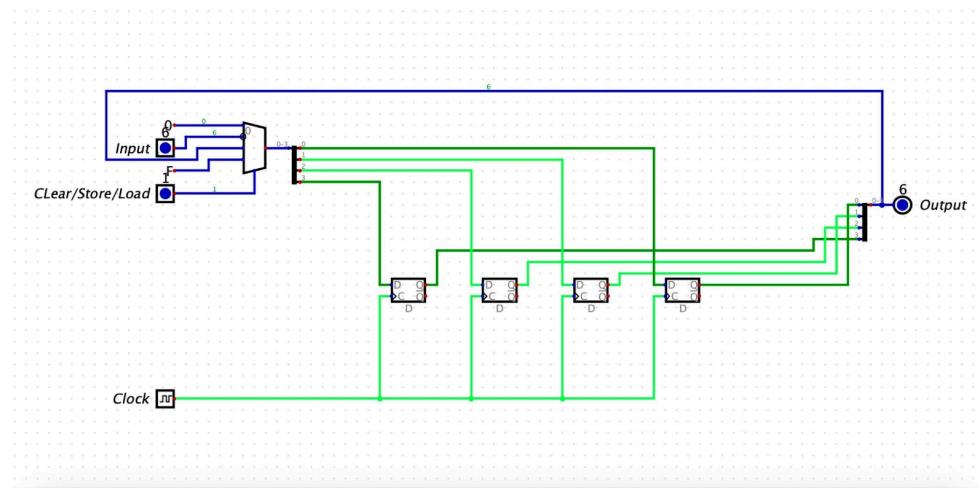
The general purpose register is a small memory unit that stores 4 bits of data. It uses 3 inputs: an Input which designates the data which can be processed; a clock to maintain synchronization; and a control signal which specifies which function that the register will perform. When the control signal is set to 0 it will clear the register to zero, when set to 1 it stores the input value into the register, when set to 2 it loads the data currently stored in the register, and when set to 3 it will set the data in the register to max size(15 for a 4 bit register).

Testing:

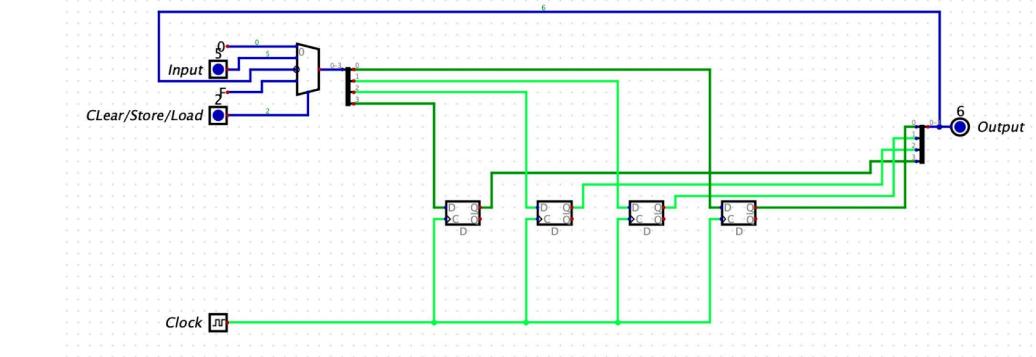
Testing this circuit will consist of showing a 4 bit input value which will have the Write, Read, Clear, and then the Set Max operations performed on it. To demonstrate the accuracy of the load operation, the input will be changed before changing the control signal to assure that the correct value is being output.

Test Case 1: 6

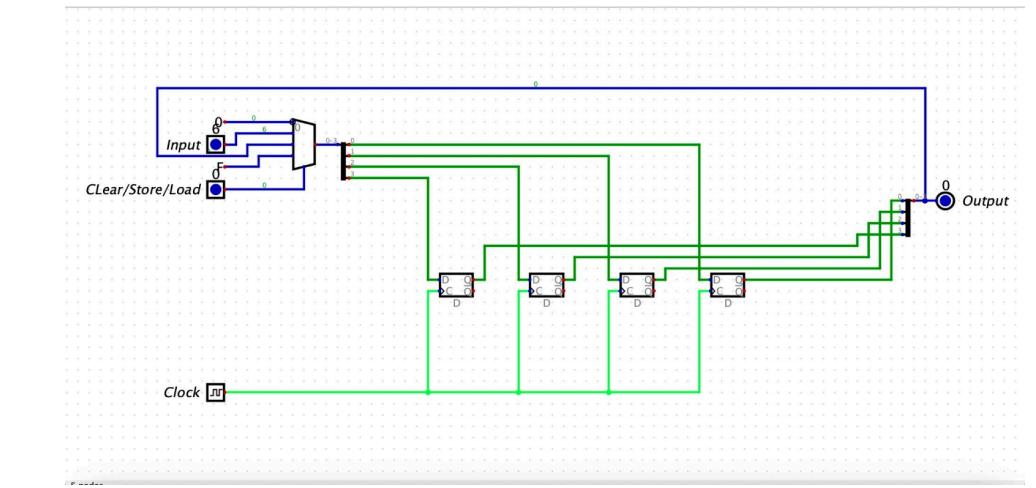
- Write:



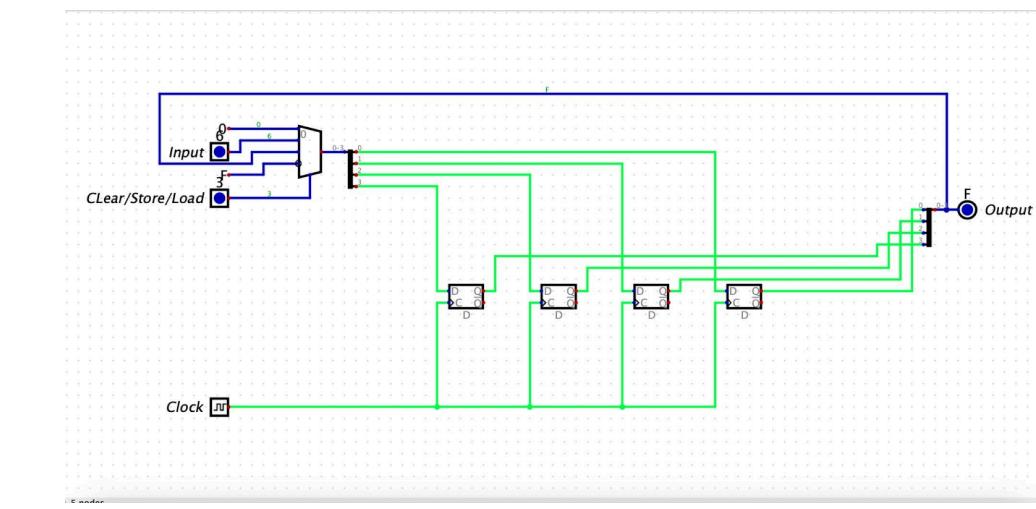
- ### - Read:



- **Clear:**

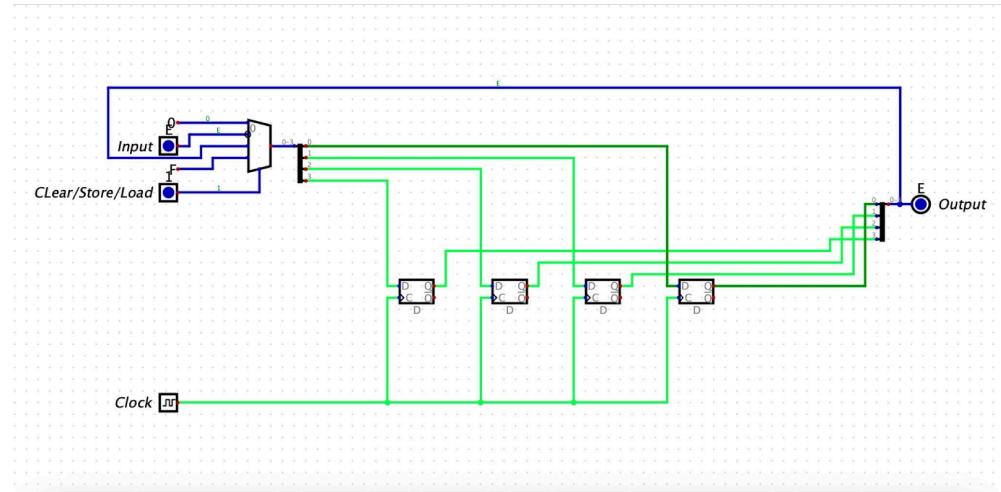


- Set to Max:

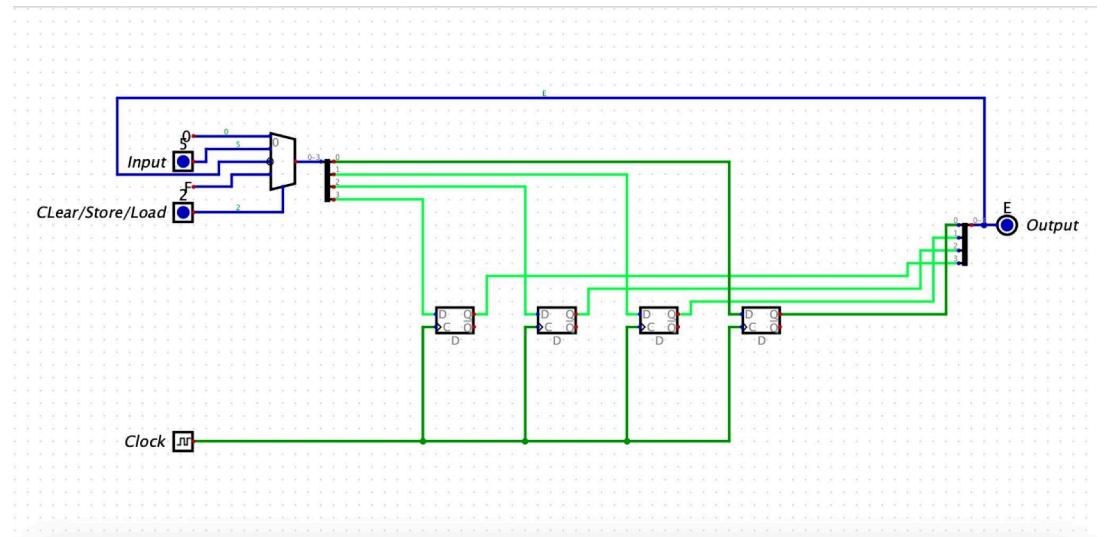


Test Case 2: 14

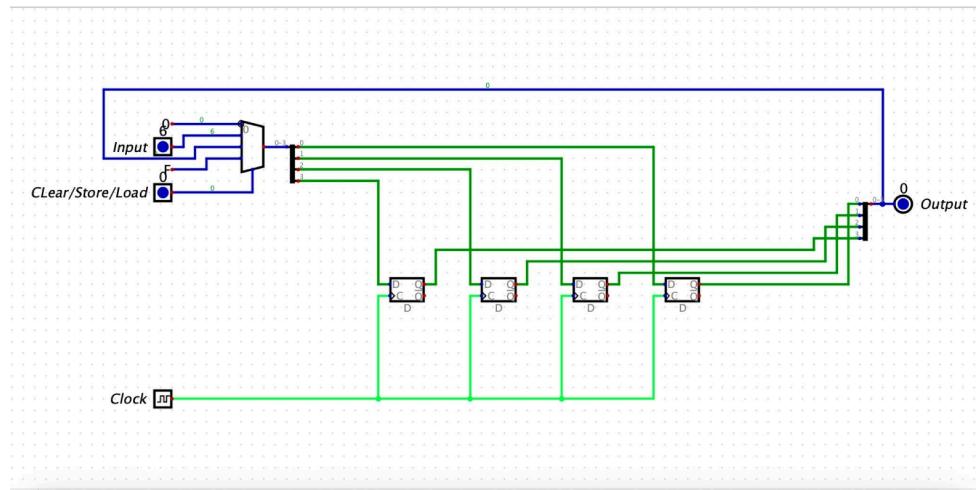
- Write:



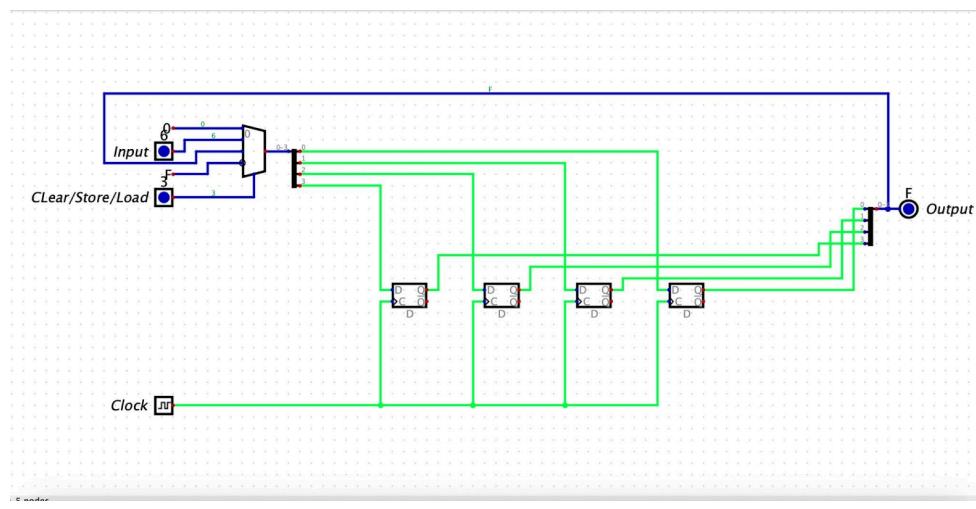
- Read:



- Clear:



- Set to Max:



Program Counter:

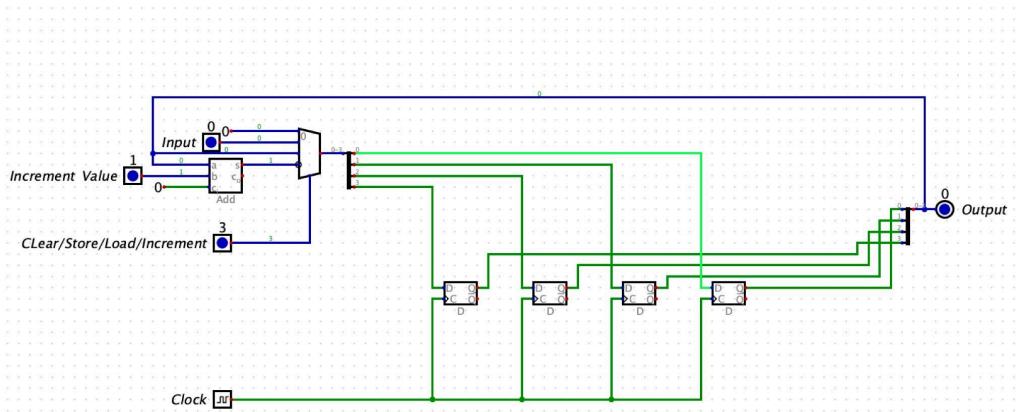
The program counter keeps track of the next instruction to be executed. It is built on the base of the General Purpose Register, however the Set to Max control signal has been replaced with a signal that increments the value currently being stored in the register by a 4 bit value.

Testing:

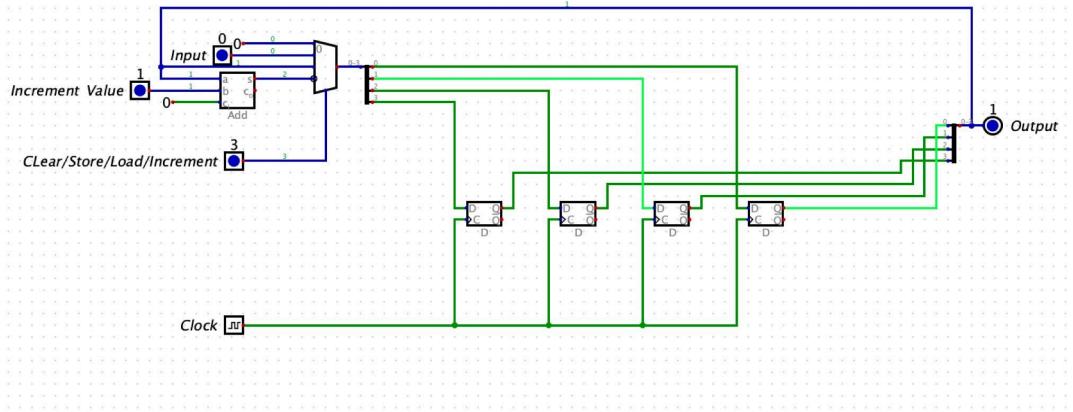
Testing for this circuit will consist of beginning the circuit with the value 0 stored, and then incrementing the circuit by a chosen value. Three clock cycles will be shown for each test case beginning with the default value..

Test Case 1: 1

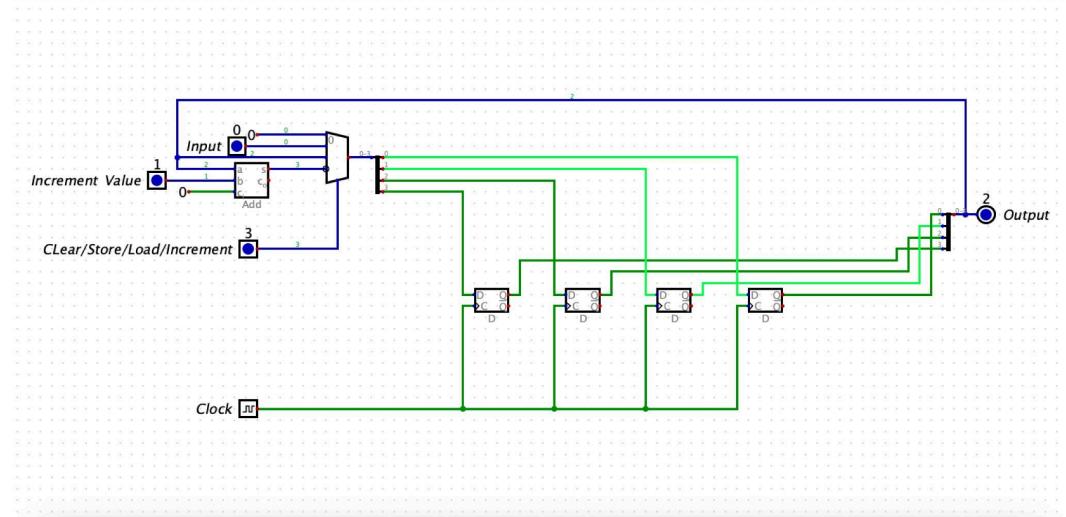
- Clock Cycle 0:



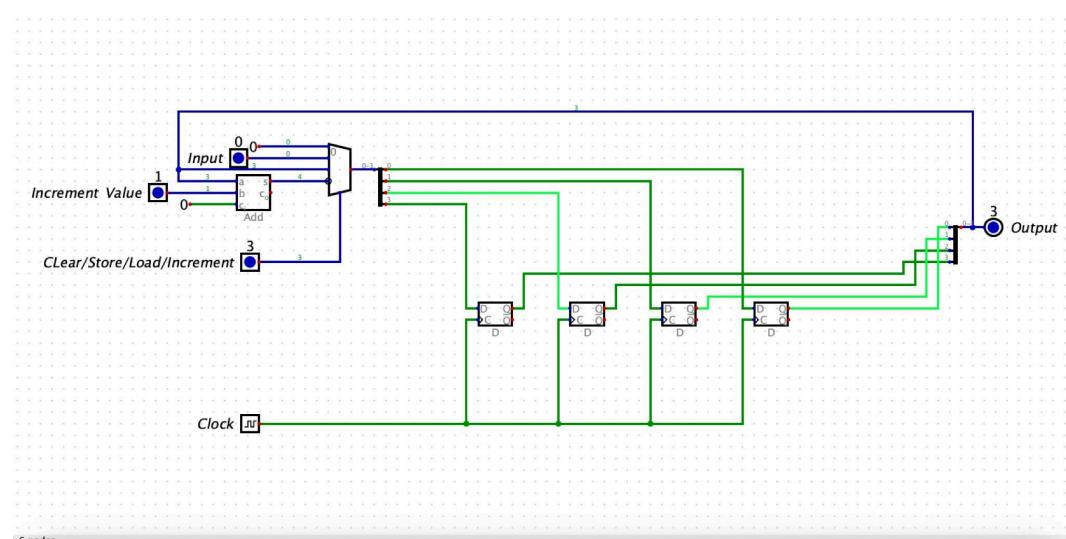
- Clock Cycle 1:



- Clock Cycle 2:

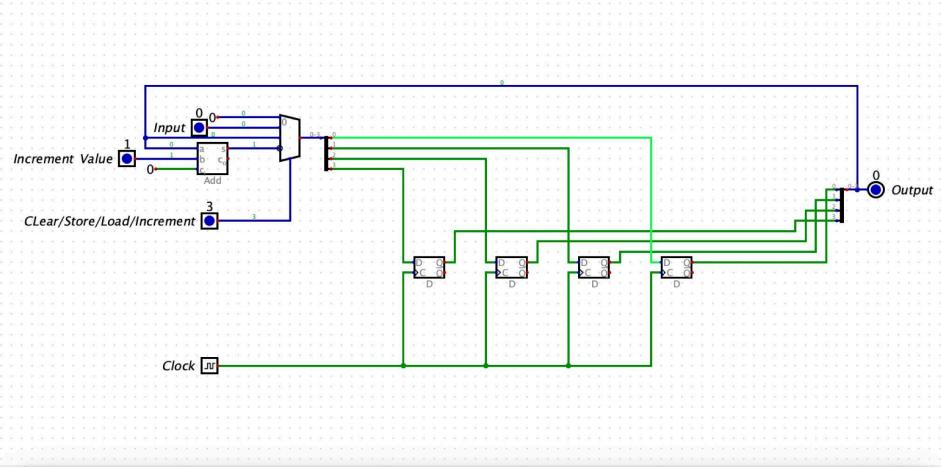


- Clock Cycle 3:

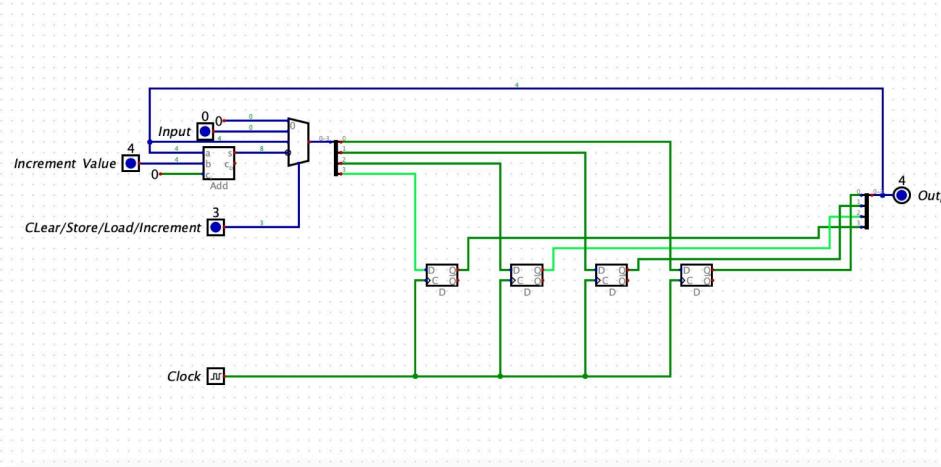


Test Case 2: 4

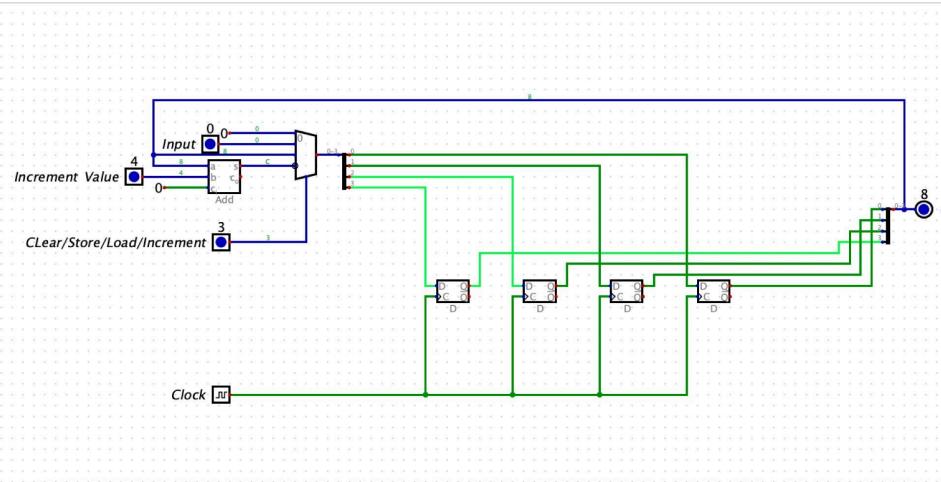
- Clock Cycle 0:



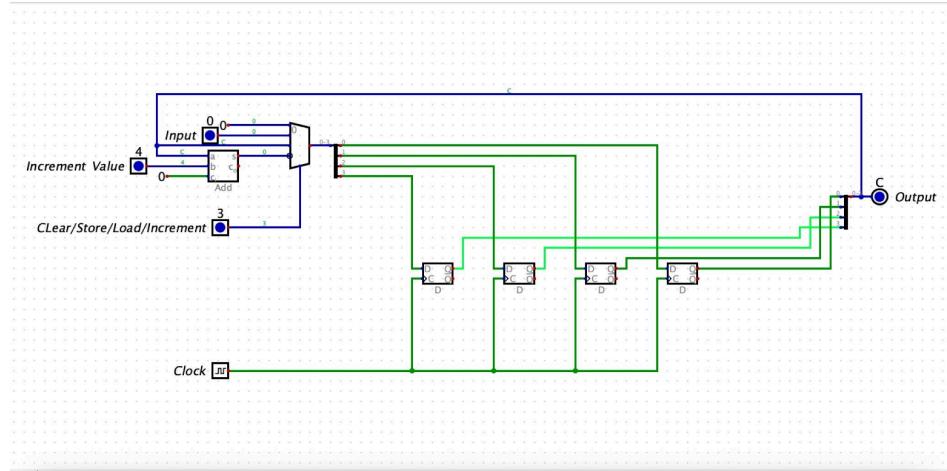
- Clock Cycle 1:



- Clock Cycle 2:

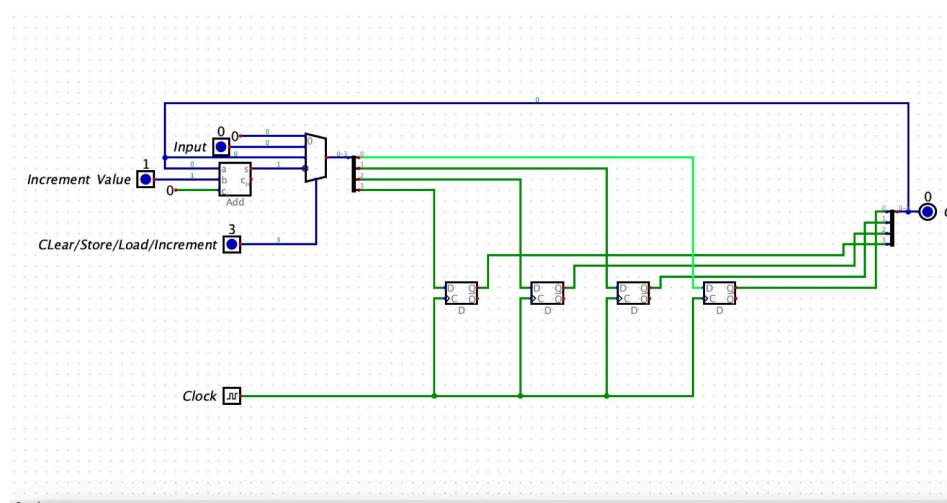


- Clock Cycle 3:

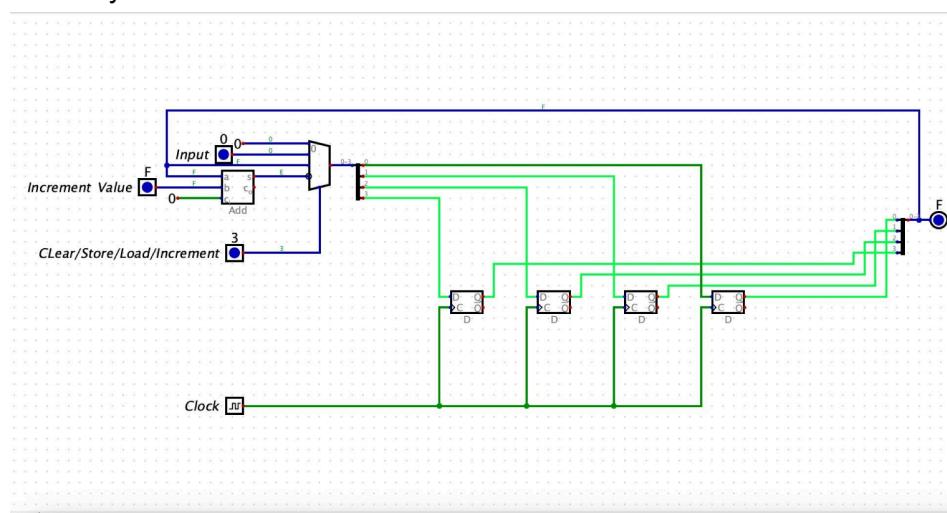


Test Case 3: 15

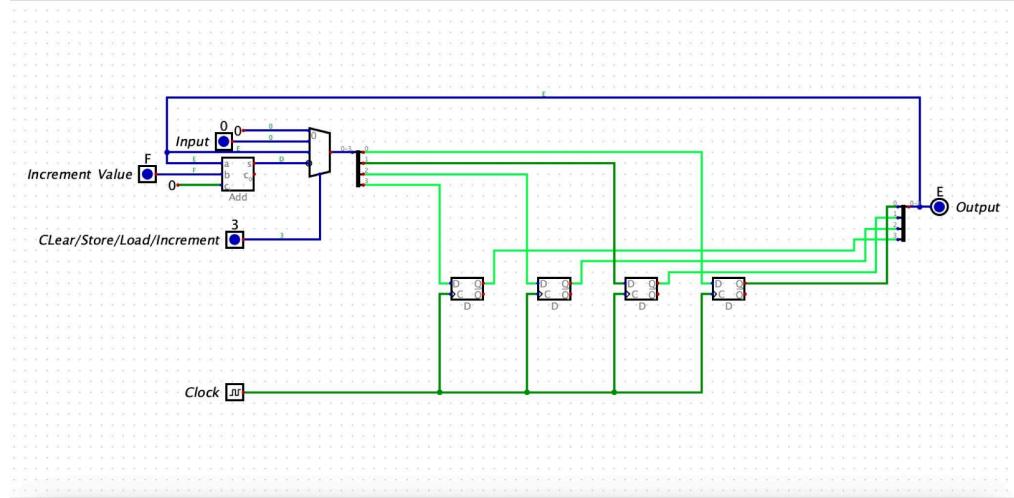
- Clock Cycle 0:



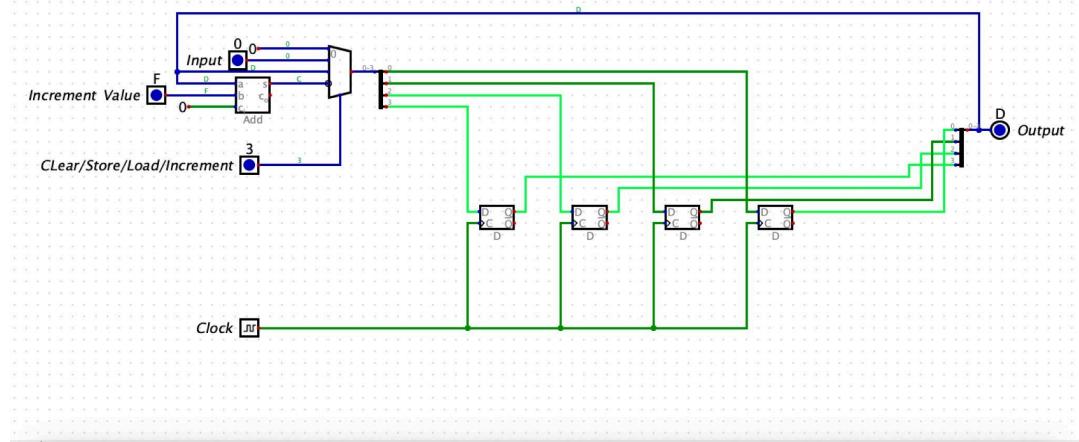
- Clock Cycle 1:



- Clock Cycle 2:

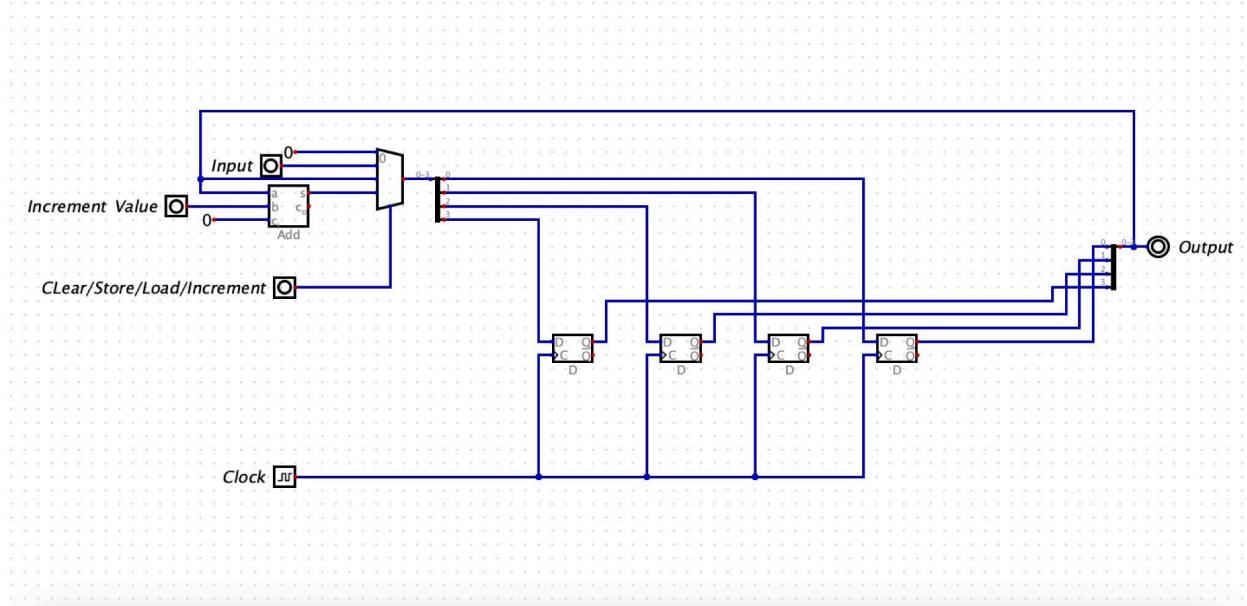


- Clock Cycle 3:



Instruction Register

The Instruction Register we implemented was identical to the Program Counter. It is pictured below.



DRAM

The DRAM is a larger unit of memory than the registers which can store 64 bits of data. It has 4 inputs: the Address Bus, a 4 bit input which is fed as a selector bit into both the decoder and the multiplexer; the Control Bus, a 2 bit input which is fed into each GPR which makes up the DRAM to determine the action performed on each register; the Data Bus, a 4 bit input which determines what value would be stored in each register; and the Clock, which maintains synchronization.

Testing:

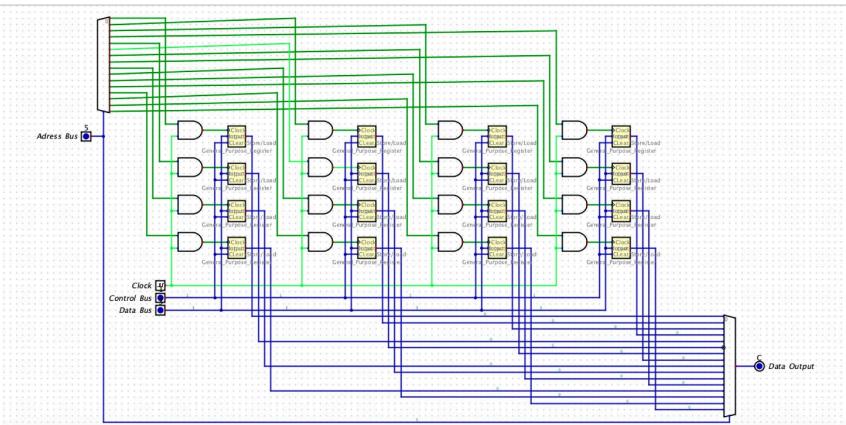
Testing this circuit will consist of choosing values for which register to act on, what data to store, and showing both the read and write functions given the previous data.

Test Case 1:

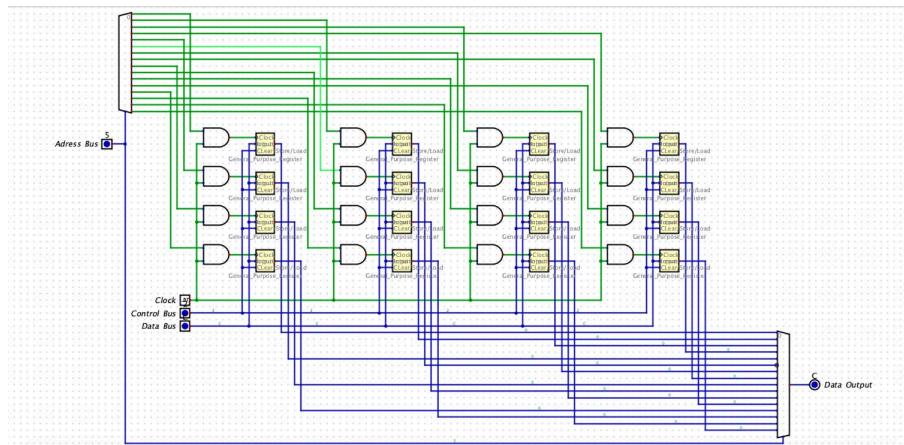
Address Pin: 5

Data Value: 12

- Write:



- Read:

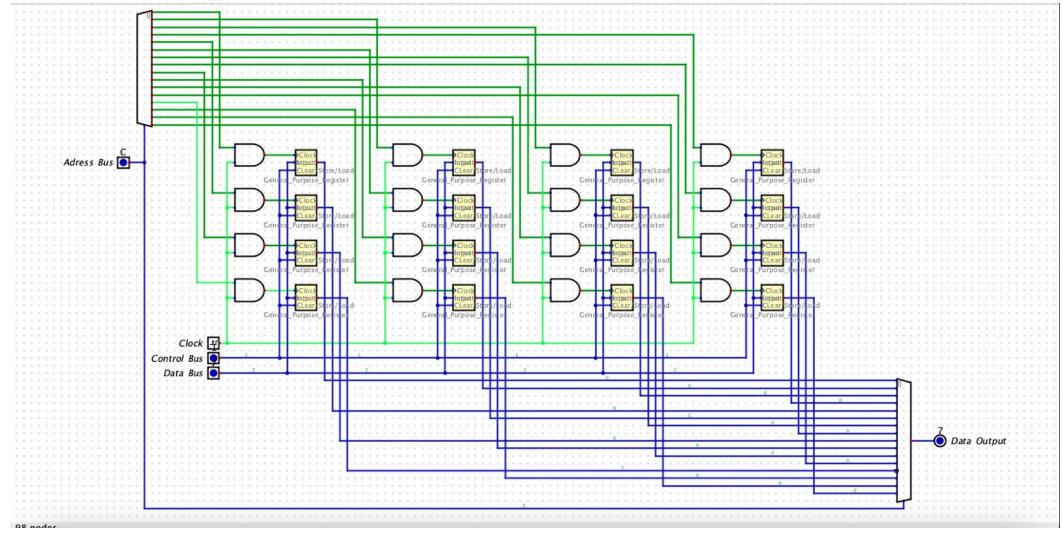


Test Case 2:

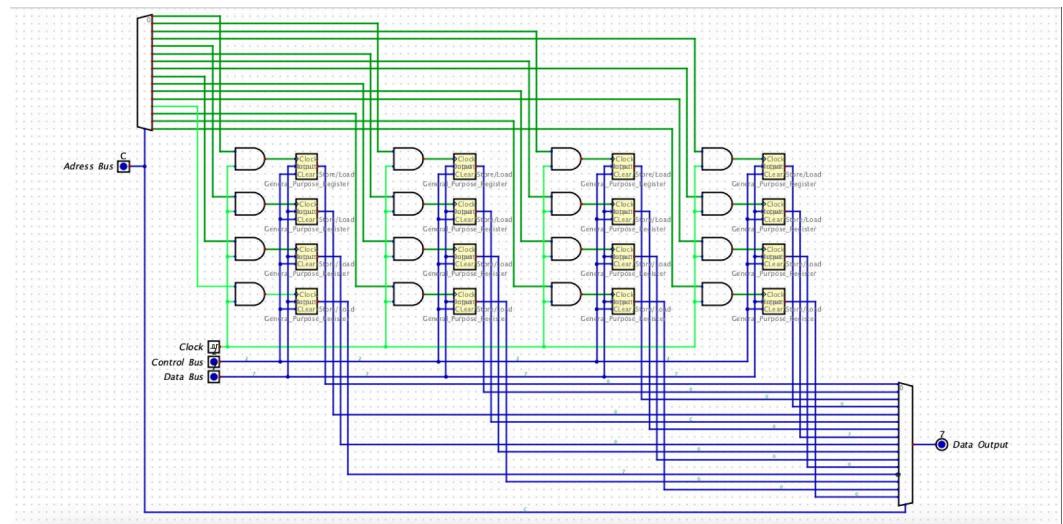
Address Pin: 12

Data Value: 7

- Write:



- Read:

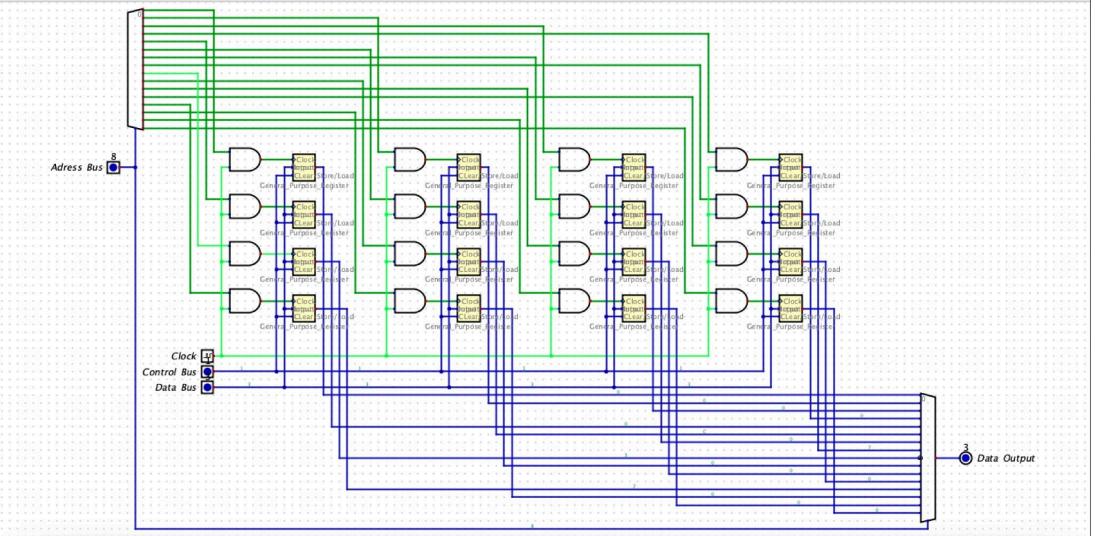


Test Case 3:

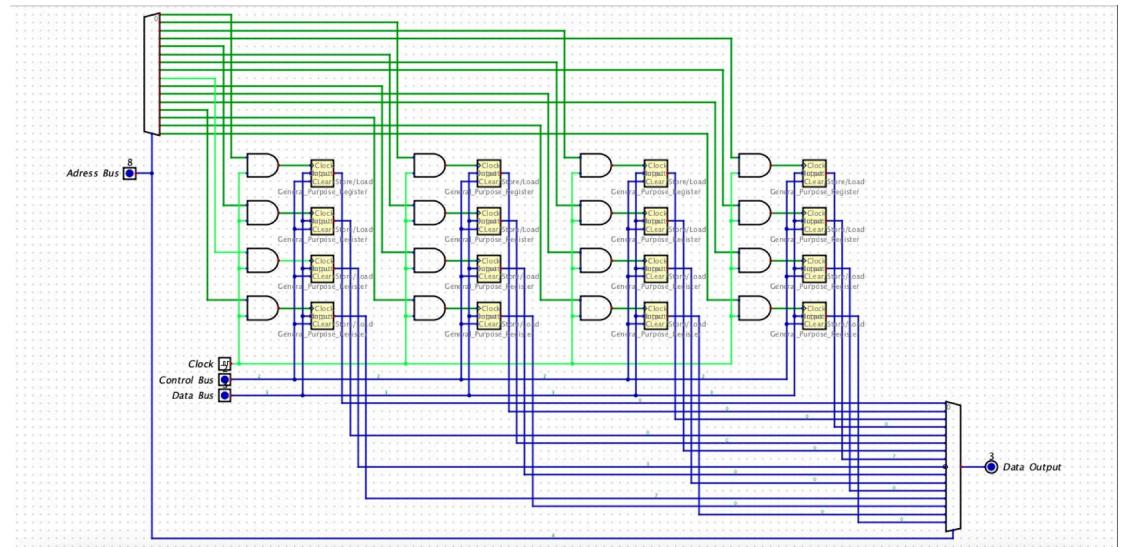
Address Pin: 8

Data Value: 3

- Write:



- Read:



Note:

- Since all test cases are performed on the same instance of the circuit, all registers are storing their respective values simultaneously and can and have been tested to properly retrieve those values.