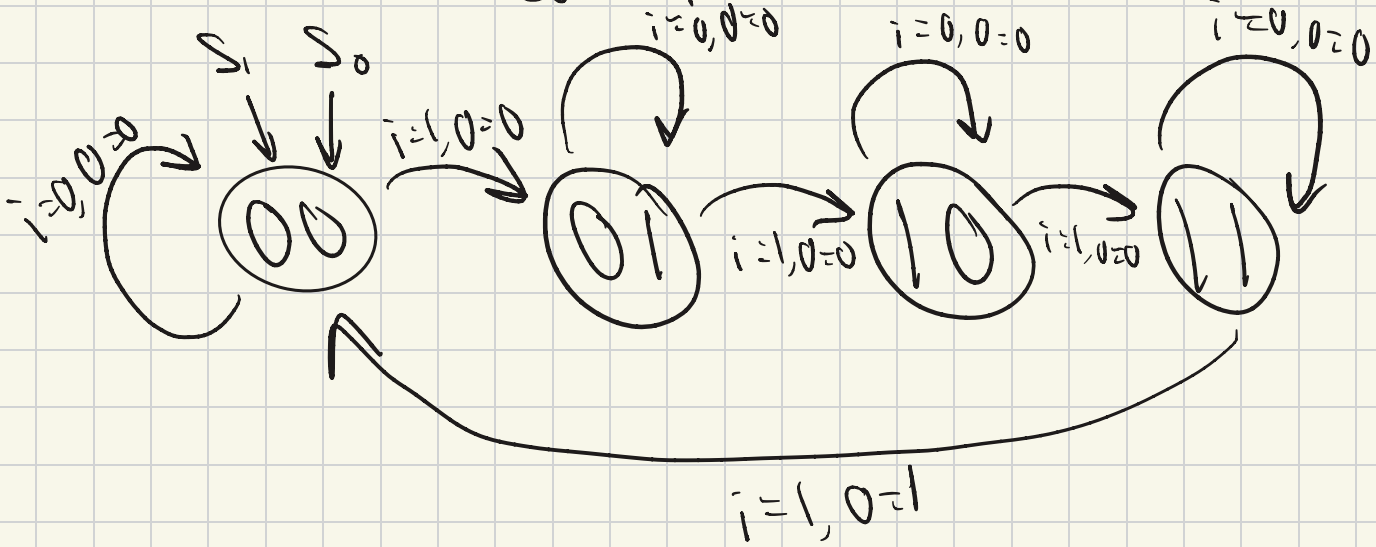
Sequential Logic Circuit

Smaller

→ Counter (2-bit)

→ Control unit



State Diagram

Present State		Inputs	Next State		Output		
S_1^t	S_0^t	i	S_1^{t+1}	S_0^{t+1}	O	D_{S_1}	D_{S_0}
0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	1
0	1	0	0	1	0	0	1
0	1	1	1	0	0	1	0
1	0	0	1	0	0	1	0
1	0	1	1	1	0	1	1
1	1	0	1	1	0	1	1
1	1	1	0	0	1	0	0

D	Q^{t+1}
0	0
1	1

expressions for D-flip flops & output

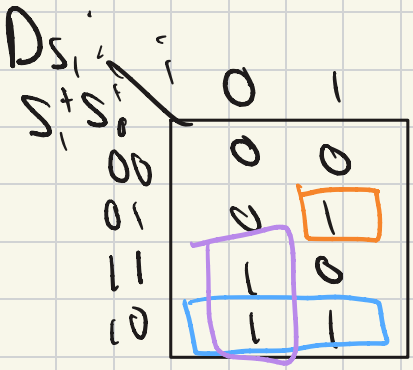
$$D_{S_1} = f(S_1, S_0, i)$$

$$D_{S_0} = f(S_1, S_0, i)$$

$$O = f(S_1, S_0, i)$$

K-map for

D_{S_1}:

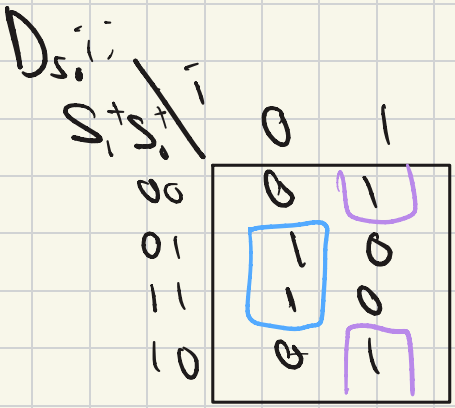


$S_1^+\overline{S_0^+}$ +

$S_1^+\overline{i}$ +

$\overline{S_1^+}S_0^+\overline{i}$

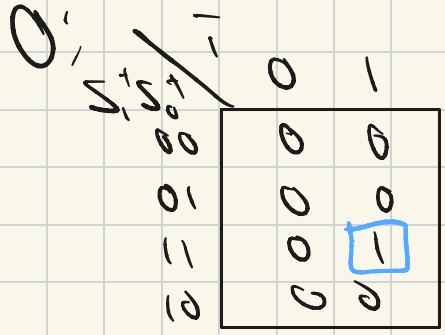
D_{S_0}:



$S_0^+\overline{i}$ +

$\overline{S_0^+}i$

O:



$S_1^+S_0^+\overline{i}$