Quantum legitimacy of reversible gate and a new design of multiplier based on R gate

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Abstract: Quantum full adder plays a key role in the design of quantum computer. The efficiency of quantum adder directly determine the speed of a quantum computer, and the complexity of it is closely related to the difficulty and the cost of building a quantum computer. Existed full adder based on R gate is a great design but it is not suitable to construct a quantum multiplier. In this paper we show the quantum legitimacy of some common reversible gates, then use R gate to propose a new design of quantum full adder. We will use the new designed quantum full adder to optimize the quantum multiplier which is based on R gate. We will show that the new designed one can be optimized by local optimization rule so that it will have lower quantum cost than before.

Keywords: Reversible gate; Quantum full adder; Quantum multiplier

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INTRODUCTION

Quantum computers have far more computing power than classical computers. This is because of the properties called quantum parallel operation. Plenty of questions cannot be solved with a classical computer because it will cost ridiculous resources. Quantum computer can solve some of these problems because of quantum parallel operation. Based on this properties, a lot of quantum algorithms have been designed. Grover's search algorithm[1] and Shor's factorization algorithm are included [2]. Since quantum computer is based on quantum gates, and all quantum gates are reversible, so the research of reversible gates plays an important role in quantum computers.

The research of reversible gates is an important branch of basis mathematics. The reason why reversible gates were the first choice is that it doesn't consume any energy in theory. Based on Landauer's principles[3], if a computation could be done reversibly, then the energy consumed can be zero. Since a reversible gate maps each input vector to an output vector uniquely and vice versa[4], that means a reversible computation doesn't erase any information, it doesn't cost any energy. Besides the application in quantum computer, reversible gates are also widely used in other fields such as: low power CMOS systems[5], optical computing[6], DNA computing[7], nanotechnology[8]. It is very clear that the research of reversible gates will provide a solid theoretical basis for fundamentals and applications.

Arithmetic adders and multipliers are the fundamental component in computational units. It is clear that adders and multipliers are the fundamental of a classical computer. As a result, quantum adder and multiplier should be designed to build a perfect quantum computer. But it lies a question: classical adders and multipliers are irreversible(most of classical logic gate are irreversible such as AND and OR), hence they cannot be used directly in a quantum computer. Thus, quantum arithmetic operations must be built from reversible gates[9]. Based on this idea, lots of reversible adders and multipliers using different reversible gates have been proposed. A design of reversible full adder using two RG gates is introduced in[10]. Thersesal et.al [11]has proposed a new reversible gate called NR gate, then used this gate to construct a full adder and subtractor. Thapilyal et.al [12] used a TR gate to build a full adder, and it has been optimized. Islam et.al [13]has proposed a full adder with two P gates, and the quantum cost of it has been optimized by Anindita Banerjee et.al [14]. A new reversible gate is introduced in[15], then it has been used to made a full adder and subtractor [16].

In this paper, we focus on the quantum legitimacy of main reversible gate and a new design of multiplier using R gate. We are going to show the quantum legitimacy of N gate, C gate, T gate, P gate and R gate. Then we proposed a new design of full adder using R gate. We will show that when we used the new full adder to build a multiplier, our new design multiplier has absolute advantage than using the existed full adder based on R gate, and our design has the lowest garbage bit and quantum cost, then we will explain the advantages of using R gate to build quantum Arithmetic operations. The chapters are distributed as follows: In section 2, we introduced some definitions and facts which will be referred in this paper. Section 3 listed some reversible gates, and show the quantum legitimacy of these reversible gates. In section 4, we proposed a new design of full adder, then build a multiplier with it. In section 5, we will give a conclusion and we will compare our designs with relevant designs proposed by others.

DEFINITIONS AND FACT

First, we recall some basic concepts and facts.

Definition 1. *An m-input, m-output, totally-specified Boolean function is reversible if it maps each input assignment to a unique output assignment.*

Definition 2. *An n-input, n-output gate is reversible if it realizes a reversible function[17].*

Definition 3. *Reversible gate G corresponds to a reversible function f, and it is bijective[18][19].*

As we can seen from the three Definitions above, a reversible gate is equal to a bijective function, and it is a boolean function. It means many properties about bijective function and boolean function are applicable for reversible gates.

Definition 4. *The cost of the circuit is the total cost of all the n gates used to synthesize the circuit[19].*

This Definition give us a way to compute the whole quantum cost of a circuit.

Definition 5. *The constant bit is an input to the circuit used to compute some given logical operations[16].*

Simply, a constant bit is an input bit which value is given.

Definition 6. *Garbage bit is an additional output to the reversible logical gate, that is added to make the number of inputs equal to the number of outputs whenever necessary, in order to achieve reversibility[20].*

Garbage bit is something that people love and hate. The existed of garbage bit makes irreversible gate to reversible gate. the existence of it is essential. But garbage bit will destroy the interference properties crucial to quantum computation. As a result, we should keep its quantity as low as possible, even it will generate additional consumption, especially in quantum computer and quantum computation.

Definition 7. *The quantum cost of any reversible circuit is the number of 2-qubit gates used to build the circuit. Generally speaking, we consider the quantum cost of any 1-qubit gate as zero, the quantum cost of any 2-qubit reversible gate as one, and the quantum cost of the other reversible gates is calculated by counting the number of 2-qubit gates used to build them[18][19].*

Definition 8. *A quantum bit can be defined by a vector, and denoted by qubit. There are two based qubit, 0 and 1. [21]And their corresponding vectors are:* $|0\rangle = \begin{pmatrix} 1 \\ 0 \end{pmatrix}$ *and* $|1\rangle = \begin{pmatrix} 0 \\ 1 \end{pmatrix}$.

Definition 9. *A reversible gate is quantum legitimacy if it can be represented by a unitary matrix M [21].*

COMMON REVERSIBLE GATES AND QUANTUM LEGITIMACY

There are many reversible gates, and these gates can used to constructed lots of circuits. In this section we introduce some common reversible gates and show the matrix of them, so that these reversible gates can be used as quantum gates, which means circuits based on these gates are also suit for quantum computers.

The NOT gate(N) is a one-bit gate, it flips the input bits unconditionally. The quantum cost of NOT gate is zero. it is trivial that for a 1×1 reversible circuit, there is only one NOT gate. In quantum computation, it is called Pauli matrix, and it can be represented by matrix $X = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix}$.

The Controlled-NOT gate or CNOT gate, is a reversible gate, and also a two-qubit quantum gate. The quantum cost of CNOT gate is one. It is easy to see that there are two possible CNOT gates for a 2×2 circuit. The action of the CNOT gate is given by $|c\rangle|t\rangle \rightarrow |c\rangle|c \oplus t\rangle$, that is, if the control qubit is set to $|1\rangle$ then the target qubit is flipped, otherwise the target qubit is let alone. Thus, the matrix representation of CNOT are

$$C(1,2) = \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \end{pmatrix} \text{ and } C(2,1) = \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 \end{pmatrix}.$$

The Toffoli gate (T), is a 3×3 reversible gate, and also a three-qubit quantum gate. The quantum cost of Toffoli gate is five. There are three possible Toffoli gates for a 3×3 circuit. The circuit representation is showed in FIG. 1. The action of the Toffoli gate is given by $|a\rangle|b\rangle|c\rangle \rightarrow |ab\rangle \oplus c\rangle$, that is, if the control qubit $|x\rangle$ and $|y\rangle$ are set to $|1\rangle$ at the same time, then the target qubit is flipped, otherwise the target qubit is let alone. Thus, the matrix representation of Toffoli gates are

$$T(1,2,3) = \begin{pmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \end{pmatrix},$$

$$T(1,3,2) = \begin{pmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \end{pmatrix},$$

and

$$T(2,3,1) = \begin{pmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \end{pmatrix}.$$

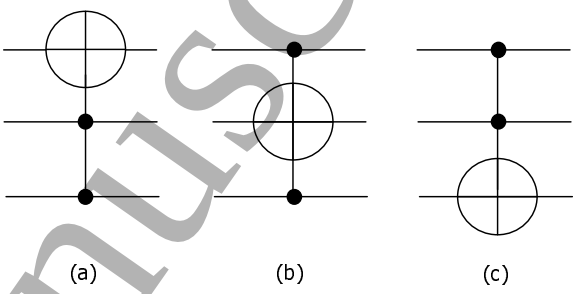

FIG. 1: The Toffoli Gate, figure (a) represent T(2,3,1), figure (b) represent T(1,3,2) and figure (c) represent T(1,2,3).

The Fredkin gate (F), is a 3×3 reversible gate, and also a three-qubit quantum gate. The quantum cost of Fredkin gate is five, which is optimized in [22]. There are three possible Fredkin gates for a 3×3 circuit. The circuit representation is showed in FIG. 2. The action of the Fredkin gate is if the control qubit $|x\rangle$ is set to $|1\rangle$, then swap the values of the other two qubits, otherwise the gate will do nothing. Thus, the matrix representation of Fredkin gates are

$$F(1,2,3) = \begin{pmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{pmatrix},$$

$$F(2,1,3) = \begin{pmatrix} 1&0&0&0&0&0&0&0\\ 0&1&0&0&0&0&0&0\\ 0&0&1&0&0&0&0&0\\ 0&0&0&0&0&0&1&0\\ 0&0&0&0&1&0&0&0\\ 0&0&0&0&0&1&0&0\\ 0&0&0&1&0&0&0&0\\ 0&0&0&0&0&0&0&1 \end{pmatrix}$$

and

$$F(3,1,2) = \begin{pmatrix} 1&0&0&0&0&0&0&0\\ 0&1&0&0&0&0&0&0\\ 0&0&1&0&0&0&0&0\\ 0&0&0&0&0&1&0&0\\ 0&0&0&0&1&0&0&0\\ 0&0&0&1&0&0&0&0\\ 0&0&0&0&0&0&1&0\\ 0&0&0&0&0&0&0&1 \end{pmatrix}.$$

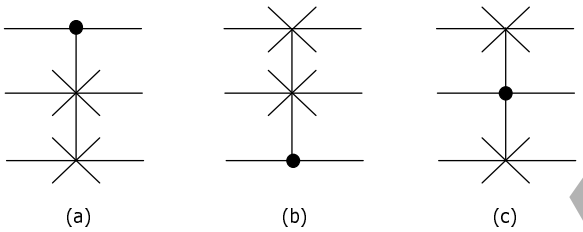

FIG. 2: The Fredkin Gate, figure (a) represent F(1,2,3), figure (b) represent F(3,1,2) and figure (c) represent F(2,1,3).

The R^n gate is a n-qubit universal reversible gate, we can make a universal gate library only used R^n gate. It is first introduced in [15], and used to construct a full adder/substractor in [16]. It combines the functionality of the NOT gate, the CNOT gate and the Toffoli gate. We will make a multiplier using R^3 gate, so we introduce R^1, R^2 and R^3 only.

R^1 gate is just like NOT gate, it is a 1×1 gate, and flips the input qubit unconditionally. The quantum cost of R^1 gate is zero.

R^2 gate is a combine of NOT gate and CNOT gate. If the control qubit is set to $|1\rangle$ then the target qubit is flipped, otherwise the target qubit is let alone, then flips the control qubit unconditionally. The quantum cost of R^2 gate is one. There are two possible R^2 gate for a 2×2 circuit and FIG. 3 shows the circuit representation. It can be represented by $R^2(1,2) = \begin{pmatrix} 0&0&1&0\\ 0&0&0&1\\ 0&1&0&0\\ 1&0&0&0 \end{pmatrix}$ and $R^2(2,1) = \begin{pmatrix} 0&1&0&0\\ 0&0&1&0\\ 0&0&0&1\\ 1&0&0&0 \end{pmatrix}$. So R^2 gate is a quantum gate.

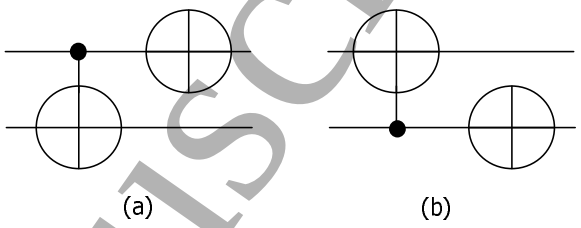

FIG. 3: The R^2 Gate, figure (a) represent R(1,2) and figure (b) represent R(2,1).

The R^3 gate is a three-qubit gate, the function of this gate can be described as follow: first use $|x\rangle$ and $|y\rangle$ as control bits to flip $|z\rangle$. Second $|x\rangle$ used as a control bit to flip $|y\rangle$, then flips $|z\rangle$ unconditionally. Finally use $|z\rangle$ as control bit to flip $|x\rangle$. The quantum cost of R^3 gate can be optimized to four with moving rules[23][24]. There are six possible R^3 gates for a 3×3 circuit. FIG. 4 shows the circuit representation and FIG. 5 shows the optimization process. It is easy to calculate the matrix corresponding to each R^3 gate, we list the calculation results below.

$$R^3(1,2,3) = \begin{pmatrix} 0&0&1&0&0&0&0&0\\ 0&0&0&1&0&0&0&0\\ 0&0&0&0&0&0&0&1\\ 0&0&0&0&1&0&0&0\\ 0&0&0&0&0&1&0&0\\ 0&0&0&0&0&0&1&0\\ 1&0&0&0&0&0&0&0\\ 0&1&0&0&0&0&0&0 \end{pmatrix},$$

$$R^3(1,3,2) = \begin{pmatrix} 0&1&0&0&0&0&0&0\\ 0&0&0&0&0&0&0&1\\ 0&0&0&1&0&0&0&0\\ 0&0&0&0&1&0&0&0\\ 0&0&0&0&0&0&1&0\\ 1&0&0&0&0&0&0&0\\ 0&0&0&0&0&1&0&0\\ 0&0&1&0&0&0&0&0 \end{pmatrix},$$

$$R^3(2,1,3) = \begin{pmatrix} 0&0&0&0&1&0&0&0\\ 0&0&0&1&0&0&0&0\\ 0&0&0&0&0&0&1&0\\ 0&0&0&0&0&1&0&0\\ 0&0&0&0&0&0&0&1\\ 1&0&0&0&0&0&0&0\\ 0&1&0&0&0&0&0&0\\ 0&0&1&0&0&0&0&0 \end{pmatrix},$$

$$R^3(2,3,1) = \begin{pmatrix} 0&0&0&0&1&0&0&0\\ 0&0&0&0&0&1&0&0\\ 0&0&0&1&0&0&0&0\\ 0&0&0&0&0&0&1&0\\ 0&0&0&0&0&0&0&1\\ 0&0&1&0&0&0&0&0\\ 1&0&0&0&0&0&0&0\\ 0&1&0&0&0&0&0&0 \end{pmatrix},$$

$$R^3(3,1,2) = \begin{pmatrix} 0&1&0&0&0&0&0&0\\ 0&0&0&0&0&0&0&1\\ 0&0&0&0&0&0&1&0\\ 1&0&0&0&0&0&0&0\\ 0&0&0&0&0&1&0&0\\ 0&0&1&0&0&0&0&0\\ 0&0&0&1&0&0&0&0\\ 0&0&0&0&1&0&0&0 \end{pmatrix},$$

$$R^3(3,2,1) = \begin{pmatrix} 0&0&1&0&0&0&0&0\\ 0&0&0&0&0&1&0&0\\ 0&0&0&0&0&0&0&1\\ 1&0&0&0&0&0&0&0\\ 0&0&0&0&0&0&1&0\\ 0&0&0&1&0&0&0&0\\ 0&1&0&0&0&0&0&0\\ 0&0&0&0&1&0&0&0 \end{pmatrix}.$$

As a result, R^3 gate is a quantum gate.

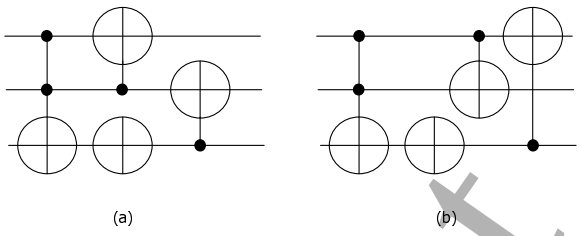

FIG. 4: The R^3 Gate, figure (a) represent R(3,1,2), figure (b) represent R(1,3,2). We haven't list every representation of R^3 gate, the other is similar to these two examples.

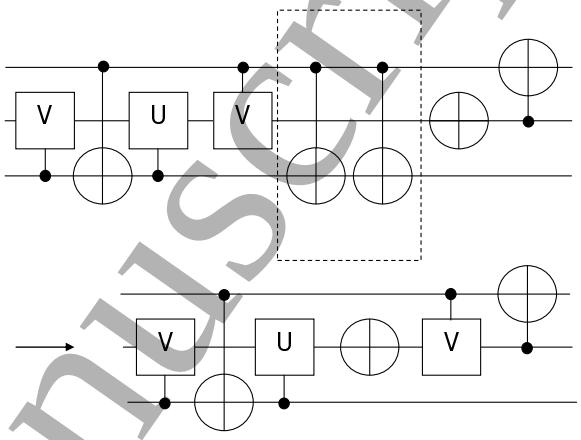

FIG. 5: The Optimization Process

PROPOSED MULTIPLIER

In this section, we will proposed three new designs, which are half adder, full adder and multiplier, designed using R gate.

A half adder can calculate the operation $S = X + Y$ and the carry out bit C. The combination of $R^3(3,1,2)$ and $R^2(2,1)$ can do this. we use three input qubit $|x\rangle$, $|y\rangle$, which is the target value, and a constant qubit $|0\rangle$. We will get three output qubit, the first one is the summation bit S_i, the second one is a garbage bit, and the third one is the carry out bit C_i. The quantum cost of our half adder is four. FIG. 6 shows the proposed half adder.

Using this half adder, we can make a full adder. FIG. 7 shows the full adder. This design use two half adder, using one constant bit and produce two garbage bit, the quantum cost of this full adder is six. FIG. 8 shows the optimized process.

Now we can apply our half adder and full adder to build a multiplier. A multiplier is consist of a partial

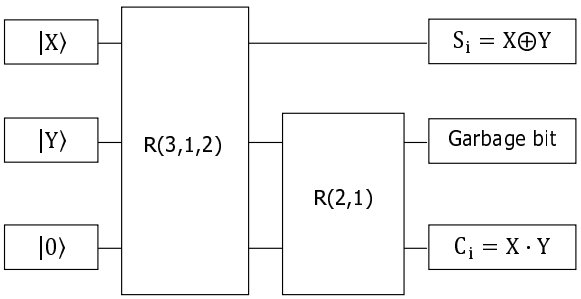

FIG. 6: The Half Adder Using R Gate

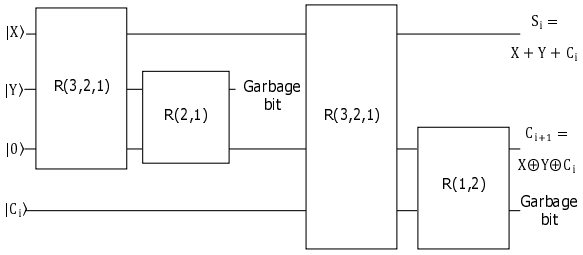

FIG. 7: The Full Adder Using R Gate

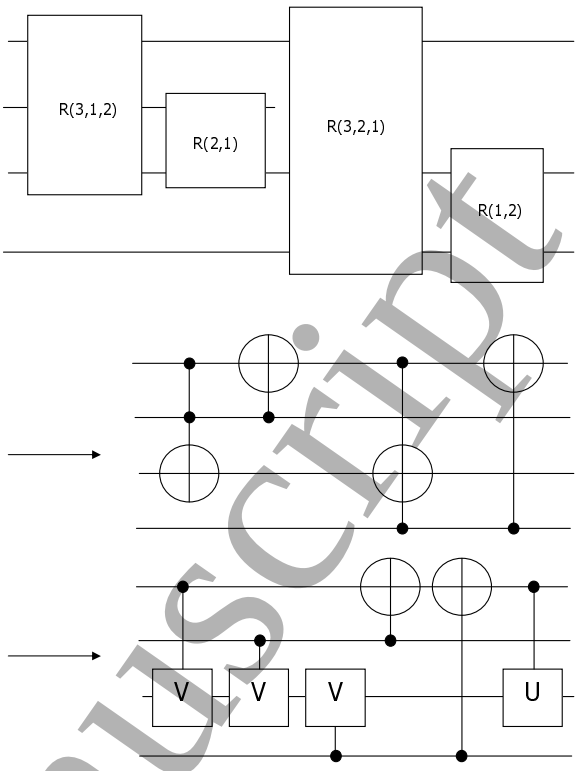

FIG. 8: The Optimization Process

product generator circuit(PPCG) and a reversible parallel adder(RPA), we use the partial product generator circuit proposed in [14], then give the structure of an array multiplier in FIG.9.

It should be noted that the PPCG proposed in [14] use only Toffoli gate, but we choose R gate library instead of NCT gate, it means we need more R gate to synthesize a Toffoli gate in order to use this PPCG. However, it is worth. On one hand, this circuit produce the lowest garbage bit, which is of great importance in a quantum computer. On the other hand, based on the view of [14], more quantum gates does not means more quantum cost. After simplification, we use the same numbers of N, V and U gates, which mean in actual use, they do not make any difference, as a result, the gate number is out of consideration in this paper.

Finally, we compared our designs with the past work in TABLE I and TABLE II. Among them, TABLE I shows the comparison of different full adders, and TABLE II shows the comparison of different multipliers. It is easy to see from TABLE I that our design have lower quantum cost than existing design using R gate[16], and have the same garbage bit and quantum cost as the existing design[14], which means it is the best design. From

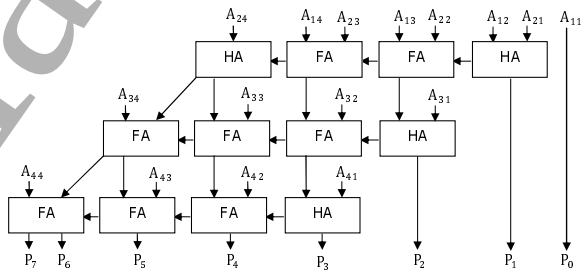

FIG. 9: RPA Circuit

TABLE II, we can see that our design is better than using the full adder proposed in [16], and have the lowest total cost.

TABLE I: comparison of full adder

	Garbage Bit	Quantum Cost	Total cost
Proposed full adder	2	6	8
Full adder/substractor[16]	1	8	9
Existing full adder[13]	2	8	10
Existing full adder[14]	2	6	8

TABLE II: comparison of full adder

	Garbage bit	Quantum Cost	Total cost
Proposed multiplier	28	144	172
multiplier using[16]	28	160	188
Existing multiplier[14]	28	144	172
Existing multiplier[13]	52	140	192

CONCLUSION AND DISCUSSION

We have show the quantum legitimacy of some common reversible gate and give a new design of multiplier. It is very meaningful to show the quantum legitimacy of reversible gate. The different between a reversible gate and a quantum gate is that a reversible use zero or one as input while a quantum gate use vector $|0\rangle$ and $|1\rangle$ as input. However, giving a matrix representation to a reversible gate means it can deal with a vector input which means many results based on reversible gates can be applied to quantum computer directly, and promote the research and development of related interdisciplinary subjects.

Our designs use local optimization rule in order to achieve the limit optimization of quantum cost and garbage bit, in this point it is similar to the existing design. However, compared with existed designs, our design have lots of differences and advantages. The most obvious thing is that we use a new library. Our new designs are based on R gate library. R gate library is better than other gate library in many ways such as the size of minimal universal sub libraries, utilization of gate, the minimal length and so on. As a result, in the same condition, R gate library is a better choice than NCT gate library. But as is shown in TABLE II, the multiplier used the previous adders is not optimal. Our design make up for its defects in the multiplier part, and make the R gate library more advantageous in theoretical research and practical use. Moreover, Our design pays more attention to the optimization of garbage bit, although it use a little more gates, but it's worth it. Regarding the comparison between our designs and the previous results, we have done a detailed analysis in TABLE I and TABLE II.

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