Application Note 42047

Power Factor Correction (PFC) Basics

What is Power Factor?

Power factor (pf) is defined as the ratio of the real power (P) to apparent power (S), or the cosine (for pure sine wave for both current and voltage) that represents the phase angle between the current and voltage waveforms (see Figure 1). The power factor can vary between 0 and 1, and can be either inductive (lagging, pointing up) or capacitive (leading, pointing down). In order to reduce an inductive lag, capacitors are added until pf equals 1. When the current and voltage waveforms are in phase, the power factor is 1 (cos (0°) = 1). The whole purpose of making the power factor equal to one is to make the circuit look purely resistive (apparent power equal to real power).

Real power (watts) produces real work; this is the energy transfer component (example electricity-to-motor rpm). Reactive power is the power required to produce the magnetic fields (lost power) to enable the real work to be done, where apparent power is considered the total power that the power company supplies, as shown in Figure 1. This total power is the power supplied through the power mains to produce the required amount of real power.

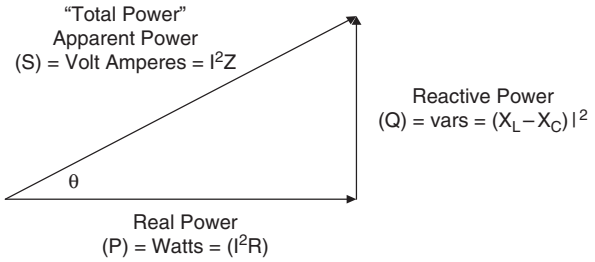

Figure 1. Power Factor Triangle (Lagging)

The previously-stated definition of power factor related to phase angle is valid when considering ideal sinusoidal waveforms for both current and voltage; however, most power supplies draw a non-sinusoidal current. When the current is not sinusoidal and the voltage is sinusoidal, the power factor consists of two factors: 1) the displacement factor related to phase angle and 2) the distortion factor related to wave shape. Equation 1 represents the relationship of the displacement and distortion factor as it pertains to power factor.

$$PF = \frac{Irms(1)}{Irms}\cos\theta = Kd \cdot K\theta \quad (1)$$

Irms(1) is the current's fundamental component and *Irms* is the current's RMS value. Therefore, the purpose of the power factor correction circuit is to minimize the input current distortion and make the current in phase with the voltage.

When the power factor is not equal to 1, the current waveform does not follow the voltage waveform. This results not only in power losses, but may also cause harmonics that travel down the neutral line and disrupt other devices connected to the line. The closer the power factor is to 1, the closer the current harmonics will be to zero since all the power is contained in the fundamental frequency.

Understanding Recent Regulations

In 2001, the European Union put EN61000-3-2, into effect to establish limits on the harmonics of the ac input current up to the 40th harmonic. Before EN61000-3-2 came into effect, there was an amendment to it passed in October 2000 that stated the only devices required to pass the rigorous Class D (Figure 2) emission limits are personal computers, personal computer monitors, and television receivers. Other devices were only required to pass the relaxed Class A (Figure 3) emission limits.

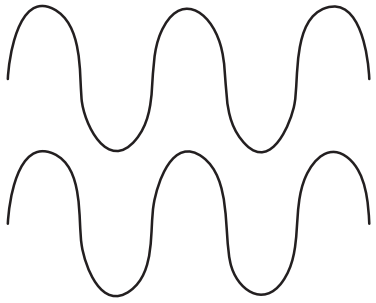

Figure 2. Both Current and Voltage Waveforms are in Phase with a pF =1 (Class D)

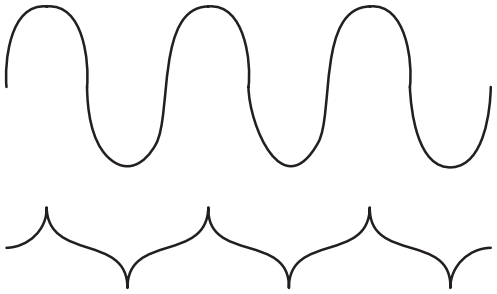

Figure 3: This is What is Called Quasi-PFC Input, Achieving a pF Around 0.9 (Class A)

Causes of Inefficiencies

One problem with switch mode power supplies (SMPS) is that they do not use any form of power factor correction and that the input capacitor C_{IN} (shown in Figure 4) will only charge when V_{IN} is close to V_{PEAK} or when V_{IN} is greater

than the capacitor voltage V_{CIN}. If C_{IN} is designed using the input voltage frequency, the current will look much closer to the input waveform (load dependent); however, any little interruption on the mainline will cause the entire system to react negatively. In saying that, in designing a SMPS, the hold-up time for C_{IN} is designed to be greater than the frequency of $V_{IN,}$ so that if there is a glitch in V_{IN} and a few cycles are missed, C_{IN} will have enough energy stored to continue to power its load.

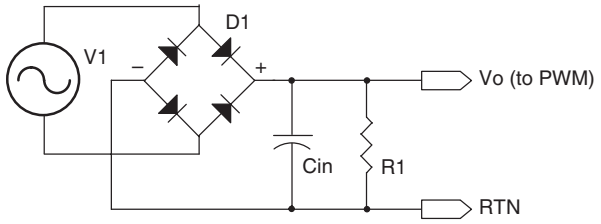

Figure 4. SMPS Input Without PFC

Figure 5 represents a theoretical result of $V_{CIN}(t)$ (shown in the circuit in Figure 4) with a very light load, and hence, very little discharge of C_{IN}. As the load impedance increases, there will be more droop from $V_{CIN}(t)$ between subsequent peaks, but only a small percentage with respect to the overall V_{IN} (e.g. with the input being 120V, maybe a 3-5 volt droop. As previously stated, C_{IN} will only charge when V_{IN} is greater than its stored voltage, meaning that a non-PFC circuit will only charge C_{IN} a small percentage of the overall cycle time.

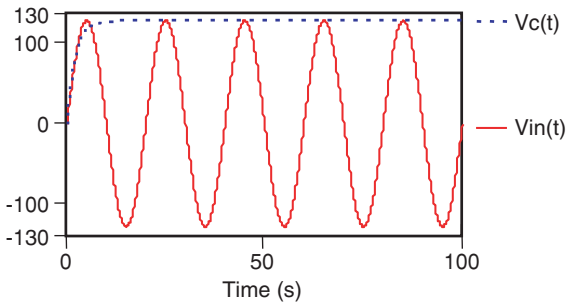

Figure 5. V_{IN} with Charging C_{IN}

After 90 degrees (Figure 6), the half cycle from the bridge drops below the capacitor voltage (C_{IN}); which back biases the bridge, inhibiting current flow into the capacitor (via V_{IN}). Notice how big the input current spike of the inductor is. All the circuitry in the supply chain (the wall wiring, the diodes in the bridge, circuit breakers, etc) must be capable of carrying this huge peak current. During these short periods the C_{IN} must be fully charged, therefore large pulses of current for a short duration are drawn from V_{IN}. There is a way to average this spike out so it can use the rest of the cycle to accumulate energy, in essence smoothing out the huge peak current, by using power factor correction.

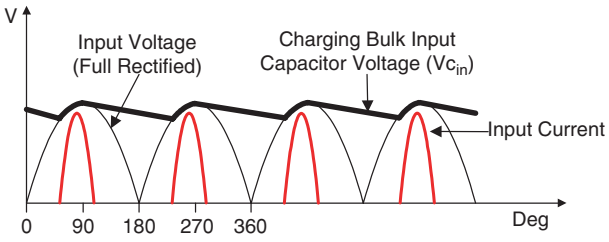

Figure 6. Voltage and Current Waveforms in a Simple Rectifier Circuit

In order to follow V_{IN} more closely and not have these high amplitude current pulses, C_{IN} must charge over the entire cycle rather than just a small portion of it. Today's non-linear loads make it impossible to know when a large surge of current will be required, so keeping the inrush to the capacitor constant over the entire cycle is beneficial and allows a much smaller C_{IN} to be used. This method is called power factor correction.

Boost Converters the Heart of Power Factor Correction

Boost converter topology is used to accomplish this active power-factor correction in many discontinuous/continuous modes. The boost converter is used because it is easy to implement and works well. The simple circuit in Figure 7 is a short refresher of how inductors can produce very high voltages. Initially, the inductor is assumed to be uncharged, so the voltage V_O is equal to $V_{IN.}$ When the switch closes, the current (I_L) gradually increases through it linearly since:

$$I_L = \frac{1}{L}\int V_L dt.$$

Voltage (V_L) across it increases exponentially until it stabilizes at V_{IN}. Notice the polarity of the voltage across the inductor, as it is defined by the current direction (inflow side is positive). When the switch opens causing the current to change from I_{max} to zero (which is a decrease, or a negative slope). Looking at it mathematically:

$$V_L = L\frac{di}{dt} \approx L\frac{\Delta i}{\Delta t},$$

or L times the change in current per unit time, the voltage approaches negative infinity (the inductor reverses polarity). Because the inductor is not ideal, it contains some amount of series resistance, which loads this "infinite" voltage to a finite number. With the switch open, and the inductor discharging, the voltage across it reverses and becomes additive with the source voltage V_{IN}. If a diode and capacitor were connected to the output of this circuit, the capacitor would charge to this high voltage (perhaps after many switch cycles). This is how boost converters boost voltage, as shown in Figure 8.

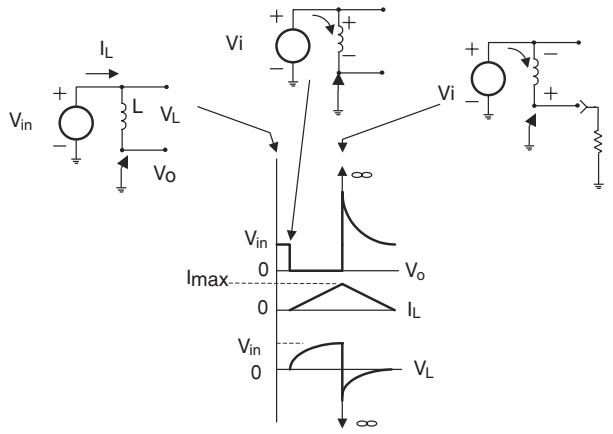

Figure 7. Flyback Action of an Inductor

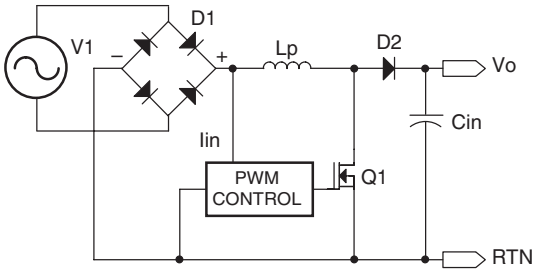

Figure 8. PFC Boost Pre-Regulator

The input to the converter is the full-rectified AC line voltage. No bulk filtering is applied following the bridge rectifier, so the input voltage to the boost converter ranges (at twice line frequency) from zero volts to the peak value of the AC input and back to zero. The boost converter must meet two simultaneous conditions: 1) the output voltage of the boost converter must be set higher than the peak value (hence the word boost) of the line voltage (a commonly used value is 385VDC to allow for a high line of 270VACrms), and 2) the current drawn from the line at any given instant must be proportional to the line voltage.

Without using power factor correction a typical switched-mode power supply would have a power factor of around 0.6, therefore having considerable odd-order harmonic distortion (sometimes with the third harmonic as large as the fundamental). Having a power factor of less than 1 along with harmonics from peaky loads reduces the real power available to run the device. In order to operate a device with these inefficiencies, the power company must supply additional power to make up for the loss. This increase in power causes the power companies to use heavier supply lines, otherwise self-heating can cause burnout in the neutral line conductor. The harmonic distortion can cause an increase in operating temperature of the generation facility, which reduces the life of equipment including rotating machines, cables, transformers, capacitors, fuses, switching contacts, and surge suppressors. Problems are caused by the harmonics creating additional losses and dielectric stresses in capacitors and cables, increasing currents in windings of rotating machinery and transformers and noise emissions in many products, and bringing about early failure of fuses and other safety components. They also can cause skin effect, which creates problems in cables, transformers, and rotating machinery. This is why power companies are concerned with the growth of SMPS, electronic voltage regulators, and converters that will cause THD levels to increase to unacceptable levels. Having the boost preconverter voltage higher than the input voltage forces the load to draw current in phase with the ac main line voltage that, in turn, rids harmonic emissions.

Modes of Operation

There are two modes of PFC operation; discontinuous and continuous mode. Discontinuous mode is when the boost converter's MOSFET is turned on when the inductor current reaches zero, and turned off when the inductor current meets the desired input reference voltage as shown in Figure 9. In this way, the input current waveform follows that of the input voltage, therefore attaining a power factor of close to 1.

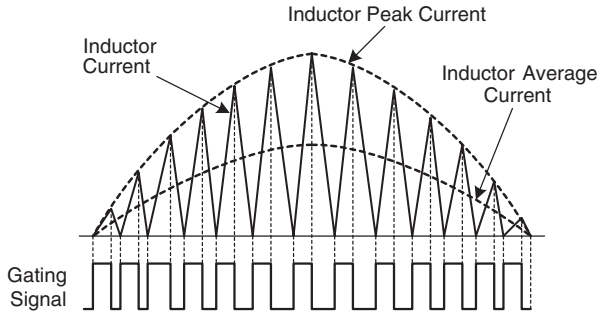

Figure 9. Discontinuous mode of operation

Discontinuous mode can be used for SMPS that have power levels of 300W or less. In comparison with continuous mode devices, discontinuous ones use larger cores and have higher I^2R and skin effect losses due to the larger inductor current swings. With the increased swing a larger input filter is also required. On the positive side, since discontinuous mode devices switch the boost MOSFET on when the inductor current is at zero, there is no reverse recovery current (I_{RR}) specification required on the boost diode. This means that less expensive diodes can be used.

Continuous mode typically suits SMPS power levels greater than 300W. This is where the boost converter's MOSFET does not switch on when the boost inductor is at zero current, instead the current in the energy transfer inductor never reaches zero during the switching cycle (Figure 10).

With this in mind, the voltage swing is less than in discontinuous mode—resulting in lower I^2R losses—and the lower ripple current results in lower inductor core losses. Less voltage swing also reduces EMI and allows for a smaller input filter to be used. Since the MOSFET is not being turned on when the boost inductor's current is at zero, a very fast reverse recovery diode is required to keep losses to a minimum.

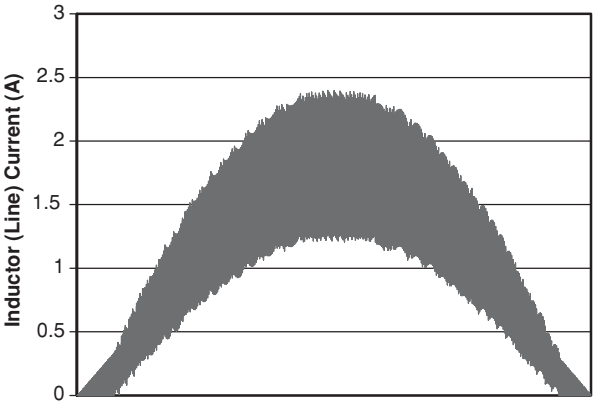

Figure 10. Continuous Mode of Operation

Fairchild offers products for all discontinuous and continuous modes of PFC operation, including critical conduction mode (FAN7527B), average current mode (FAN4810), and input current shaping mode (FAN4803).

Discontinuous Mode:

Critical Conduction Mode

A Critical Conduction mode device is a voltage mode device that works in the area between continuous and discontinuous mode. To better explain critical conduction mode lets look at the difference between discontinuous and continuous mode in a SMPS design such as a flyback converter. In discontinuous mode, the primary winding of the transformer has a dead time once the switch is turned off (including is a minimum winding reset time) and before it is energized again (Figure 11).

Figure 11. Discontinuous Mode, Flyback Power Supply Ip (Primary Current)

In continuous mode, the primary winding has not fully depleted all of its energy. Figure 12 shows that the primary winding does not start energizing at zero, rather residual current still resides in the winding.

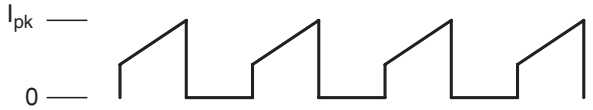

Figure 12. Continuous Mode, Flyback Power Supply I_P (Primary Current)

In critical conduction mode there are no dead-time gaps between cycles and the inductor current is always at zero before the switch is turned on. In Figure 9, the ac line current is shown as a continuous waveform where the peak switch current is twice the average input current. In this mode, the operation frequency varies with constant on time.

Continuous Mode:

Average Current Mode

The heart of the PFC controller is the gain modulator. The gain modulator has two inputs and one output. As shown in Figure 13, the left input to the gain modulator block is called the reference current (I_{SINE}). The reference current is the input current that is proportional to the input full-wave-rectified voltage. The other input, located at the bottom of the gain modulator, is from the voltage error amplifier. The error amplifier takes in the output voltage (using a voltage divider) after the boost diode and compares it to a reference voltage of 5 volts. The error amplifier will have a small bandwidth so as not to let any abrupt changes in the output or ripple erratically affect the output of the error amplifier.

The gain modulator multiplies or is the product of the reference current and the error voltage from the error amplifier (defined by the output voltage).

Figure 13 shows the critical blocks within the ML4821 (a stand alone PFC controller) to produce a power factor of greater than 95 percent. These critical blocks include the current control loop, voltage control loop, PWM control, and the gain modulator.

The purpose of the current control loop is to force the current waveform to follow the shape of the voltage waveform. In order for the current to follow the voltage, the internal current amplifier has to be designed with enough bandwidth[1] to capture enough of the harmonics of the output voltage. This bandwidth is designed using external capacitors and resistors. Once the bandwidth has been designed which in most cases is a few kHz (to not be affected by any abrupt transient), it uses information from the gain modulator to adjust the PWM control that controls whether the power MOSFET is switched on or off.

The gain modulator and the voltage control loop[2] work together to sample the input current and output voltage,[3] respectively. These two measurements are taken and than compared against each other to determine if a gain should be applied to the input of the current control. This decision is than compared against a sample of the output current to determine the duty cycle of the PWM.

The PWM control uses trailing-edge modulation as shown in Figure 14.

[1]The bandwidth is set by Fswitching/6

[2]The voltage control loop also needs to be bandwidth limited, Again, this is designed using external passive components.

[3]The output voltage of a continuous inductor current boost regulator has to be set above the maximum peak of the input voltage in order to function correctly as a PFC. The output should be 1.414 times the maximum input voltage.

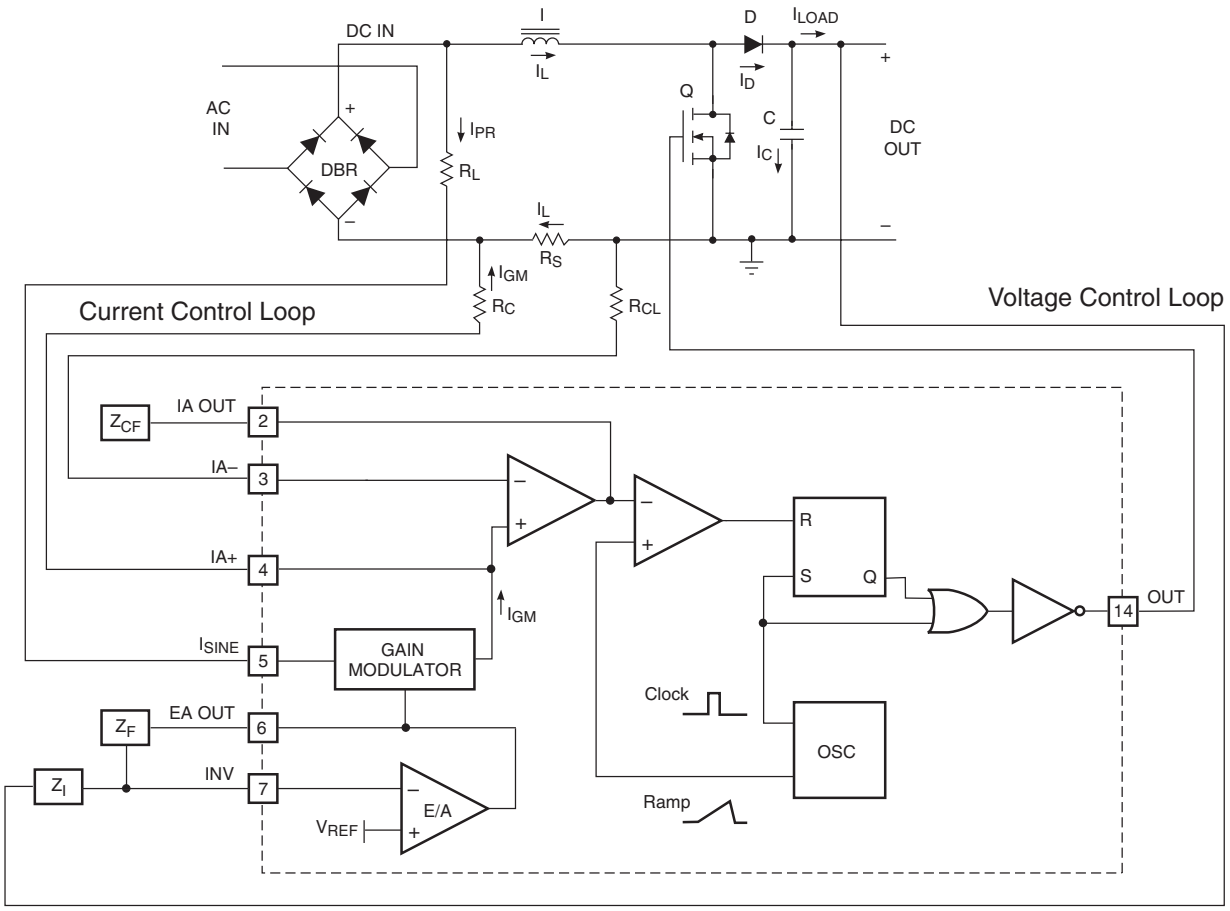

Figure 13. Example of an Average Current Mode PFC Control (ML4821)

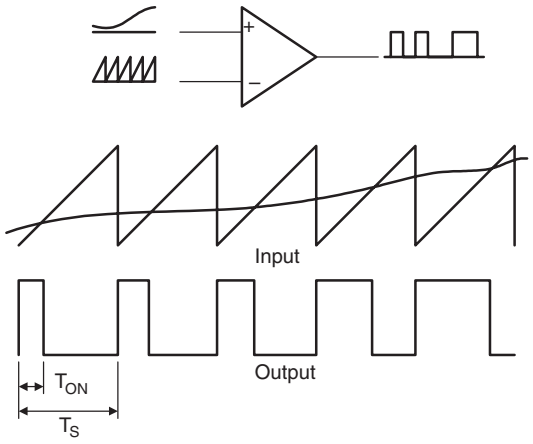

Figure 14. Trailing-Edge Modulation[4]

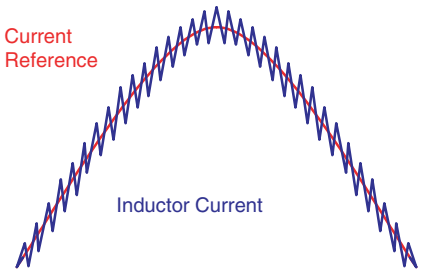

Figure 15. Typical Average Current Mode Waveform

[4] Trailing edge modulation is when the output switches on when the output of the comparator passes through the trailing edge of the sawtooth wave created.

The line that goes through the saw tooth waveform is the output of the differential amplifier within the current loop control. The output of the differential amplifier (located on the top of Figure 13) goes into an R-S flip flop that controls the power MOSFET. The average current mode waveform is shown in Figure 14. Figure 15 shows the waveform of what a typical average current PFC device looks like.

Continuous Mode:

Input Current Shaping

Fairchild's FAN4803 features input current shaping, another control method of the continuous current mode PFC. Figure 16 shows the internal PFC block of the FAN4803. Unlike the conventional/typical average current mode PFC controller, the FAN4803 does not need input voltage information and a multiplier. It changes the slope of an internal ramp according to the error amplifier output voltage, while the current sense information and the ramp signal are used to determine the turn-on time. As shown in Figure 17a, the switch is turned on when the current sense voltage meets the internal ramp signal and the switch is turned off by the internal clock signal. To control the output voltage, the slope of the internal ramp signal is adjusted. By comparing Figure 17a and Figure 17b, one can see that the average current increases if the slope increases and decreases if the slope decreases.

Using the continuous mode characteristic, the following equations show that the inductor current is proportional to the sinusoidal waveform at the turn-on time. Therefore the inductor current minimum value during one switching cycle follows the sinusoidal current reference as shown in Figure 18. However, the inductor current peak value during one switching cycle is not controlled to follow the sinusoidal reference. Therefore the average inductor current might not be sinusoidal. To make the average inductor current close to the sinusoidal reference, the inductance has to be high enough to make the current ripple small.

$$V_L = V_{IN} = L\frac{di_L}{t_{on}} \quad \text{: During on-time}$$

$$V_L = (V_{IN} - V_{OUT}) = L\frac{di_L}{t_{off}} \quad \text{: During off-time}$$

$$V_{IN} \bullet t_{on} = (V_{OUT} - V_{IN}) \bullet t_{off},\ \frac{t_{off}}{T_S} = \frac{V_{IN}}{V_{OUT}} \quad \text{: CCM condition}$$

$$V_{CS} = Vramp = Veao\frac{t_{off}}{T_S} = Veao\frac{V_{IN}}{V_{OUT}} \quad \text{: Switch off to on instant}$$

$$Rs \bullet i_L(t_O + t_{off}) = \frac{Veao}{V_{OUT}} V_{IN} \bullet \sin(\omega t)$$

$$\therefore I_{L(\min)} = i_L(t_O + t_{off}) \propto \sin(\omega t)$$

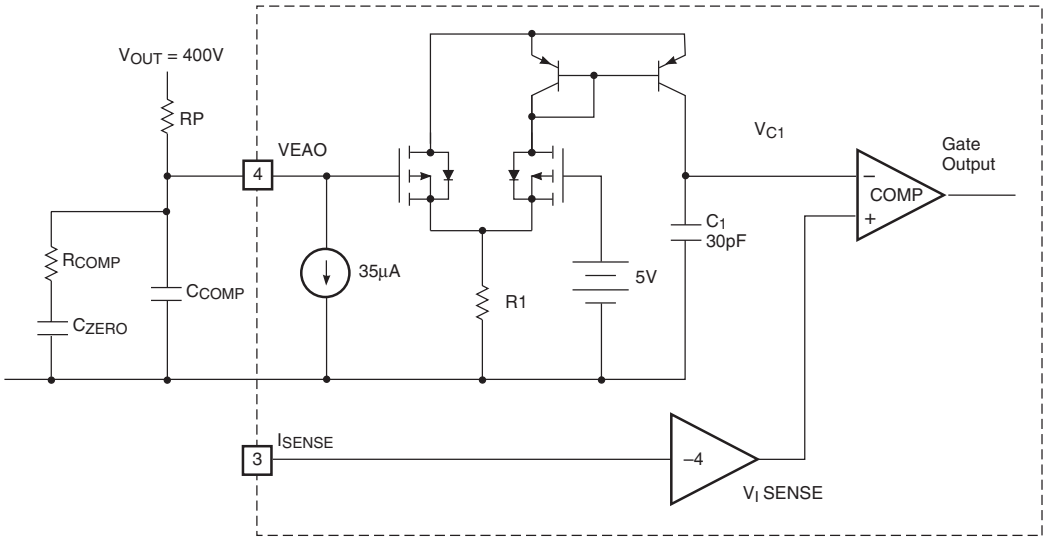

Figure 16. Example of the Input Current Shaping PFC Controller (FAN4803

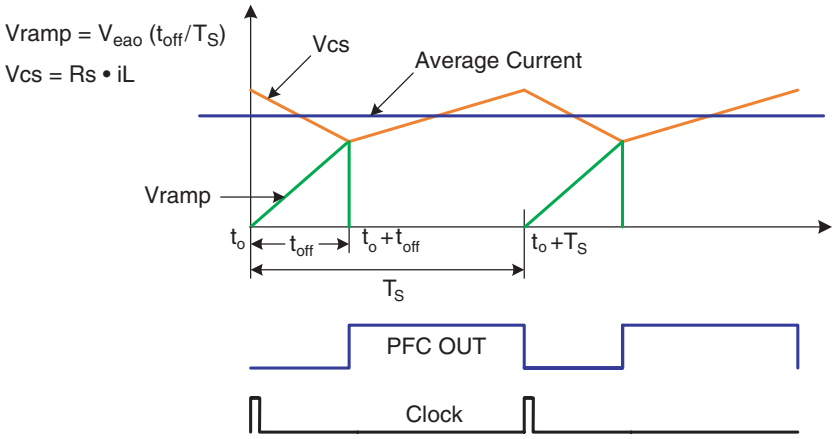

Figure 17a. Typical Input Current Shaping PFC Waveform

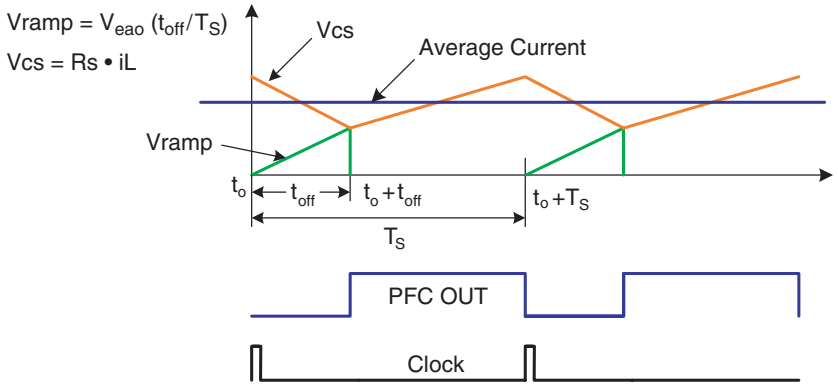

Figure 17b. Typical Input Current Shaping PFC Waveform

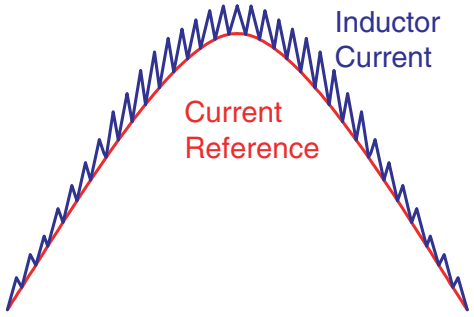

Figure 18. Input Current Shaping PFC Waveform

Leading Edge Modulation/Trailing Edge Modulation (LEM/TEM) versus Trailing Edge Modulation/Trailing Edge Modulation (TEM/TEM)

Leading edge/trailing edge modulation is a patented Fairchild technique to synchronize the PFC controller to the PWM controller. Typically TEM/TEM is used in PFC/PWM controllers which results in an additional step as well as a larger PFC bulk capacitor (as shown below).

Trailing Edge Modulation/Trailing Edge Modulation (TEM/TEM)

Figure 19a shows the PFC inductor being energized.

Figure 19b shows the energy from the inductor being transferred into the PFC bulk capacitor.

When the PWM switch is closed, as shown in Figure 19c, the energy stored within the PFC bulk capacitor is used to drive the load. Every time this cycle is repeated, the PFC bulk capacitor has to be fully charged since it is fully discharged when the PWM switch is closed.

Fairchild Patented Leading Edge Modulation/ Trailing Edge Modulation (LEM/TEM) Technique

In LET/TEM the PFC and PWM switches are tied together, but opening and closing 180 degrees out of phase, so when the PFC switch is open the PWM switch is closed and vice versa. Initially when the PFC switch is closed, the PFC inductor is energized, once the PWM switch is closed, both the output and the PFC bulk capacitor are energized. Figures 20a and 20b show that upon repetition of this cycle, the PFC bulk capacitor does not have to be that large because it is not powering the output all by itself, the PFC inductor is helping out as well.

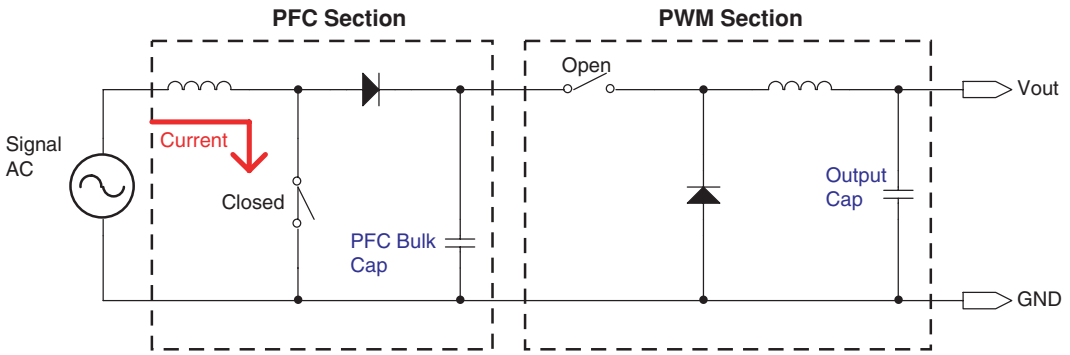

Figure 19a. Energizing the PFC Inductor

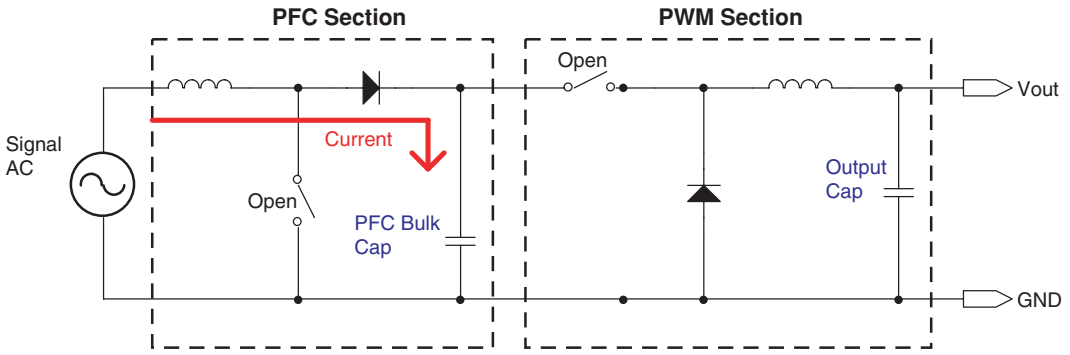

Figure 19b. Charging the PFC Bulk Capacitor

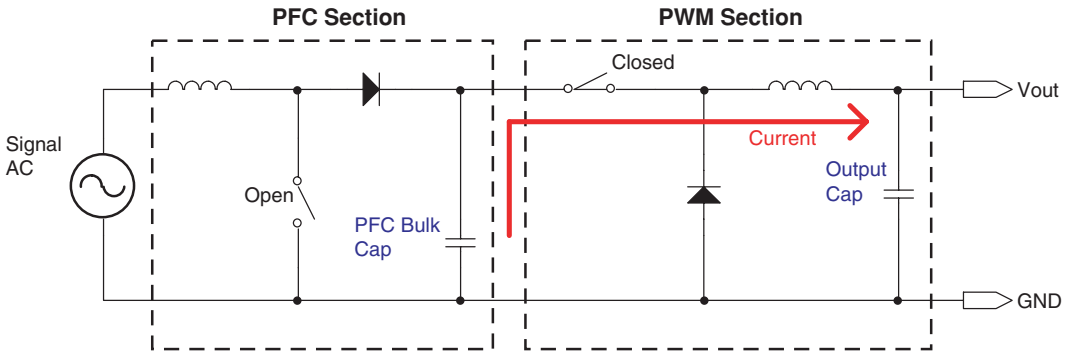

Figure 19c. Powering the Output

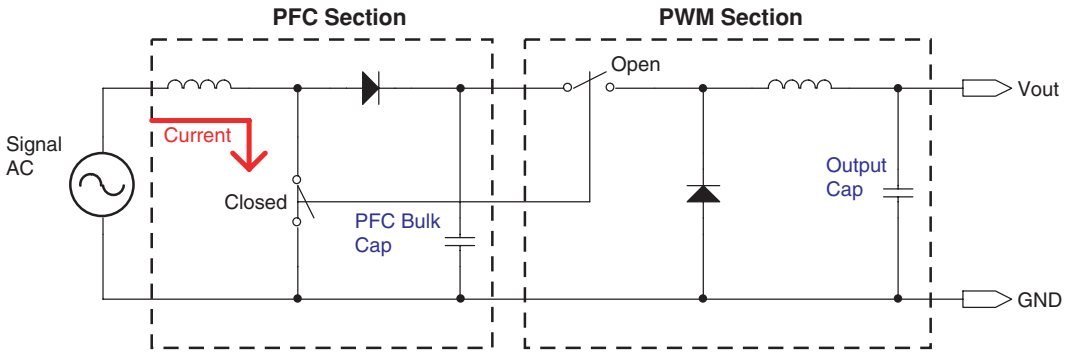

Figure 20a. Energizing the PFC Inductor

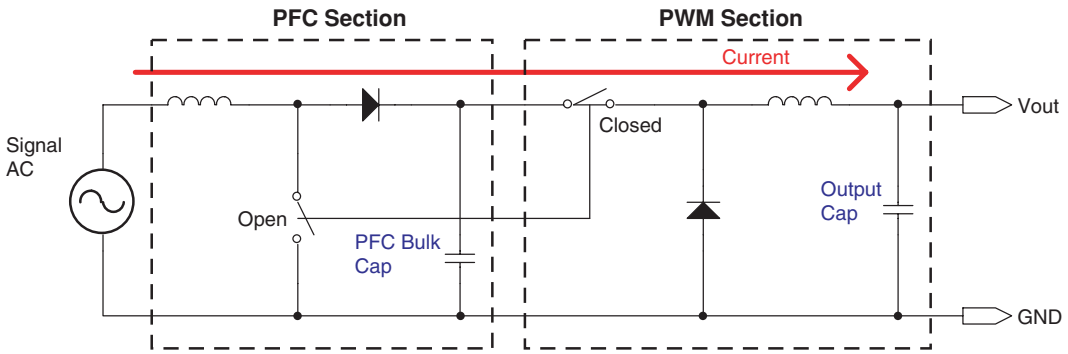

Figure 20b. Charging the PFC Bulk Capacitor and Powering the Output

Conclusion

Power companies do not get excited over low power factor driven devices, plus the extra cost of unused or wasted power can be quite large. This is why PFC on the device side has become an important part of the final power system design for so many products. There are many standards in place (example, EN 61000-3-2) to drive power consumption to a power factor of 1 and keep total harmonic distortion to a minimum. Depending on the output power and the designer's needs, a SMPS can be designed with either a discontinuous or continuous mode stand alone PFC controller, or a continuous PFC/PWM mode device can be used. PFC controllers are forecasted to grow to $175 million in 2006, and standards are reducing the minimum power limits on systems that require PFC, more and more PFC controllers will be used.