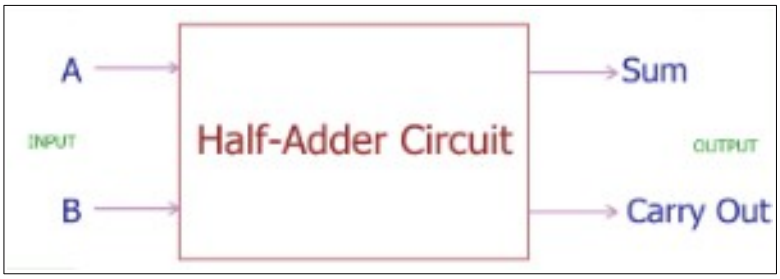
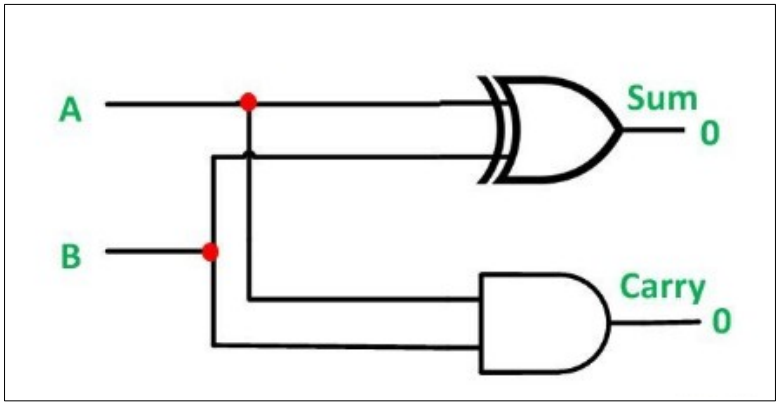
100 Days of RTL Challenge-Day 1

Half Adder:

Half adder is the simplest of all adder circuits. Half adder is a combinational arithmetic circuit that adds two numbers and produces a sum bit (s) and carry bit (c) both as output. The addition of 2 bits is done using a combination circuit called a Half adder. The input variables are augend and addend bits and output variables are sum & carry bits. A and B are the two input bits.





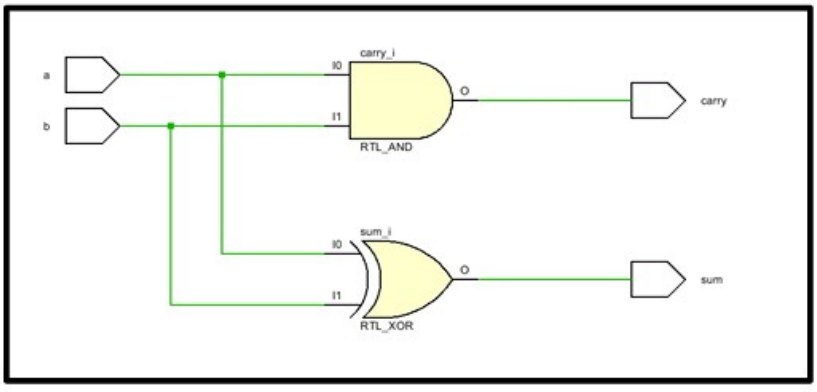
RTL Code:

```
module adder(a, b, sum, carry);
input a, b;
output sum, carry;
assign sum = a^b;
assign carry = a&b;
endmodule
```

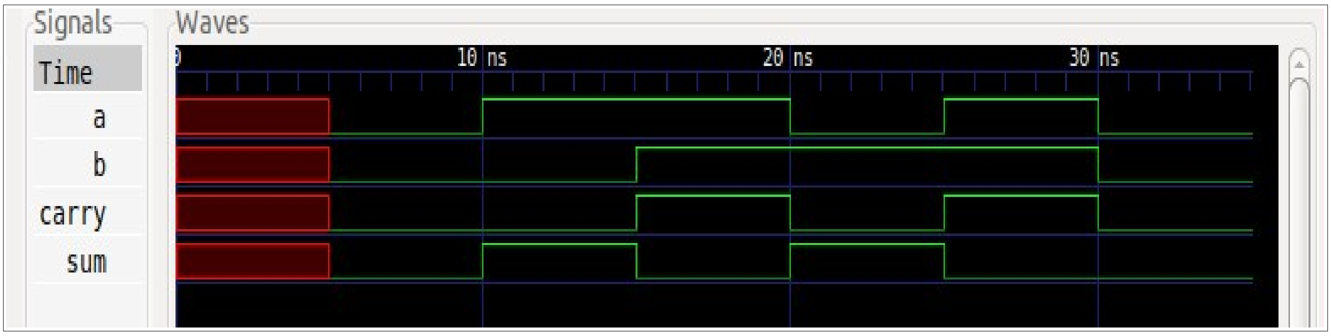
TestBench:

```
`timescale 1ns/1ns

module adder_test;

    reg a, b;

    wire sum, carry;

    adder DUT(.a(a), .b(b), .sum(sum), .carry(carry));

    initial begin
        $dumpfile("adder.vcd");
        $dumpvars(0, adder_test);
        $monitor($time, "  a = %b, b = %b, sum = %b, carry = %b", a, b, sum, carry);

        #5 a = 0; b = 0;  // 00 -> 0 sum, 0 carry
        #5 a = 1; b = 0;  // 01 -> 1 sum, 0 carry
        #5 a = 1; b = 1;  // 11 -> 0 sum, 1 carry
        #5 a = 0; b = 1;  // 10 -> 1 sum, 0 carry
        #5 a = 1; b = 1;  // 11 -> 0 sum, 1 carry
        #5 a = 0; b = 0;  // 00 -> 0 sum, 0 carry
        #5 $finish;
    end

endmodule
```

Schematic:



Simulation Result:



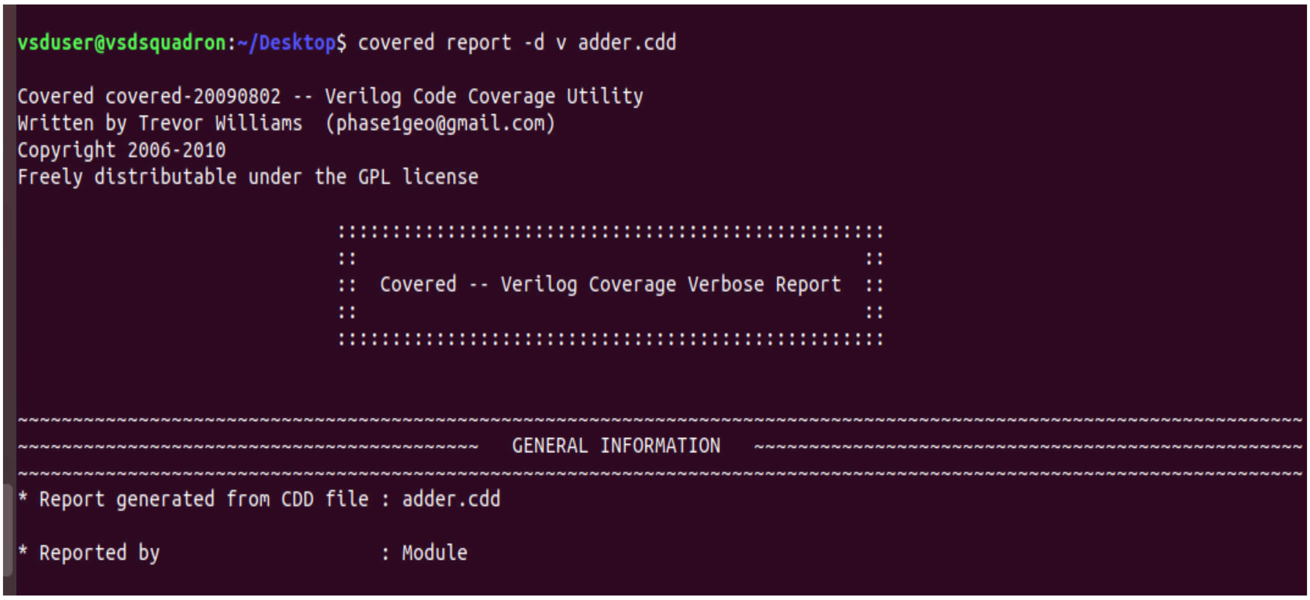
Code Coverage Report :

Code coverage is analyzed using the tool “covered”. It is using to evaluate the Code coverage of the Testbench i.e, how efficiently the alll test cases all analyzed.
It reports Line Coverage, Toggle Coverage, Combinational Logic Coverage and Finite State Machine Coverage
Code coverage is evaluated using the following command(in Linux).

covered score -t adder_test -v adder_test.v -v adder.v -vcd adder.vcd -o adder.cdd

To view the report, run the command as follows:

covered report -d v adder.cdd



```
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~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~   LINE COVERAGE RESULTS   ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
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Module/Task/Function      Filename                 Hit/ Miss/Total    Percent hit
------------------------------------------------------------------------------------------------------------------------------
  $root                   NA                         0/    0/    0      100%
  adder_test              adder_test.v              12/    0/   12      100%
  adder                   adder.v                    2/    0/    2      100%
------------------------------------------------------------------------------------------------------------------------------
  Accumulated                                       14/    0/   14      100%


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~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~   TOGGLE COVERAGE RESULTS   ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
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                                                         Toggle 0 -> 1                        Toggle 1 -> 0
Module/Task/Function      Filename                 Hit/ Miss/Total    Percent hit      Hit/ Miss/Total    Percent hit
------------------------------------------------------------------------------------------------------------------------------
  $root                   NA                         0/    0/    0      100%             0/    0/    0      100%
  adder_test              adder_test.v               4/    0/    4      100%             4/    0/    4      100%
  adder                   adder.v                    4/    0/    4      100%             4/    0/    4      100%
------------------------------------------------------------------------------------------------------------------------------
  Accumulated                                        8/    0/    8      100%             8/    0/    8      100%

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~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~   COMBINATIONAL LOGIC COVERAGE RESULTS   ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
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                                                                            Logic Combinations
Module/Task/Function              Filename                              Hit/Miss/Total    Percent hit
------------------------------------------------------------------------------------------------------------------------------
  $root                           NA                                      0/   0/   0      100%
  adder_test                      adder_test.v                            0/   0/   0      100%
  adder                           adder.v                                 7/   0/   7      100%
------------------------------------------------------------------------------------------------------------------------------
  Accumulated                                                             7/   0/   7      100%


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~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~   FINITE STATE MACHINE COVERAGE RESULTS   ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
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                                                             State                              Arc
Module/Task/Function      Filename                Hit/Miss/Total    Percent Hit     Hit/Miss/Total    Percent hit
------------------------------------------------------------------------------------------------------------------------------
  $root                   NA                        0/   0/   0      100%             0/   0/   0      100%
  adder_test              adder_test.v              0/   0/   0      100%             0/   0/   0      100%
  adder                   adder.v                   0/   0/   0      100%             0/   0/   0      100%
------------------------------------------------------------------------------------------------------------------------------
  Accumulated                                       0/   0/   0      100%             0/   0/   0      100%
```