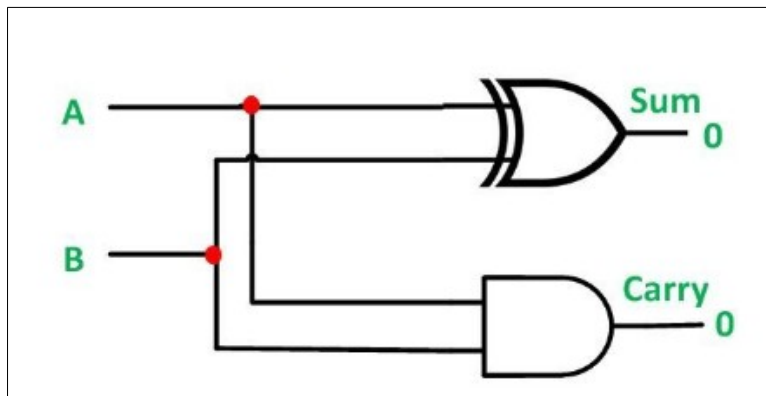


Half Adder:

Half adder is the simplest of all adder circuits. Half adder is a combinational arithmetic circuit that adds two numbers and produces a sum bit (s) and carry bit (c) both as output. The addition of 2 bits is done using a combination circuit called a Half adder. The input variables are augend and addend bits and output variables are sum & carry bits. A and B are the two input bits.



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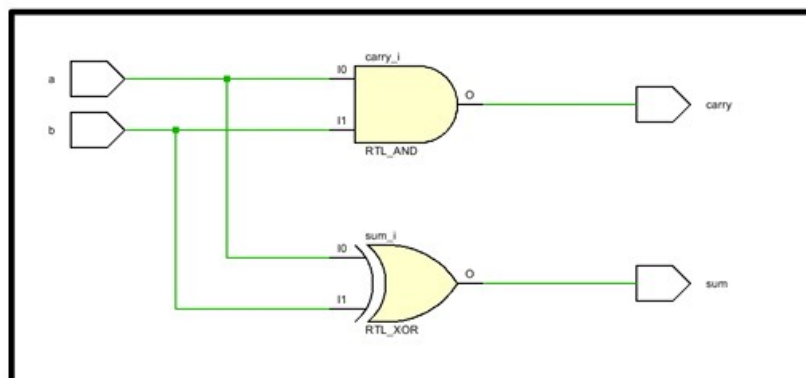
RTL Code:

```
1 module adder(a, b, sum, carry);
2   input a, b;
3   output sum, carry;
4   assign sum = a^b;
5   assign carry = a&b;
6 endmodule
```

TestBench:

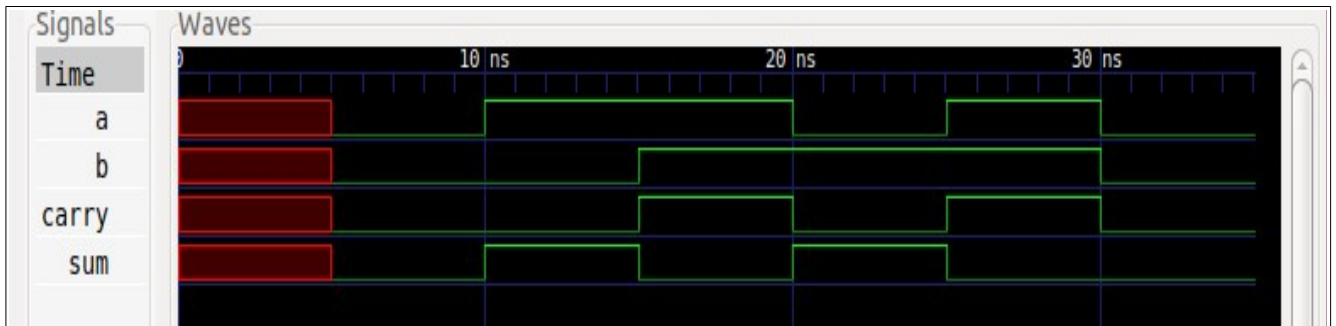
```
1 `timescale 1ns/1ns
2
3 module adder_test;
4
5     reg a, b;
6
7     wire sum, carry;
8
9     adder DUT(.a(a), .b(b), .sum(sum), .carry(carry));
10
11     initial begin
12         $dumpfile("adder.vcd");
13         $dumpvars(0, adder_test);
14         $monitor($time, " a = %b, b = %b, sum = %b, carry = %b", a, b, sum, carry);
15
16         #5 a = 0; b = 0; // 00 -> 0 sum, 0 carry
17         #5 a = 1; b = 0; // 01 -> 1 sum, 0 carry
18         #5 a = 1; b = 1; // 11 -> 0 sum, 1 carry
19         #5 a = 0; b = 1; // 10 -> 1 sum, 0 carry
20         #5 a = 1; b = 1; // 11 -> 0 sum, 1 carry
21         #5 a = 0; b = 0; // 00 -> 0 sum, 0 carry
22         #5 $finish;
23     end
24
25 endmodule
```

Schematic:



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Simulation Result:



Code Coverage Report :

Code coverage is analyzed using the tool “covered”. It is using to evaluate the Code coverage of the Testbench i.e, how efficiently the all test cases all analyzed.

It reports Line Coverage, Toggle Coverage, Combinational Logic Coverage and Finite State Machine Coverage

Code coverage is evaluated using the following command(in Linux).

```
covered score -t adder_test -v adder_test.v -v adder.v -vcd adder.vcd -o adder.cdd
```

To view the report, run the command as follows:

```
covered report -d v adder.cdd
```

```
vsduser@vsdsquadron:~/Desktop$ covered report -d v adder.cdd

Covered covered-20090802 -- Verilog Code Coverage Utility
Written by Trevor Williams (phase1geo@gmail.com)
Copyright 2006-2010
Freely distributable under the GPL license

:::
::
:: Covered -- Verilog Coverage Verbose Report
::
:::

----- GENERAL INFORMATION -----
* Report generated from CDD file : adder.cdd
* Reported by : Module
```

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LINE COVERAGE RESULTS									
Module/Task/Function	Filename	Hit/ Miss/Total			Percent hit				
\$root	NA	0/	0/	0	100%				
adder_test	adder_test.v	12/	0/	12	100%				
adder	adder.v	2/	0/	2	100%				
Accumulated		14/	0/	14	100%				
TOGGLE COVERAGE RESULTS									
Module/Task/Function	Filename	Toggle 0 -> 1				Toggle 1 -> 0			
		Hit/	Miss/	Total	Percent hit	Hit/	Miss/	Total	Percent hit
\$root	NA	0/	0/	0	100%	0/	0/	0	100%
adder_test	adder_test.v	4/	0/	4	100%	4/	0/	4	100%
adder	adder.v	4/	0/	4	100%	4/	0/	4	100%
Accumulated		8/	0/	8	100%	8/	0/	8	100%
COMBINATIONAL LOGIC COVERAGE RESULTS									
Module/Task/Function	Filename	Logic Combinations							
		Hit/Miss/Total	Percent hit						
\$root	NA	0/	0/	0	100%				
adder_test	adder_test.v	0/	0/	0	100%				
adder	adder.v	7/	0/	7	100%				
Accumulated		7/	0/	7	100%				
FINITE STATE MACHINE COVERAGE RESULTS									
Module/Task/Function	Filename	State				Arc			
		Hit/Miss/Total	Percent Hit			Hit/Miss/Total	Percent hit		
\$root	NA	0/	0/	0	100%	0/	0/	0	100%
adder_test	adder_test.v	0/	0/	0	100%	0/	0/	0	100%
adder	adder.v	0/	0/	0	100%	0/	0/	0	100%
Accumulated		0/	0/	0	100%	0/	0/	0	100%