CD4048BMS

CMOS Multifunction Expandable 8 Input Gate

December 1992

Features

- **High-Voltage Type (20V Rating)**
- **Three State Output**
- **Many Logic Functions Available in One Package**
- **Standardize, Symmetrical Output Characteristics**
- **100% Tested for Quiescent Current at 20V**
- **Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C**
- **Noise Margin (Over Full Package Temperature Range):**
  - **1V at VDD = 5V**
  - **2V at VDD = 10V**
  - **2.5V at VDD = 15V**
- **5V, 10V and 15V Parametric Ratings**
- **Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications

- **Selection of Up to 8 Logic Functions**
- **Digital Control of Logic**
- **General Purpose Gating Logic**
  - **Decoding**
  - **Encoding**

Description

CD4048BMS is an 8-input gate having four control inputs. Three binary control inputs - Ka, Kb, and Kc - provide the implementation of eight different logic functions. These functions are OR, NOR, AND, NAND, OR/AND, OR/NAND, AND/OR and AND/NOR.

A fourth control input, Kd, provides the user with a 3-state output. When control input Kd is high, the output is either a logic 1 or a logic 0 depending on the inner states. When control input Kd is low, the output is an open circuit. This feature enables the user to connect this device to a common bus line.

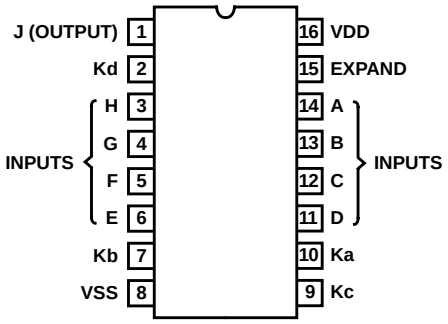
In addition to the eight input lines, an EXPAND input is provided that permits the user to increase the number of inputs into a CD4048BMS (see Figure 2). For example, two CD4048BMS's can be cascaded to provided a 16-input multifunction gate. When the EXPAND input is not used, it should be connected to VSS.

The CD4048BMS is supplied in these 16 lead outline packages:

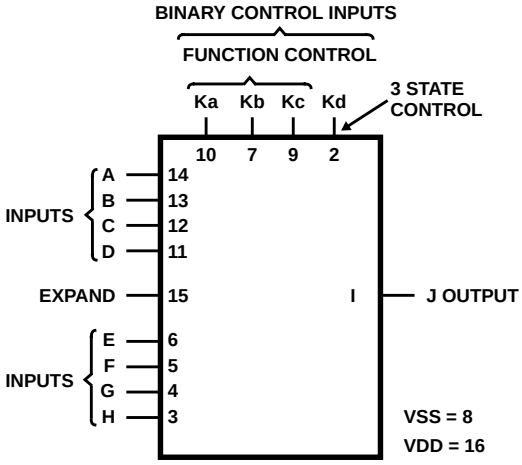
Braze Seal DIP	H4S
Frit Seal DIP	H1E
Ceramic Flatpack	H6W

Pinout

CD4048BMS
TOP VIEW



Functional Diagram



Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) . . . . . -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs . . . . . -0.5V to VDD +0.5V
DC Input Current, Any One Input . . . . . ±10mA
Operating Temperature Range . . . . . -55^oC to $+125^oC$
Package Types D, F, K, H
Storage Temperature Range (TSTG) . . . . . -65^oC to $+150^oC$
Lead Temperature (During Soldering) . . . . . $+265^oC$
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	$80^oC/W$	$20^oC/W$
Flatpack Package	$70^oC/W$	$20^oC/W$

Maximum Package Power Dissipation (PD) at $+125^oC$
For TA = -55^oC to $+100^oC$ (Package Type D, F, K) 500mW
For TA = $+100^oC$ to $+125^oC$ (Package Type D, F, K) . . . . . Derate Linearity at $12mW/^oC$ to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature . . . . . $+175^oC$

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	$+25^oC$	-	0.5	µA
				2	$+125^oC$	-	50	µA
		VDD = 18V, VIN = VDD or GND		3	-55^oC	-	0.5	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	$+25^oC$	-100	-	nA
				2	$+125^oC$	-1000	-	nA
			VDD = 18V	3	-55^oC	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	$+25^oC$	-	100	nA
				2	$+125^oC$	-	1000	nA
			VDD = 18V	3	-55^oC	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	$+25^oC$	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	$+25^oC$	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	$+25^oC$	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	$+25^oC$	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	$+25^oC$	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	$+25^oC$	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	$+25^oC$	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	$+25^oC$	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	$+25^oC$	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	$+25^oC$	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	$+25^oC$			
		VDD = 18V, VIN = VDD or GND		8A	$+125^oC$			
		VDD = 3V, VIN = VDD or GND		8B	-55^oC			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	11	-	V
Tri-State Output Leakage	IOZL	VIN = VDD or GND VOUT = 0V	VDD = 20V	1	$+25^oC$	-0.4	-	µA
				2	$+125^oC$	-12	-	µA
			VDD = 18V	3	-55^oC	-0.4	-	µA
Tri-State Output Leakage	IOZH	VIN = VDD or GND VOUT = VDD	VDD = 20V	1	$+25^oC$	-	0.4	µA
				2	$+125^oC$	-	12	µA
			VDD = 18V	3	-55^oC	-	0.4	µA

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Ka to Output	TPHL TPLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	600	ns
			10, 11	+125°C, -55°C	-	810	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.25	µA
				+125°C	-	7.5	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.5	µA
				+125°C	-	15	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.5	µA
				+125°C	-	30	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	7	-	V
Propagation Delay Ka to Output	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	300	ns
		VDD = 15V	1, 2, 3	+25°C	-	240	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Inputs to Output	TPHL2 TPLH2	VDD = 5V	1, 2, 3	+25°C	-	600	ns
		VDD = 10V	1, 2, 3	+25°C	-	300	ns
		VDD = 15V	1, 2, 3	+25°C	-	240	ns
Propagation Delay Kb to Output	TPHL3 TPLH3	VDD = 5V	1, 2, 3	+25°C	-	450	ns
		VDD = 10V	1, 2, 3	+25°C	-	170	ns
		VDD = 15V	1, 2, 3	+25°C	-	110	ns
Propagation Delay Kc to Output	TPHL4 TPLH4	VDD = 5V	1, 2, 3	+25°C	-	280	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Propagation Delay Expand Input to Output	TPHL5 TPLH5	VDD = 5V	1, 2, 3	+25°C	-	380	ns
		VDD = 10V	1, 2, 3	+25°C	-	180	ns
		VDD = 15V	1, 2, 3	+25°C	-	130	ns
Propagation Delay 3 State Kd to Output	TPHZ, LZ TPZH, ZL	VDD = 5V	1, 2, 4	+25°C	-	160	ns
		VDD = 10V	1, 2, 4	+25°C	-	70	ns
		VDD = 15V	1, 2, 4	+25°C	-	50	ns
Transition Time	TTLH TTHL	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7	pF
3 State Output Capacitance	CO		1, 2	+25°C	-	10	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. CL = 50pF, RL = 1K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25^{O}C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - SSI	IDD	±0.1µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	1	2 - 15	16			
Static Burn-In 2 Note 1	1	8	2 - 7, 9 - 16			
Dynamic Burn-In Note 1	-	8, 15	2, 16	1	9 - 14	3 - 7
Irradiation Note 2	1	8	2 - 7, 9 - 16			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagrams

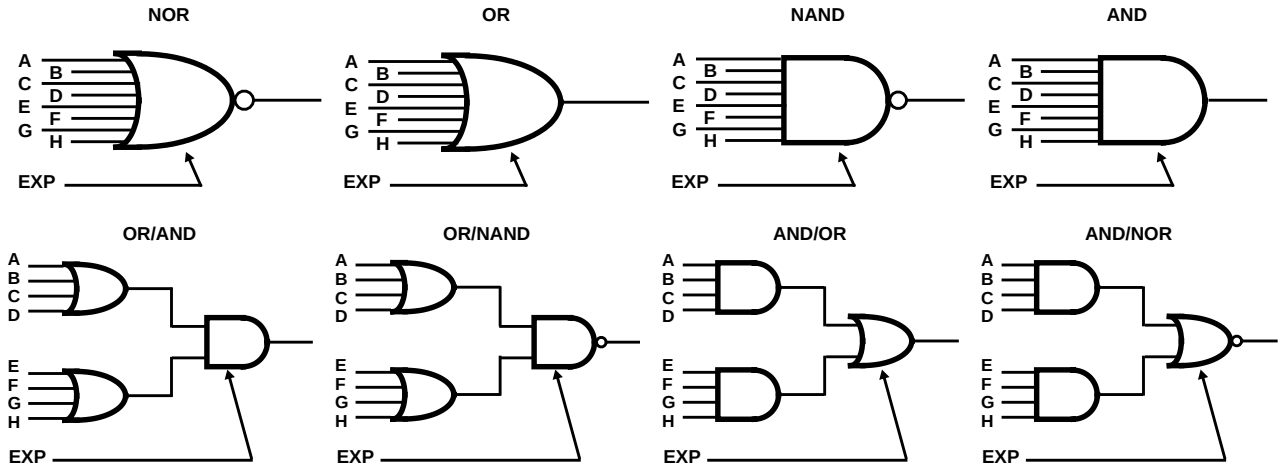


FIGURE 1. BASIC LOGIC CONFIGURATIONS

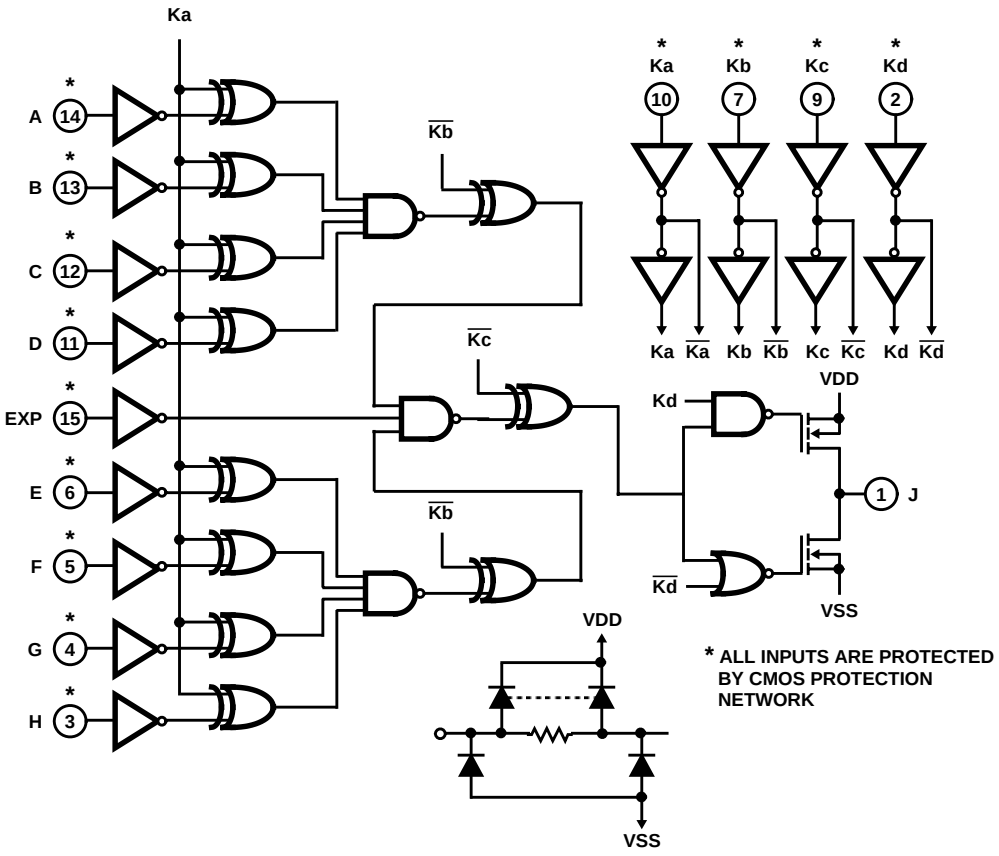


FIGURE 2. LOGIC DIAGRAM

Logic Diagrams (Continued)

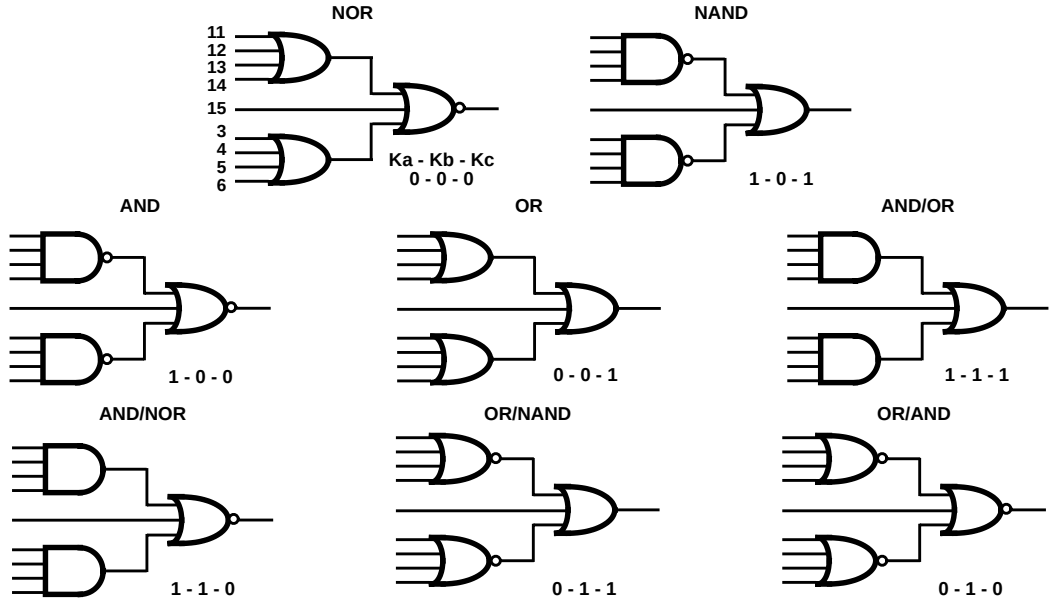
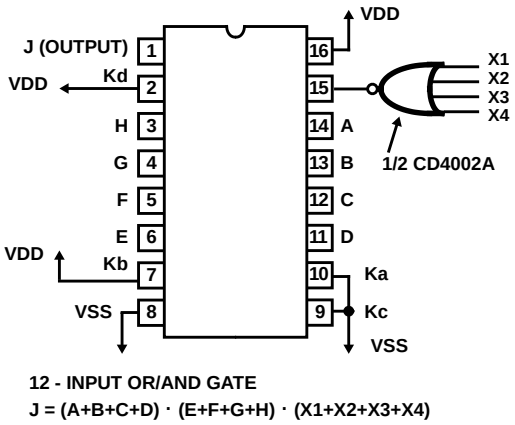


FIGURE 3. ACTUAL CIRCUIT LOGIC CONFIGURATIONS

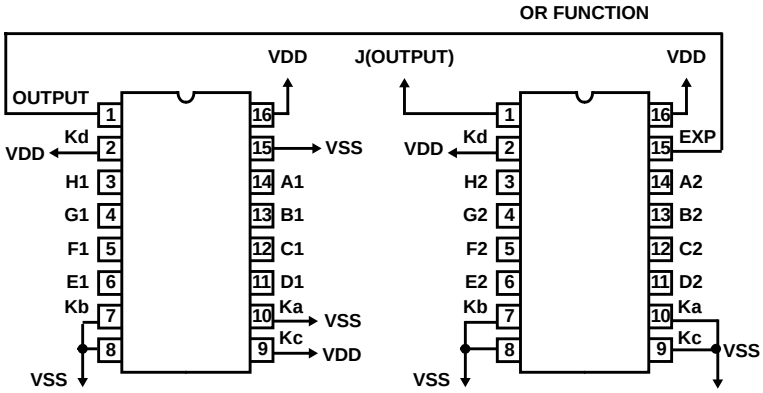
Applications of Expand Input



12 - INPUT OR/AND GATE

$J = (A+B+C+D) \cdot (E+F+G+H) \cdot (X1+X2+X3+X4)$

FIGURE 4. 12 INPUT OR/AND GATE



16 - INPUT NOR GATE

$J = \overline{A1 + B1 + C1 + D1 + E1 + F1 + G1 + H1 + A2 + B2 + C2 + D2 + E2 + F2 + G2 + H2}$

FIGURE 5. 16 INPUT NOR GATE

IMPLEMETATION OF EXPAND INPUT FOR 9 OR MORE INPUTS

OUTPUT FUNCTION	FUNCTION NEEDED AT EXPAND INPUT	OUTPUT BOOLEAN EXPRESSION
NOR	OR	$J=\overline{(A+B+C+D+E+F+G+H)+(EXP)}$
OR	OR	$J=(A+B+C+D+E+F+G+H)+(EXP)$
AND	NAND	$J=(ABCDEFGH)\bullet\overline{(EXP)}$
NAND	NAND	$J=\overline{(ABCDEFGH)\bullet\overline{(EXP)}}$
OR/AND	NOR	$J=(A+B+C+D)\bullet(E+F+G+H)\bullet\overline{(EXP)}$
OR/NAND	NOR	$J=\overline{(A+B+C+D)\bullet(E+F+G+H)\bullet\overline{(EXP)}}$
AND/NOR	AND	$J=\overline{(ABCD)+(EFGH)+(EXP)}$
AND/OR	AND	$J=(ABCD)+(EFGH)+(EXP)$

NOTES: 1. (EXP) designates the EXPAND function (i.e., X1 + X2 + . . .XN).

2. Refer to FUNCTION TRUTH TABLE for connection of unused inputs.

FUNCTION TRUTH TABLE

OUTPUT FUNCTION	BOOLEAN EXPRESSION	Ka	Kb	Kc	UNUSED INPUT*
NOR	$J=\overline{A+B+C+D+E+F+G+H}$	0	0	0	VSS
OR	J=A+B+C+D+E+F+G+H	0	0	1	VSS
OR/AND	J=(A+B+C+D)•(E+F+G+H)	0	1	0	VSS
OR/NAND	$J=\overline{(A+B+C+D)•(E+F+G+H)}$	0	1	1	VSS
AND	J=ABCDEFGH	1	0	0	VDD
NAND	$J=\overline{ABCDEFGH}$	1	0	1	VDD
AND/NOR	$J=\overline{ABCD+EFGH}$	1	1	0	VDD
AND/OR	J=ABCD+EFGH	1	1	1	VDD
Kd = 1 Normal Inverter Action Kd = 0 High Impedance Output					

EXPAND Input = 0

*See Figures 1, 2, 3, 4 and 5

Typical Performance Characteristics

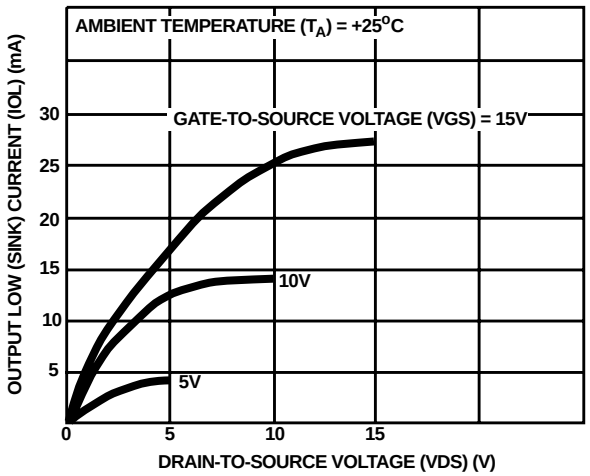


FIGURE 6. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

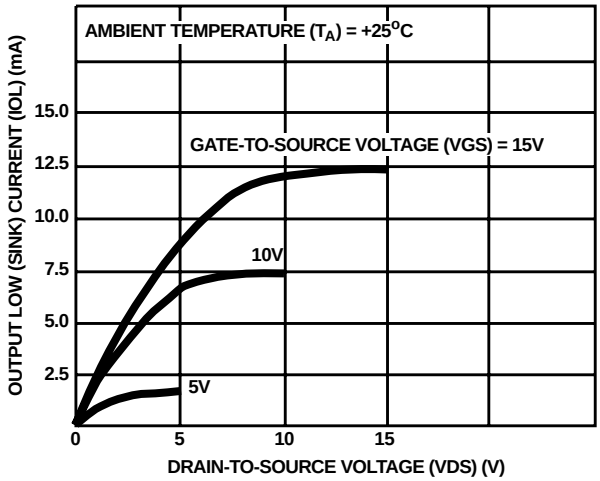


FIGURE 7. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

Typical Performance Characteristics (Continued)

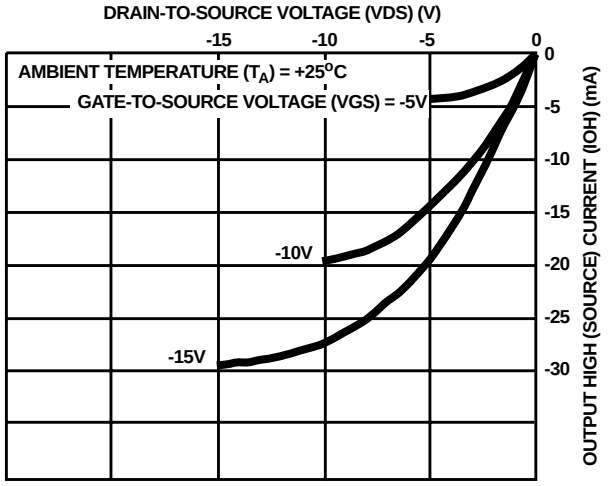


FIGURE 8. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

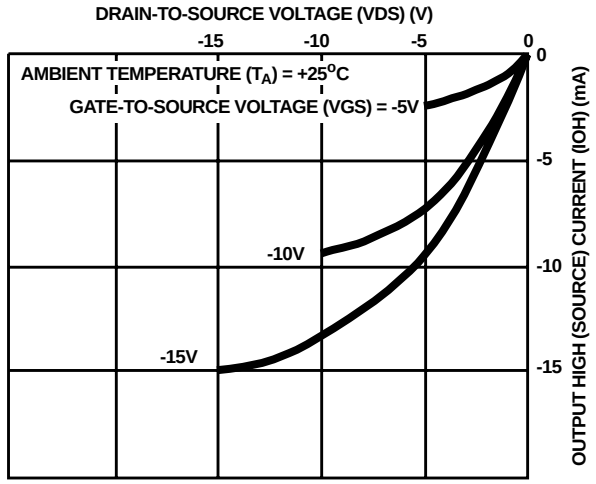


FIGURE 9. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

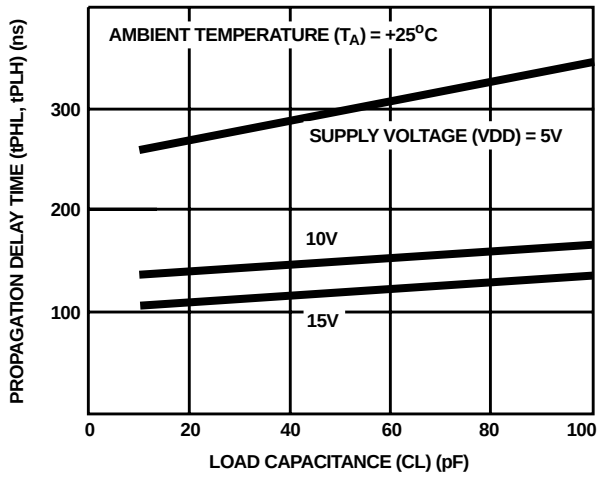


FIGURE 10. TYPICAL PROPAGATION DELAY TIME (LOGIC INPUTS TO OUTPUT) AS A FUNCTION OF LOAD CAPACITANCE

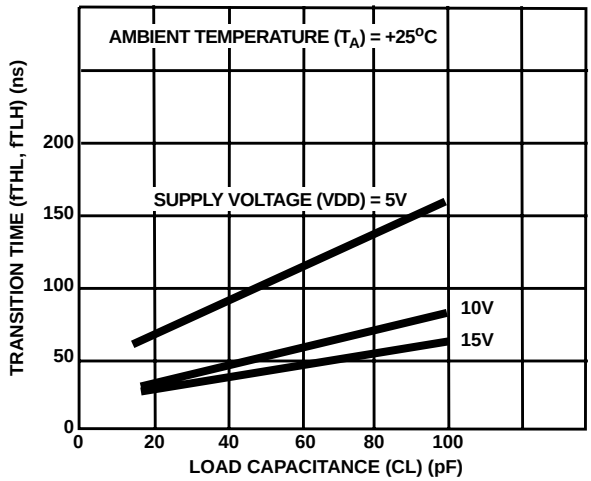


FIGURE 11. TYPICAL TRANSITION TIME vs LOAD CAPACITANCE

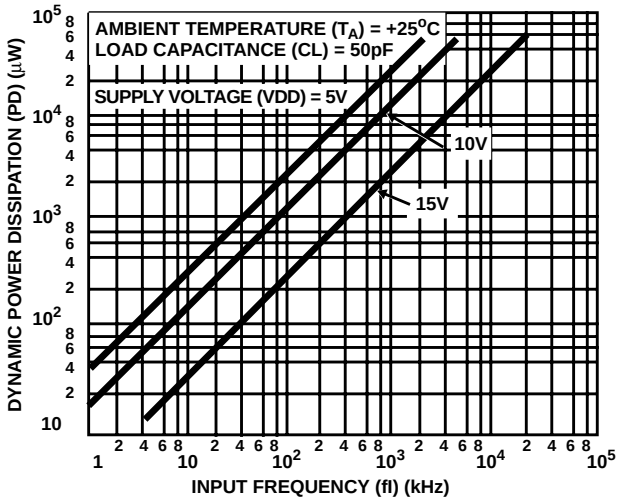


FIGURE 12. TYPICAL POWER DISSIPATION AS A FUNCTION OF INPUT FREQUENCY

Test Circuits and Wave Forms

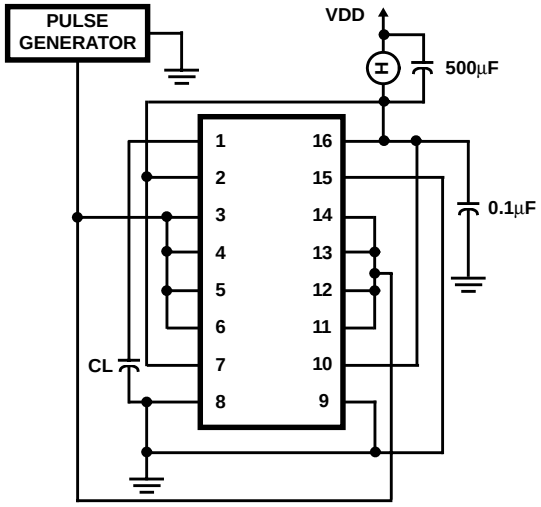


FIGURE 13. DYNAMIC POWER DISSIPATION TEST CIRCUIT

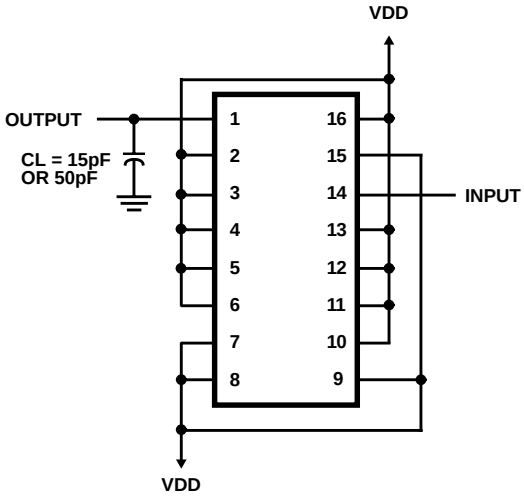


FIGURE 14. TEST CIRCUIT FOR tPHL, tTHL, AND tTHL (AND) MEASUREMENTS

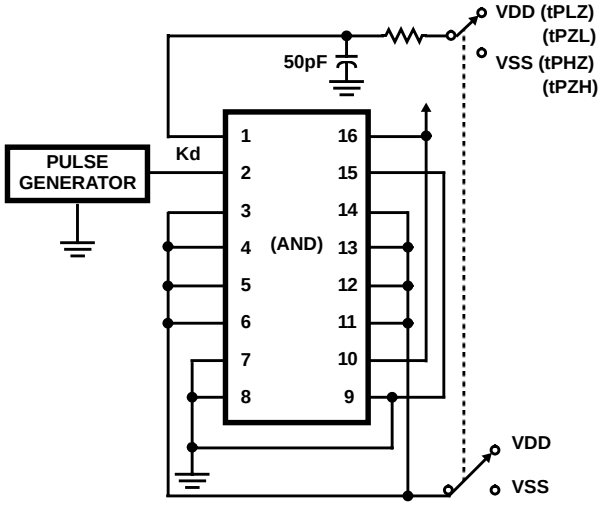


FIGURE 15. TEST CIRCUIT FOR tPZL, tPZH, tPLZ, AND tPHZ (AND)

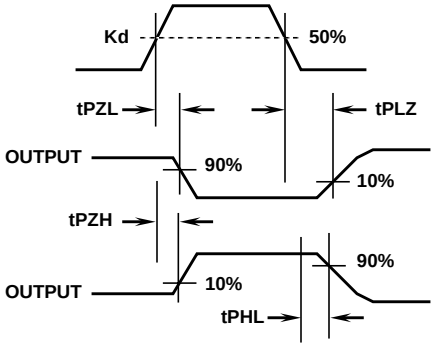


FIGURE 16. WAVEFORMS FOR tPZL, tPZH, tPLZ AND tPHZ (AND)

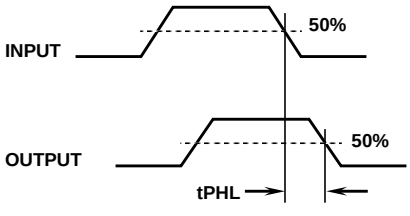


FIGURE 17. WAVEFORMS FOR tPHL AND tPHL (AND)

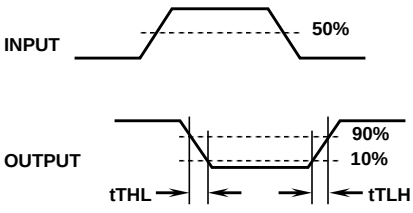
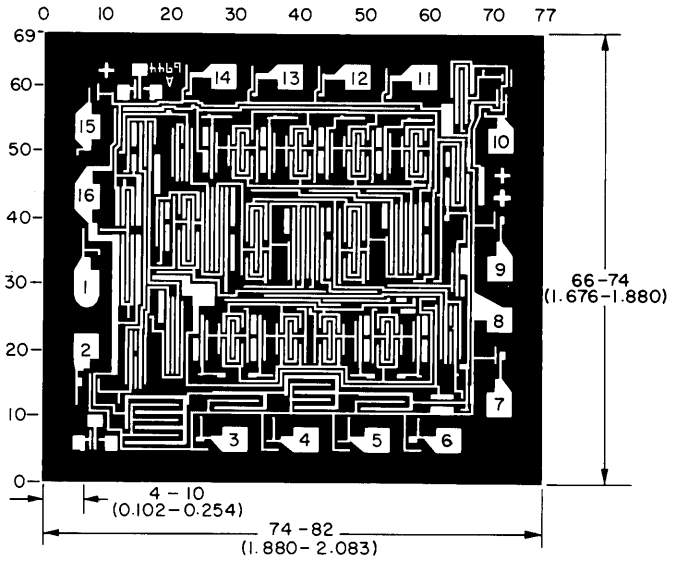


FIGURE 18. WAVEFORMS FOR tTHL AND tTLH (AND)

Chip Dimensions and Pad Layout



Dimensions in parentheses are in millimeters
and are derived from the basic inch dimensions
as indicated. Grid graduations are in mils (10^{-3} inch)

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

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