Circuits with Flip-Flop = Sequential Circuit

Circuit = State Diagram = State Table

State Minimization

Sequential Circuit Design

Example: Sequence Detector

Example: Binary Counter

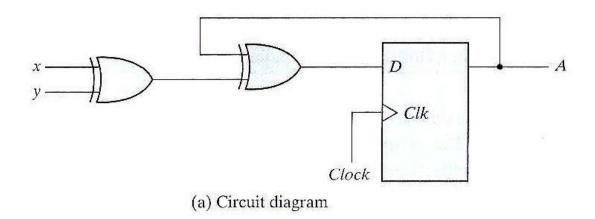
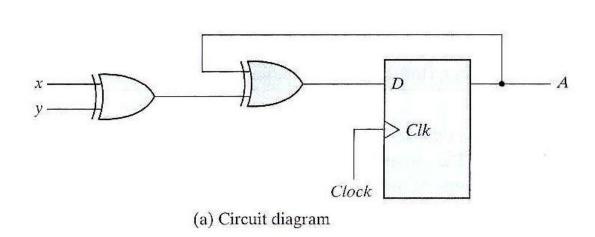


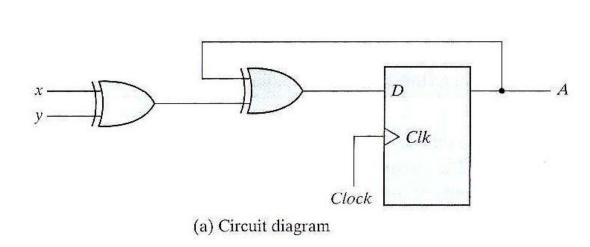
FIGURE 5.17
Sequential circuit with D flip-flop



state	Inp	uts	state
A	х	у	A
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

(b) State table

FIGURE 5.17
Sequential circuit with D flip-flop



Present state	Inp	uts	Next state
A	х	у	A
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

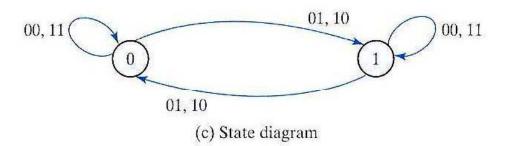
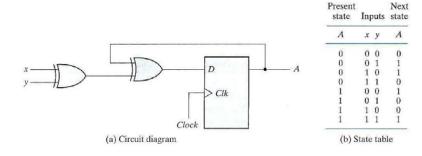


FIGURE 5.17
Sequential circuit with D flip-flop



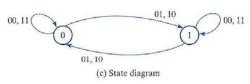


FIGURE 5.17
Sequential circuit with *D* flip-flop

Terms:

State: flip-flop output combination

Present state: before clock

Next state: after clock

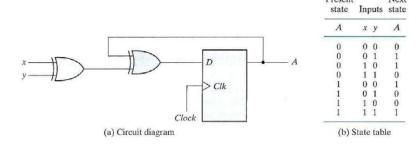
State transition <= clock

1 flip-flop => 2 states

2 flip-flops => 4 states

3 flip-flops => 8 states

4 flip-flops => 16 states



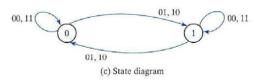
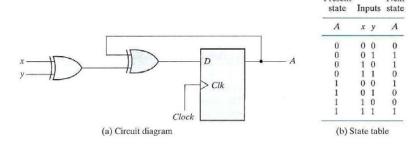


FIGURE 5.17
Sequential circuit with *D* flip-flop

Sequential circuit components:

Flip-flop(s)
Clock
Logic gates
Input
Output



State diagram:

Circle => state

Arrow => transition input/output

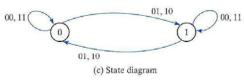
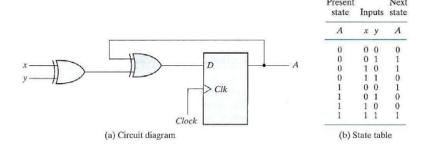


FIGURE 5.17
Sequential circuit with *D* flip-flop



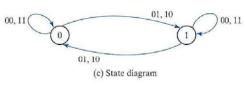


FIGURE 5.17 Sequential circuit with *D* flip-flop

State table:

Left column => current state

Top row => input combination

Table entry => next state, output

Example:

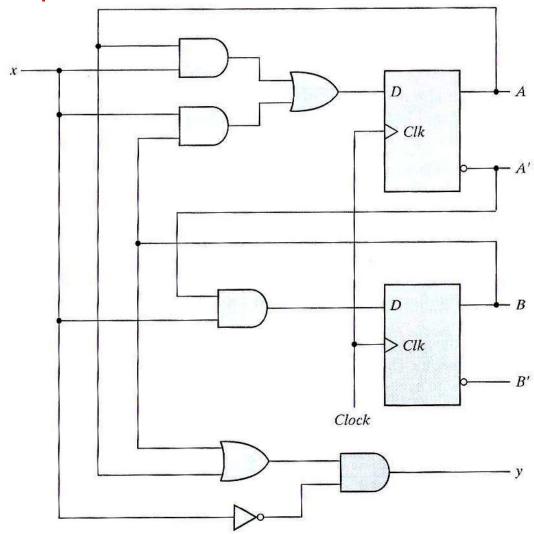


FIGURE 5.15
Example of sequential circuit

Example: Table 5.3
Second Form

Second Form of the State Table

Present		1	lext	Stat	Output		
	ate	x = 0		x =	vision (T		x = 1
A	В	A	В		В	y	y
0	0	0	0	0	1	0	0
0	1	0	0	1	1	1	0
1	0	0	0	1	0	1	0
1	1	0	0	1	0	1	O

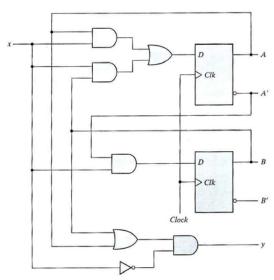


FIGURE 5.15
Example of sequential circuit

Example:

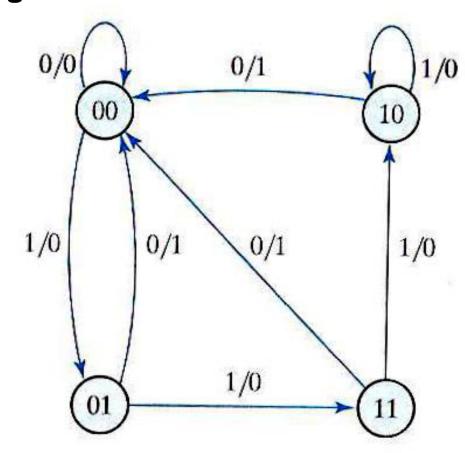
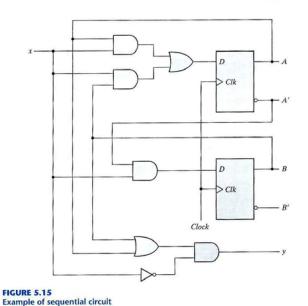


FIGURE 5.16
State diagram of the circuit of Fig. 5.15

Example:

Table 5.3Second Form of the State Table

Present		١		Stat	Output		
Sta	ate	x = 0 $x = 1$		x = 0	x = 1		
A	В	A	В	A	В	Y	y
0	0	0	0	0	1	0	0
0	1	0	0	1	1	1	0
1	0	0	0	1	0	1	O
1	1	0	0	1	0	1	0



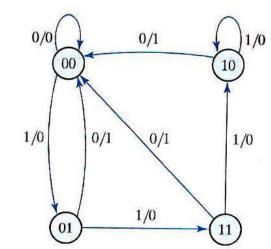


FIGURE 5.16 State diagram of the circuit of Fig. 5.15

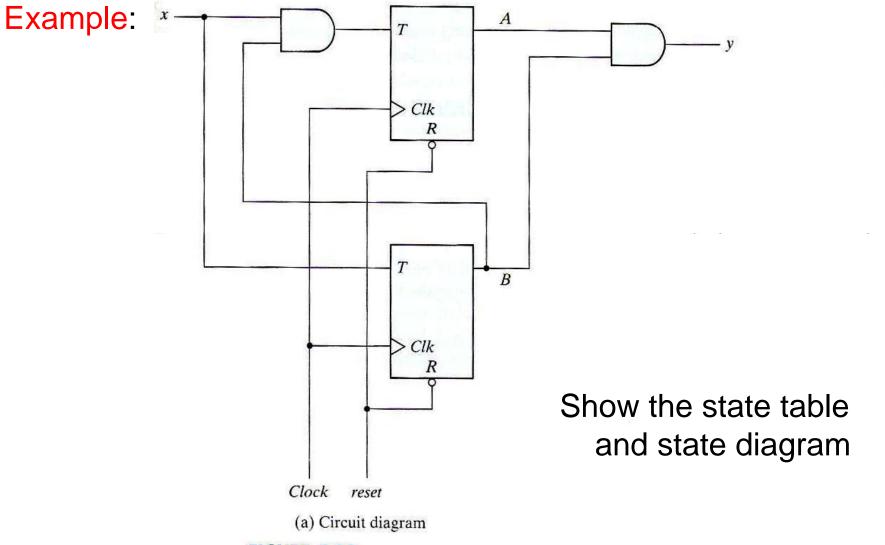
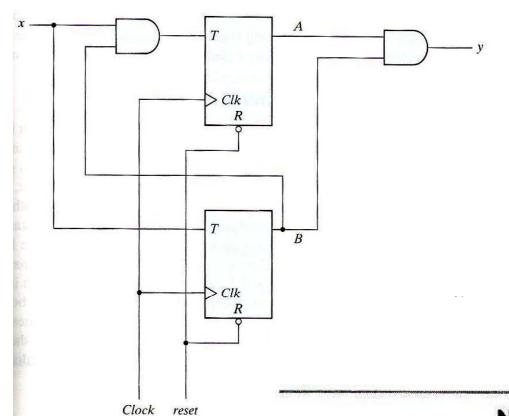


FIGURE 5.20 Sequential circuit with *T* flip-flops



P	resent
	State

Next State

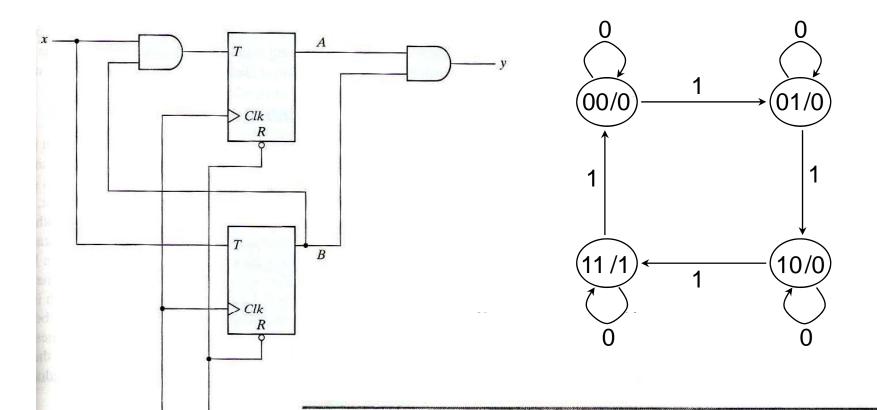
X	=	0	X	=	1

Output

circuit

- → state table
- → state diagram

					enimmuswa	
A	В	Α	В	Α	В	y
0	0	0	0	0	1	0
0	1	O	1	1	0	0
1	0	1	0	1	1	0
1	1	1	1	0	0	1



State

				• 4
	r			IŤ.
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- → state table
- → state diagram

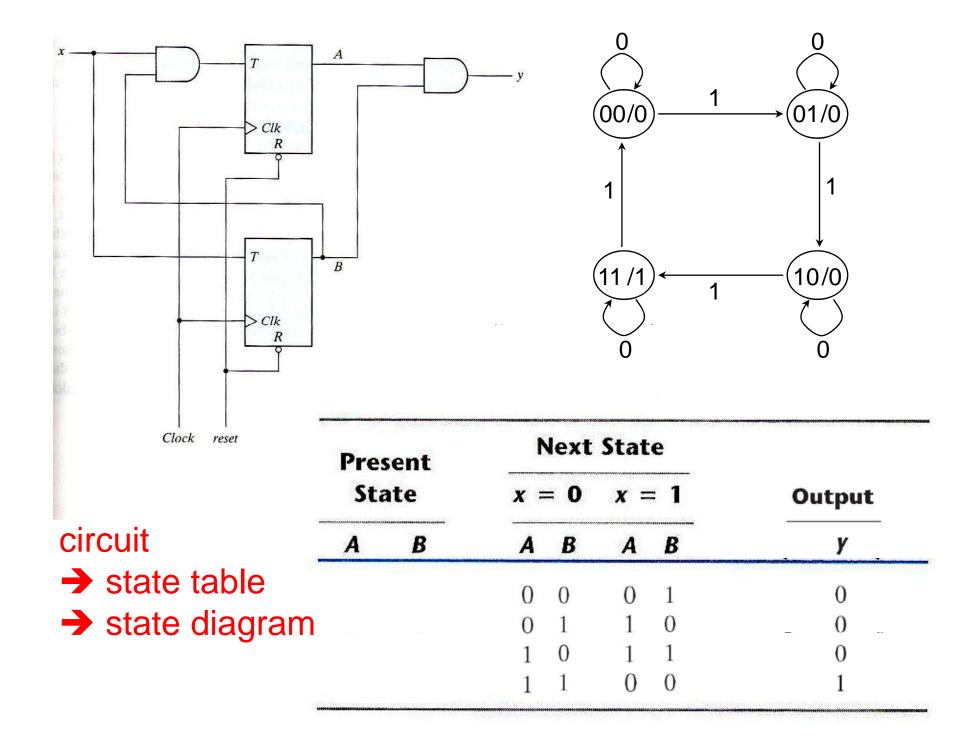
Clock reset

Present Next State

		0.34		
v	=	n	X	_ 7
^		U	^	

A	В	A	В	A	В	y
0	0	0	0	0	1	0
0	1	O	1	1	0	_ 0
1	0	1	0	1	1	0
1	1	1	1	0	0	1

Output



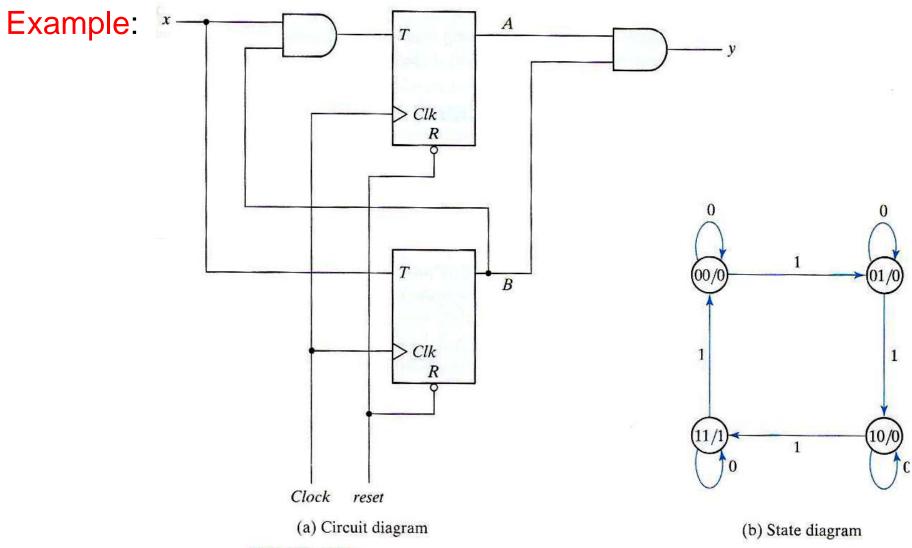
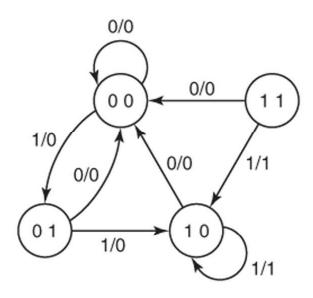
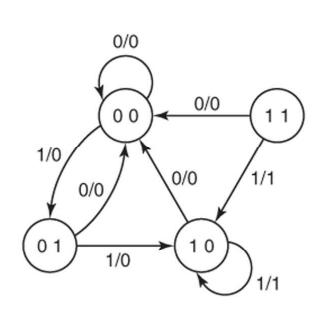


FIGURE 5.20 Sequential circuit with *T* flip-flops

Example: state diagram = state table



Example: state diagram = state table



	q^*		z	
\boldsymbol{q}	x = 0	x = 1	x = 0	x = 1
0 0	0 0	0 1	0	0
0 1	0 0	1 0	0	0
1 0	0 0	1 0	0	1
1 1	0 0	1 0	0	1

Example: Show the state diagram of following circuit

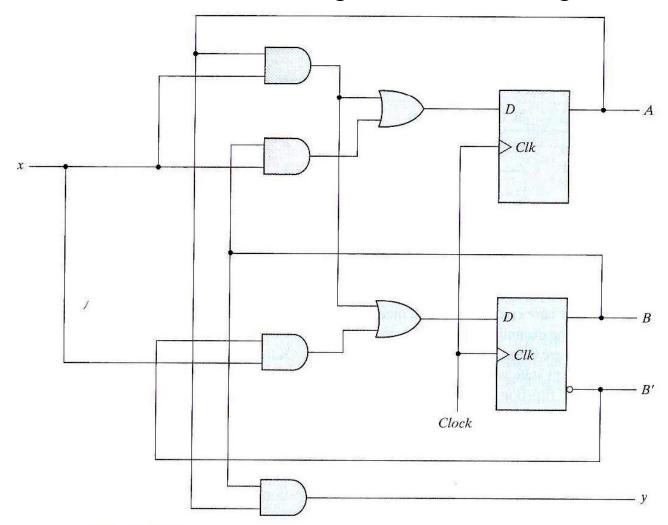


FIGURE 5.29
Logic diagram of sequence detector

Example: Show the state diagram of following circuit

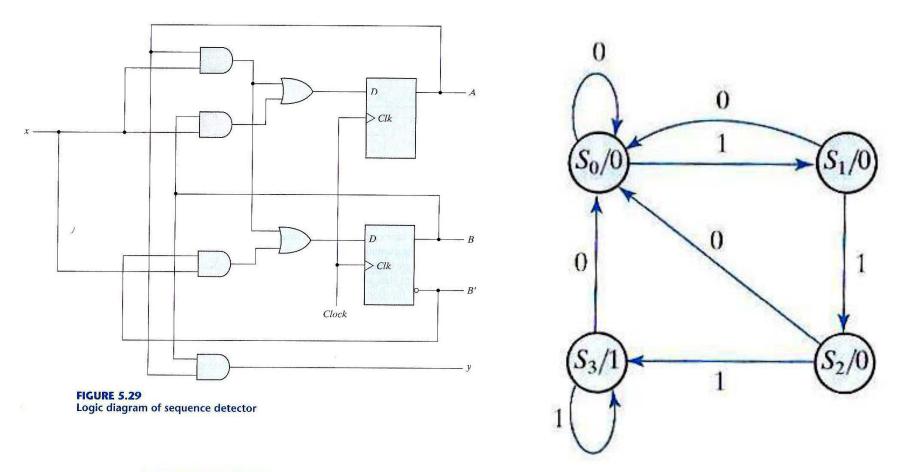


FIGURE 5.27
State diagram for sequence detector

More Example: Binary Counter – show state diagram and table

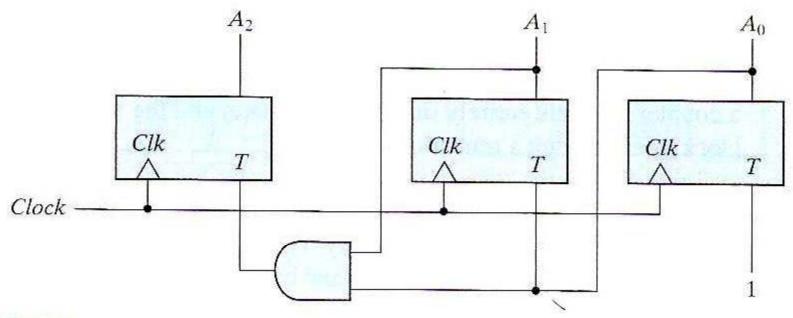


FIGURE 5.34
Logic diagram of three-bit binary counter

More Example: Binary Counter – show state diagram and table

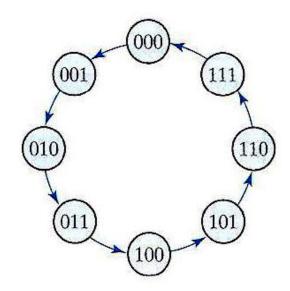


FIGURE 5.32
State diagram of three-bit binary counter

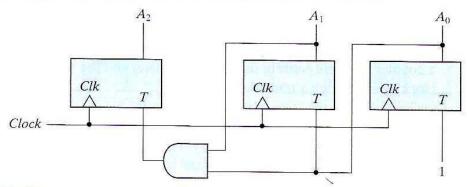


FIGURE 5.34 Logic diagram of three-bit binary counter

Quiz:

http://www.eelab.usyd.edu.au/digital_tutorial/part3/t-diag.htm

Quiz: solution

http://www.eelab.usyd.edu.au/digital_tutorial/part3/t-diag.htm

More Example:

http://www.eelab.usyd.edu.au/digital_tutorial/part3/example1-1.htm