A Low Power Dynamic Bitwidth-Adaptive Multiply Accumulate Unit for TinyML Accelerators using eSim

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***Abstract*—This report presents the design and simulation of a low-power, dynamic bitwidth-adaptive Multiply Accumulate (MAC) unit for TinyML accelerators. The architecture supports mixed-precision modes and integrates a shift-and-add multiplier, hybrid CLA-based accumulator, and zero-aware clock gating. The design is verified using eSim and synthesized using the IHP SG13G2 PDK.**

I. Objective

The objective of this project is to develop a power-efficient MAC unit suitable for TinyML workloads. Key goals include:

- Support for multiple precision modes (2×2 to 8×8)
- Signed × unsigned multiplication
- Dynamic bitwidth adaptation and zero-aware gating
- Verification using eSim and synthesis using SG13G2 PDK

II. Circuit Schematic

The MAC unit consists of a dynamic bitwidth multiplier, hybrid CLA-based accumulator, and clock gating logic. The schematic was designed in KiCad and simulated using NgSpice.

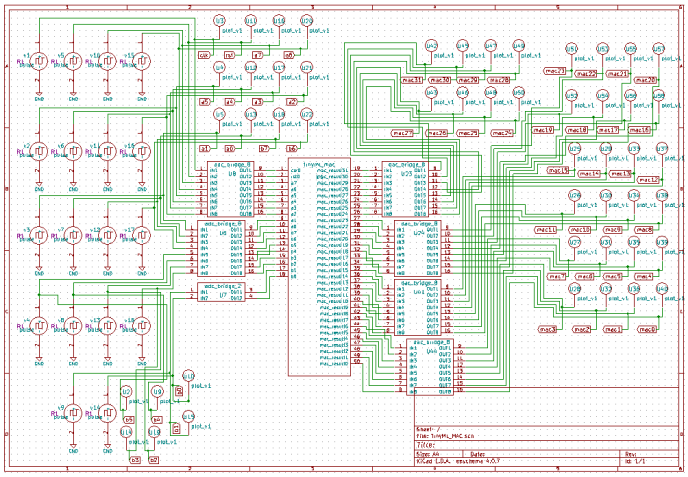

Fig. 1: MAC Unit Schematic in eSim

III. Simulation Results

Functional simulation was performed using Icarus Verilog. The RTL was then converted to NgVeri and simulated in eSim. Waveforms confirm correct operation across precision modes.

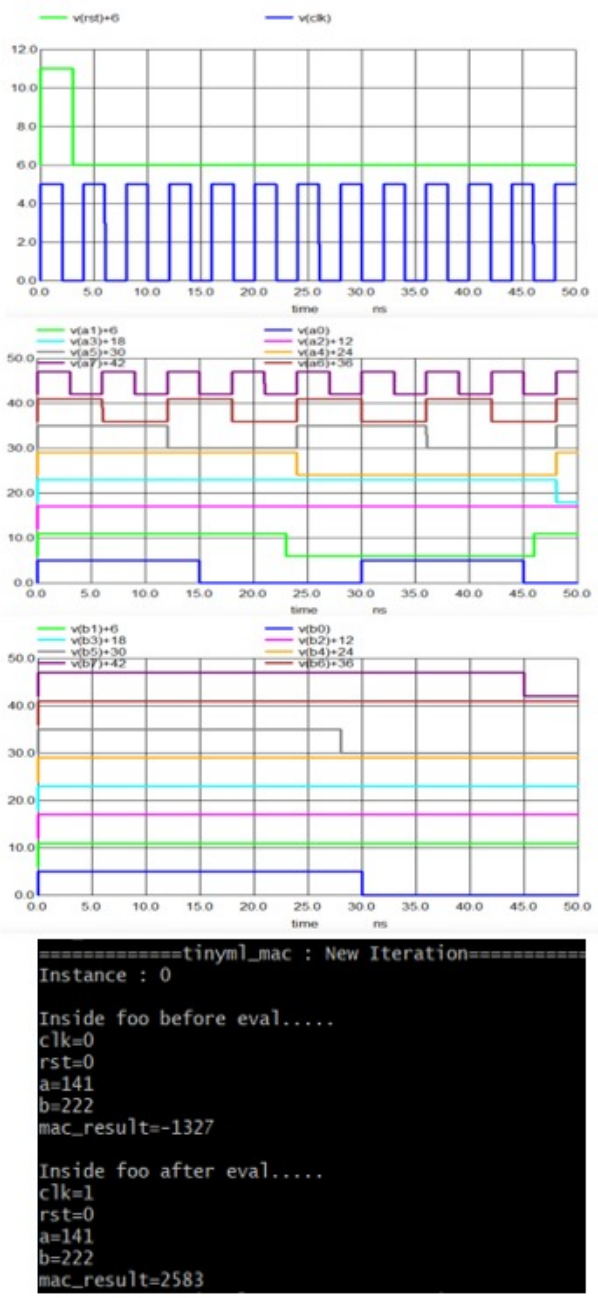

Fig. 2: Simulation Results of eSim

IV. Synthesis Results using IHP SG13G2 PDK

To meet the objectives of the eSim Marathon, the proposed MAC unit was synthesized using the IHP SG13G2 PDK. The synthesis was performed hierarchically, with each module mapped to standard cells from the SG13G2 library. The results validate the design's compatibility with silicon implementation and its suitability for low-power TinyML applications.

A. Module-Level Cell Usage

- **cla_4bit:** 24 cells
- **cla_enable_generator:** 134 cells
- **datapath:** 676 cells
- **hybrid_adder_accumulator:** 28 cells
- **tinyml_mac (top):** 9 cells

B. Design Summary

- **Total wires:** 875
- **Total wire bits:** 2713
- **Public wire bits:** 663
- **Total cells:** 1065
- **Memory/processes:** None

C. Standard Cell Breakdown

- **sg13g2_and2_1:** 199 instances
- **sg13g2_inv_1:** 119 instances
- **sg13g2_xnor2_1:** 124 instances
- **sg13g2_xor2_1:** 104 instances
- **sg13g2_a21oi_1:** 69 instances
- **sg13g2_o21ai_1:** 68 instances
- **sg13g2_nand2_1:** 96 instances
- **sg13g2_nor2_1:** 84 instances

These results confirm that the MAC unit is well-optimized for implementation using the SG13G2 PDK and maintains low complexity while supporting dynamic precision and gating features.

V. Conclusion

The proposed MAC unit demonstrates high energy efficiency and low power consumption, making it suitable for TinyML accelerators. The design supports dynamic bitwidth adaptation and zero-aware gating, and its successful synthesis using SG13G2 PDK validates its readiness for silicon implementation.

VI. GitHub Repository and Project Summary

This project was submitted as part of the **eSim Marathon 2025** organized by FOSSEE, IIT Bombay. The complete source files, simulation artifacts, schematic, and synthesis results are available in the GitHub repository below:

GitHub Link:
https://github.com/ajayboddu-2006/eSim_Marathon_2025.git

References

[1] S. Perika, B. Ajay, S. Kar, "A Low Power Dynamic Bitwidth-Adaptive Multiply Accumulate Unit for TinyML Accelerators," *ICTACT Journal on Communication Technology (IJCT)*, vol. 16, no. 3, pp. 3586–3593, Sep. 2025. DOI: 10.21917/ijct.2025.0534.