LAB REPORT

Spice Simulation I (Diode Applications)

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01 : Half wave Rectifier

Application of the diode:

The diode in a half wave rectifier circuit passes just one half of each complete sine wave of the AC supply in order to convert it into a DC supply. It does the job because of its forward bias and reverse bias functionality.

It only allows current to flow through it only when it is forward biased and stops current flow when it is reverse biased, thus the negative half-cycle is passed through the reverse biased diode to prevent negative waveform.

Circuit diagram:

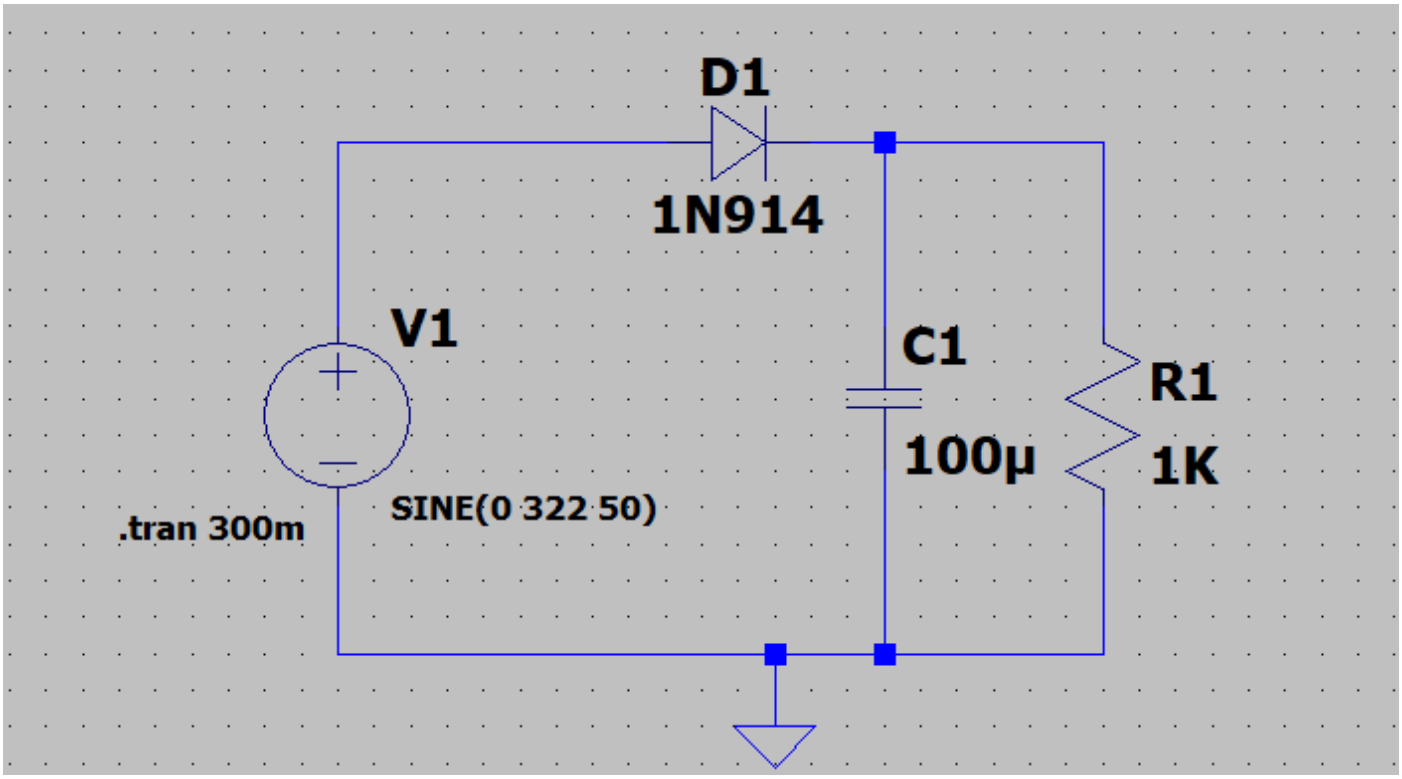

Fig: Circuit diagram for half wave rectifier in LTSpice

Circuit operation:

A half wave rectifier is defined as a type of rectifier that only allows one half-cycle of an AC voltage waveform to pass, blocking the other half cycle. It requires only a single diode to construct a half wave rectifier.

In the circuit above, as a positive cycle if V1 starts the diode is in forward bias and it also charges the capacitor in its wat to the load resistor. When the negative half cycle starts, the diode is reverse biased then and hence it stops the current from flowing into the load resistor but the charged capacitor gets discharged gradually and forms a ripple in the waveform.

Expected results:

The expected result is the waveform which has no negative part and every alternate half-cycle experiences a ripple due to the discharge of the capacitor in every negative half-cycle.

Ripple factor: The ripple factor is the ratio between the RMS value of the AC voltage (on the input side) and the DC voltage (on the output side) of the rectifier. The ripple factor of half wave rectifier is equal to 1.21. The calculation is shown below:

⊙ Ripple factor for half-wave rectifier:

$$V_r(rms) = \left[\frac{1}{T}\int_0^T V_{ac}^2\, dt\right]^{1/2}$$

$$= \left[\frac{1}{2\pi}\int_0^{2\pi} (V - V_{dc})^2\, dt\right]^{1/2}$$

$$= \left[\frac{1}{2\pi}\int_0^{2\pi} (V^2 - 2V V_{dc} + V_{dc}^2)\, dt\right]^{1/2}$$

$$= \left\{\frac{1}{2\pi}\int_0^{2\pi} V^2 dt - \frac{1}{2\pi}\int_0^{2\pi} 2V V_{dc}\, dt + \frac{1}{2\pi}\int_0^{2\pi} V_{dc}^2\, dt\right\}^{1/2}$$

$$= \left[V_{rms}^2 - 2V_{dc}^2 + V_{dc}^2\right]^{1/2}$$

$$= \left[V_{rms}^2 - V_{dc}^2\right]^{1/2}.$$

Here, V_{rms} is the rms value of the total voltage.

→ for half wave rectifier:

$$V_r(rms) = \left(V_{rms}^2 - V_{dc}^2\right)^{1/2}$$

Now, V_{rms} for half wave rectified signal is $\left(\frac{V_m}{2}\right)$ and V_{dc} for half wave rectified signal is $\frac{V_m}{\pi}$.

So, $V_r(rms) = \sqrt{\left(\frac{V_m}{2}\right)^2 - \left(\frac{V_m}{\pi}\right)^2} = 0.385\, V_m$.

Now, Ripple factor $(r) = \frac{V_r(rms)}{V_{dc}} = \frac{0.385\, V_m}{V_m/\pi} = 0.385\pi = \boxed{1.21}$

Simulation results:

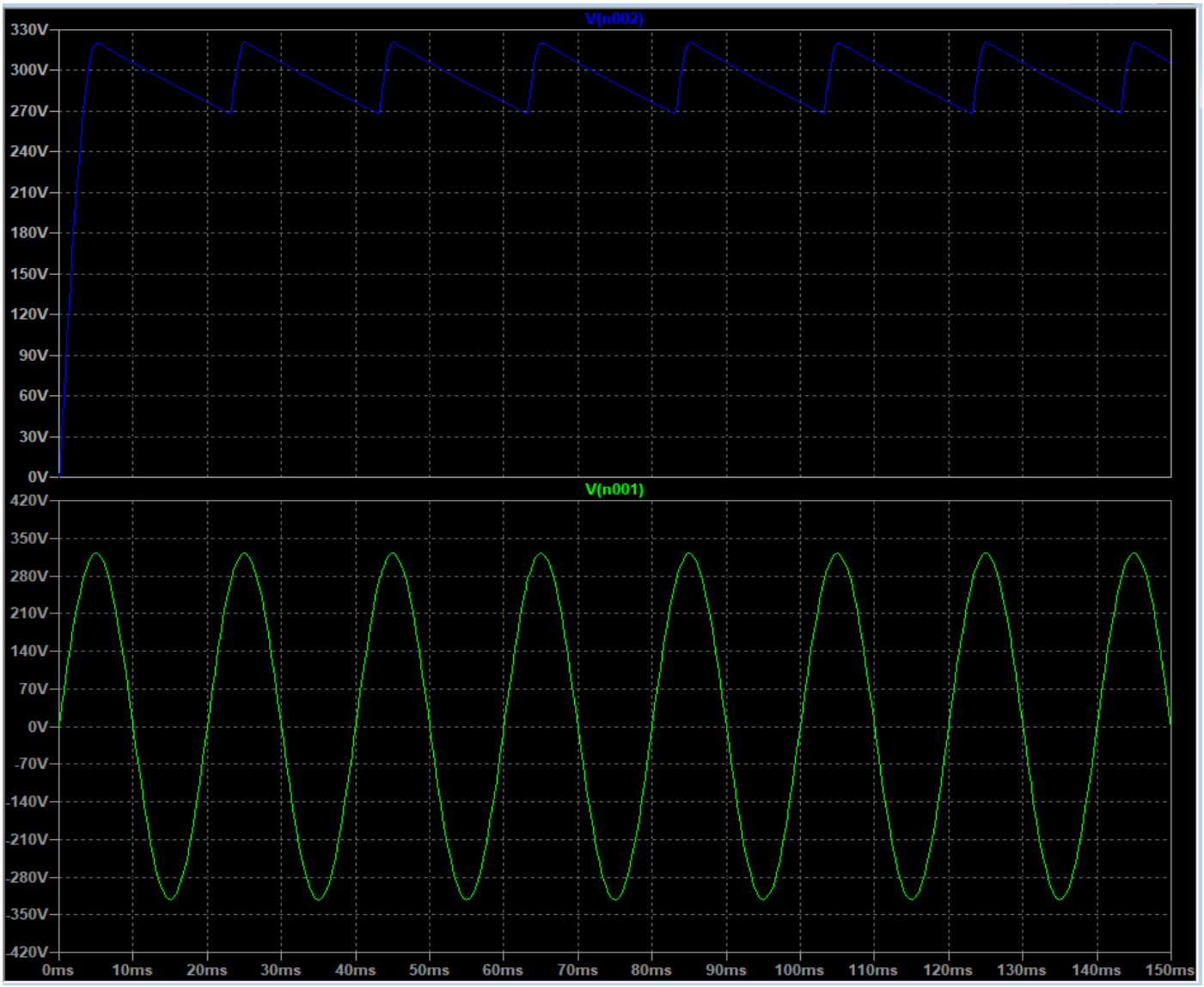

Fig: Blue graph shows the rectified output and green waveform depicts input

Real world applications:

Half wave rectifier circuits are comparatively easier to build and cheaper. Though half wave rectifier circuits are not as commonly used as the full wave rectifiers but half wave rectifier circuits are used in come insensitive devices which can withstand voltage variations. Some important uses of half wave rectifiers are:

1. Low power simple battery charger circuit.
2. In pulse generator circuits.
3. Soldering iron circuit.
4. Half wave rectifier is used in Amplitude Modulation radio circuits as detector.

02 : Full wave Rectifier

Application of the diode:

The diodes are arranged in such a way in full wave rectifier circuit such that two diodes are forward biased during the positive half-cycle and other two diodes are forward biased during the negative half-cycle.

This way the full wave rectifier circuit helps eliminate the negative part of the output and gives the output as completely positive waveform.

Circuit diagram:

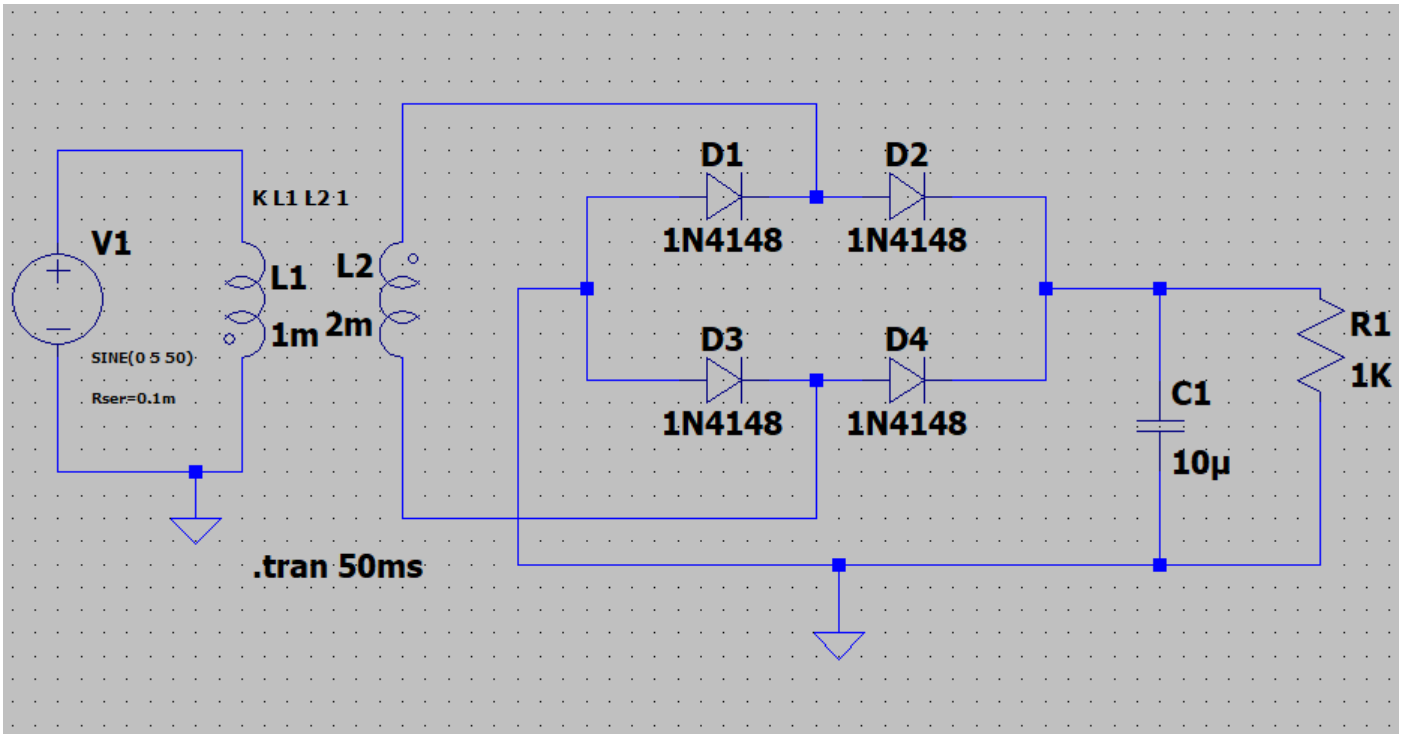

Fig: Circuit diagram for Full wave rectifier in LTSpice

Circuit operation:

There are four diodes labelled D1 to D4 and they are arranged in series pairs with only two diodes conducting current during each half-cycle duration.

When the positive half-cycle of the supply goes, D2 and D3 conduct in series while D1 and D4 are reverse biased and the current flows through the load.

During the negative half-cycle, D1 and D4 diodes conduct in series and diodes D2 and D3 switch off as they are now in reverse-biased configuration.

Current flowing through the load is the unidirectional mode and the voltage developed across the load is also unidirectional voltage. Therefore the average DC voltage across the load is 0.637V. During each half-cycle, the current flows through two diodes instead of just one

diode, so the amplitude of the output voltage is two voltage drops 1.4V less than the input V_{max} amplitude, ripple frequency is now twice the supply frequency 100Hz for a 50Hz supply.

Expected results:

Expected result is a positive only waveform which attains peak for every positive and negative half-cycle.

Ripple factor:

⇒ for full wave rectified signal

$$V_{rms} = \frac{V_m}{\sqrt{2}} \quad \text{and} \quad V_{dc} = \frac{2V_m}{\pi}$$

So,
$$V_r(rms) = \sqrt{V_{rms}^2 - V_{dc}^2}$$

or,
$$V_r(rms) = \sqrt{\left(\frac{V_m}{\sqrt{2}}\right)^2 - \left(\frac{2V_m}{\pi}\right)^2}$$

or,
$$V_r(rms) = 0.308\, V_m.$$

Now, ripple factor(r) =
$$\frac{0.308\, V_m}{V_{avg} \text{ or } V_{dc}}$$

or,
$$r = \frac{0.308\, V_m}{\frac{2V_m}{\pi}}$$

or,
$$\boxed{r = 0.483.}$$

Simulation results:

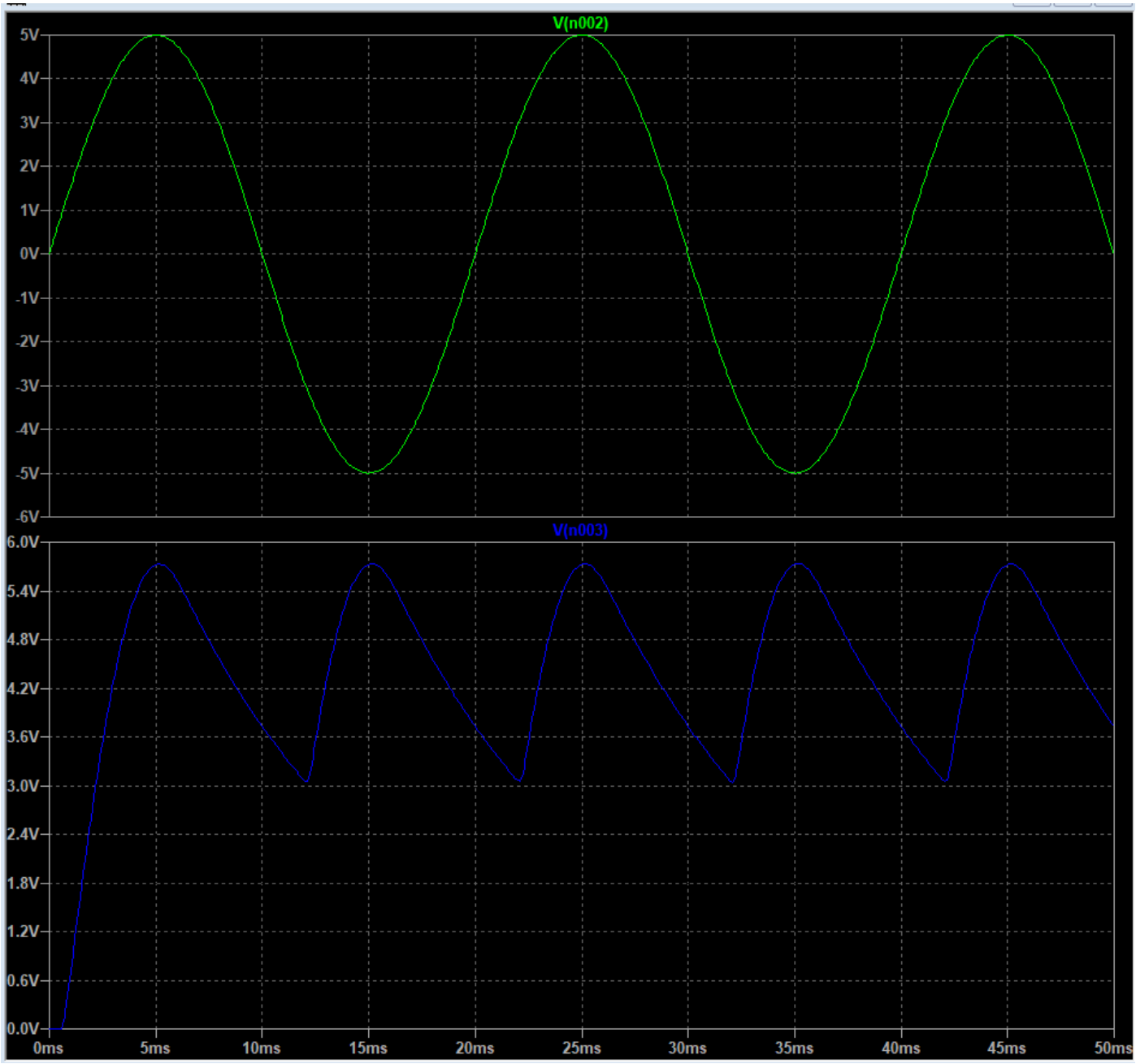

Fig: Blue graph shows the rectified output and green waveform depicts input

Real world applications:

There are many real world applications of full wave rectifiers such as:

1. For detecting the amplitude of the modulating radio signal.
2. To supply steady and polarised DC voltage in electric welding.
3. In power supply for various appliances.
4. Used for power supply in devices which require DC supply like motor and LED.

03 : Clipper Circuit

Application of the diode:

A clipping circuit or a clipper is a device used to ‘clip’ the input voltage to prevent it from attaining a value larger than a predefined one.

Depending on the features of the diode, the positive or negative region of the input signal is “clipped” off and accordingly the diode clippers may be positive or negative clippers.

Circuit diagram:

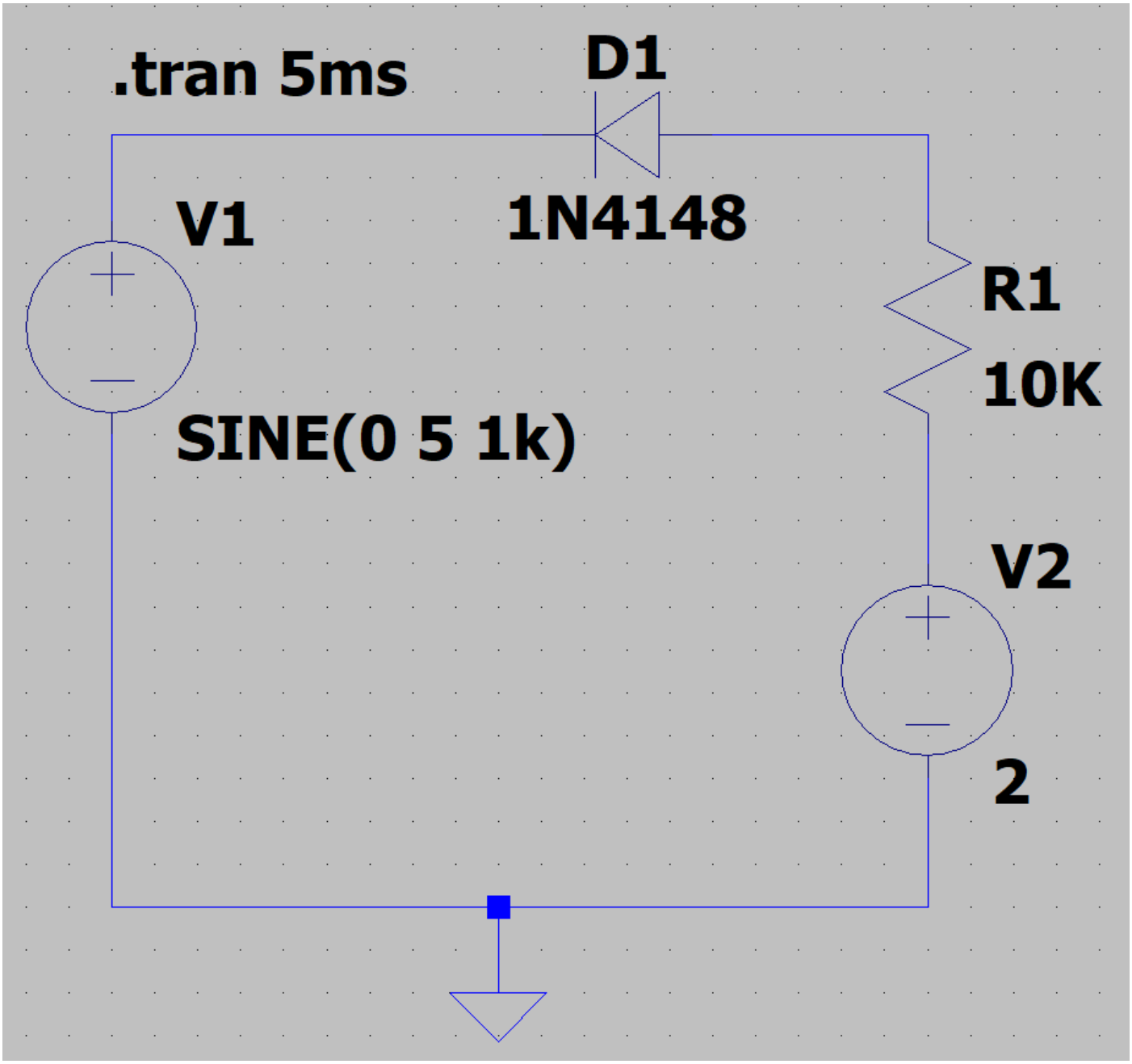

Fig: Circuit diagram of a Clipper circuit in LTSpice

Circuit operation:

In a positive clipper, the positive half cycles of the input voltage will be removed. A biased clipper comes in handy when a small portion of positive or negative half cycles of the signal voltage is to be removed. When a small portion of the positive half cycle is to be removed, it is called a biased positive clipper.

In the clipper circuit, the diode is kept in series with the load. During the positive half cycle of the input waveform, the diode 'D' is reverse biased, which maintains the output voltage at 0 Volts but since a DC voltage of 2 Volts is applied at the load resistor hence the positive waveform is clipped at 2V.

During the negative half cycle of the input, the diode is forward biased and so the negative half cycle appears across the output.

Expected results:

The waveform expected is such that the positive waveform gets clipped at 2V and the negative waveform remains unchanged.

Simulation results:

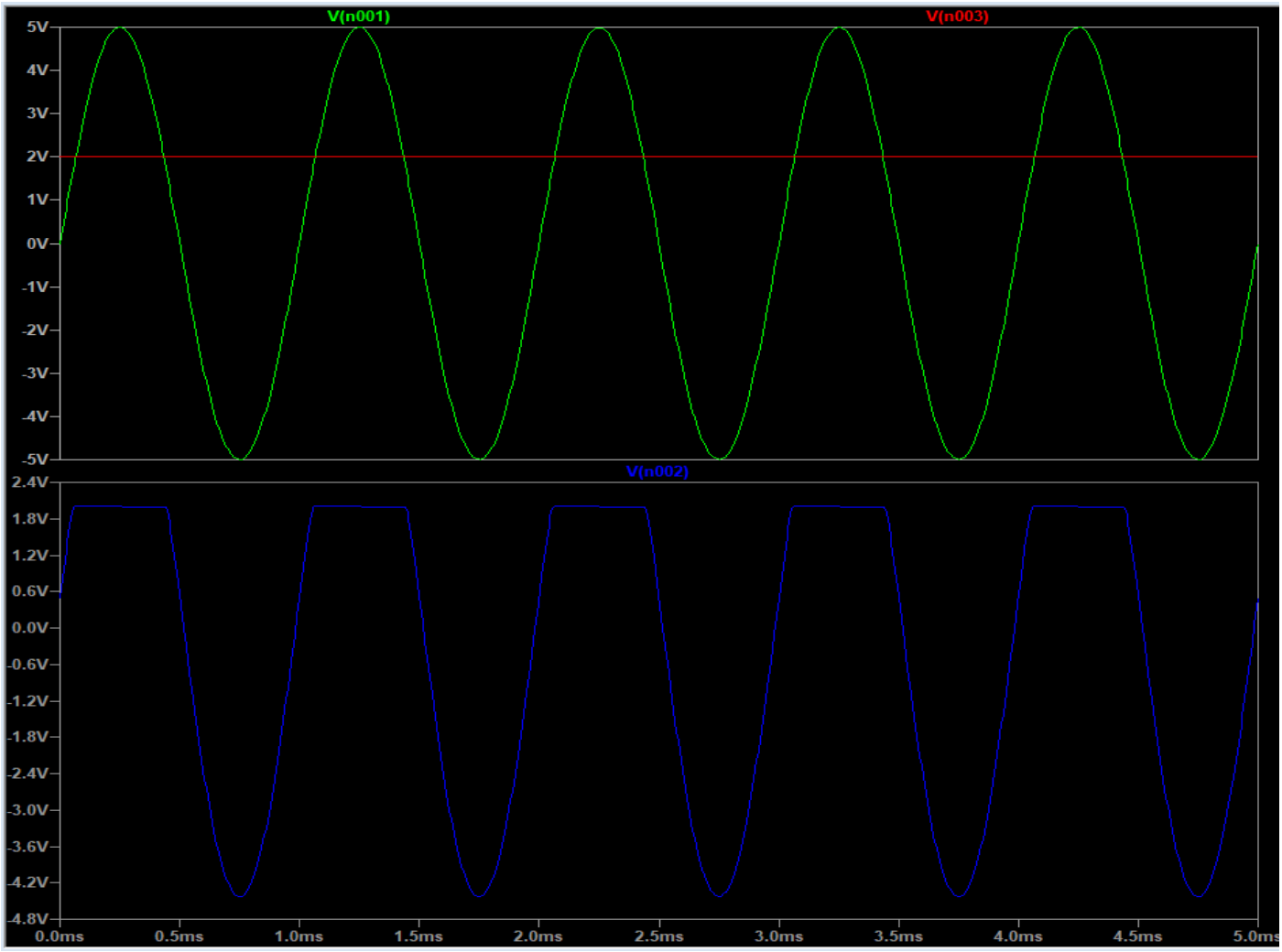

Fig: Simulation result (Waveform) of Clipper circuit (Clipped at 2V)

Real world applications:

A few among many uses of the clipper circuit are:

1. In FM transmitters to reduce noise.
2. To limit the voltage input to a device.
3. To modify an existing waveform to get the desired output.

04 : Clamper Circuit

Application of the diode:

The circuit will be called a positive clamper, when the signal is pushed upward by the circuit. When the signal moves upward, the negative peak of the signal coincides with the zero level.

Circuit diagram:

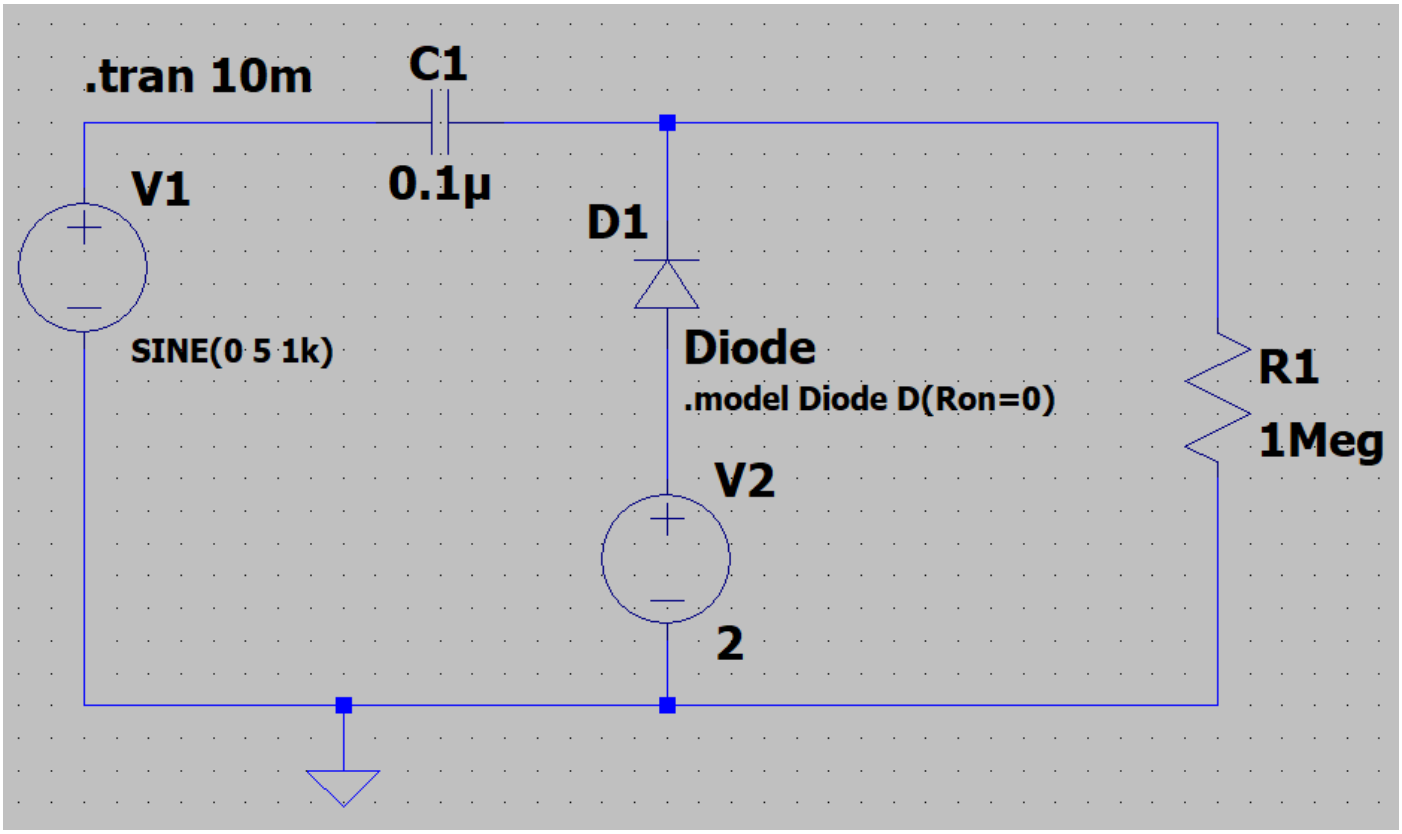

Fig: Circuit Diagram of a Clamper Circuit (Clamped to 2V)

Circuit operation:

For a clamping circuit four components are required here: a diode, a capacitor, a resistor, and an independent DC supply for a shift of 2V.

Here we have considered a positive clamping circuit, a circuit that shifts the original signal in a vertically upward direction. The diode D will be reverse biased and the capacitor C is charged with the polarity, when an input signal is applied. During the negative half cycle of input, the output voltage will be equal to the barrier potential of the diode, V_0 and the capacitor is charged to $(V - V_Q)$.

During the positive half cycle, the diode becomes reverse-biased and acts as an open-circuit. Thus, there will be no effect on the capacitor voltage.

The resistance R, being of very high value, cannot discharge C a lot during the negative portion of the input waveform. Thus during negative input, the output voltage will be the sum of the input voltage and the capacitor voltage and is equal to – V – (V — V_0) or – (2 V – V_0). The value of the peak-to-peak output will be the difference of the negative and positive peak voltage levels is equal to V_0 - [-(2V-V_0)] or 2 V.

We have also taken a bias voltage of 2V for an additional shift of the output waveform by 2 Volts.

Expected results:

We expect to see the same waveform but shifted upwards such that the lowest value is 2V but the peak to peak voltage difference remains the same as input.

Simulation results:

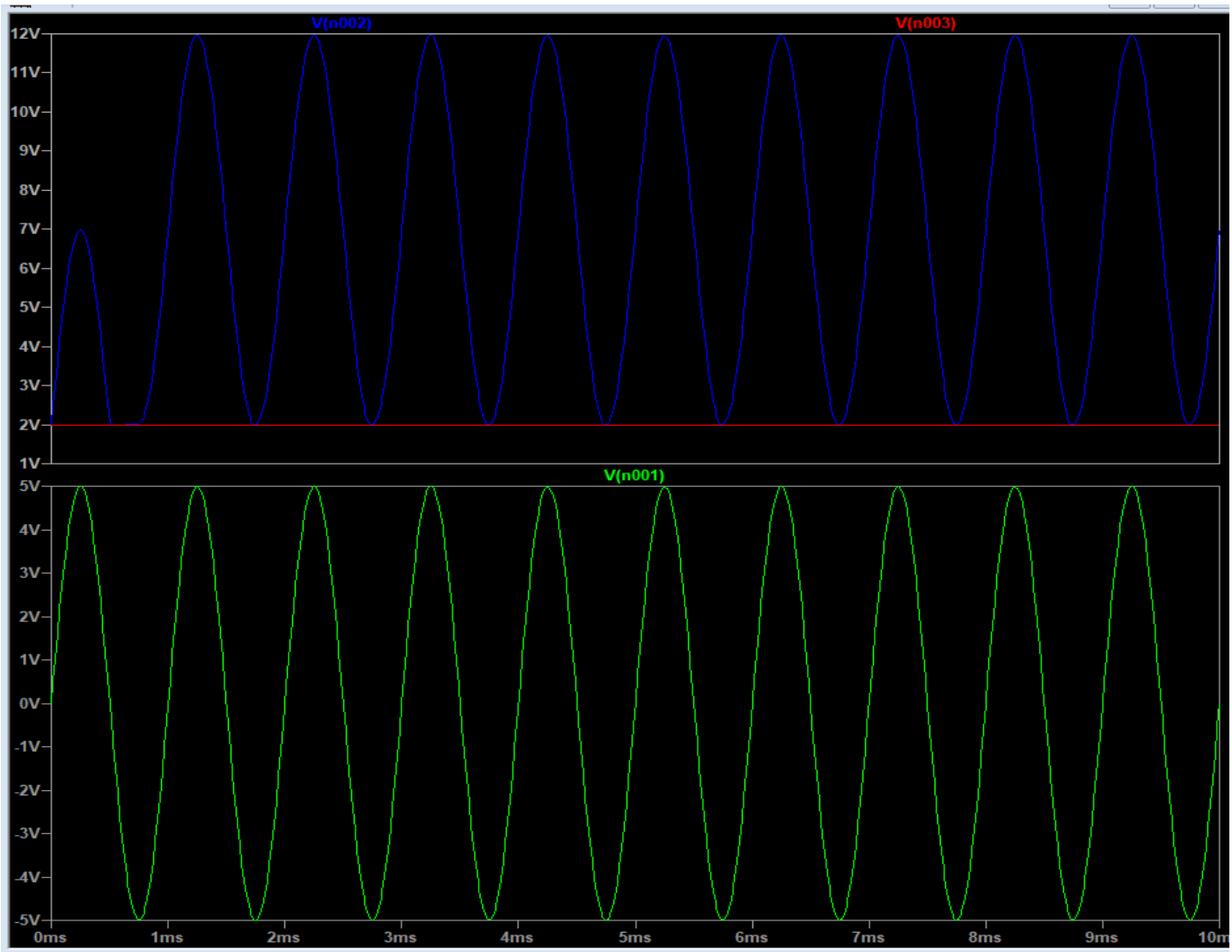

Fig: Simulation result (Waveform) of Clamper circuit (Clamped to 2V). Blue and green signals are the output and input signals respectively.

Real world applications:

Some of the applications or real world use of clamper circuits are:

1. In SONAR and RADAR testing.
2. As voltage doublers.
3. To remove distortions in circuit.
4. In video processing equipment like TV.

05 : Voltage Doubler Circuit

Application of the diode:

Voltage doubler can deliver the output voltage which is double as that of the input voltage. It is a voltage multiplier with the voltage multiplication factor equal to 2.

The circuit is formed by an oscillating AC input voltage, two capacitors and two diodes. The input is AC voltage and the output will be DC voltage with twice the peak value of the input AC.

Circuit diagram:

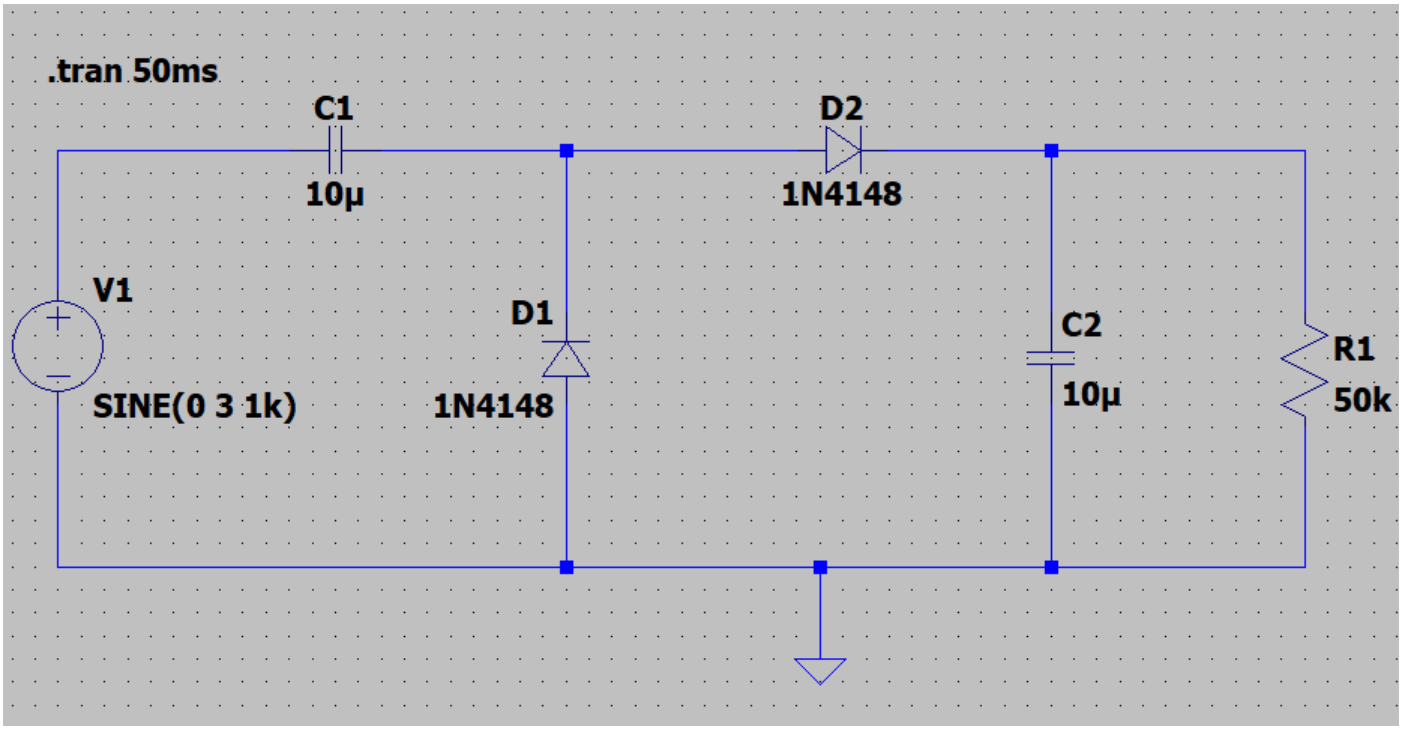

Fig: Circuit diagram of a voltage doubler

Circuit operation:

In the first negative half-cycle the diode D1 will be forward biased and will conduct hence charging the capacitor C1 to around ~2.4V because of the voltage drop across diode (~0.6V). Now, since the capacitor C1 is fully charged, so during the positive half-cycle, when the diode D2 will be in forward bias will have a potential drop of ~4.8V (due to voltage drop across diode) and hence will charge the capacitor C2 to 4.8V.

Again during the negative half-cycle the above process will repeat itself but since the capacitor C2 will discharge now, we need to make sure that the load resistance is high enough not to discharge the capacitor too quickly.

Expected results:

We expect to see a waveform with small ripples due to the choice of a good amount of load resistance and a voltage signal double ~4.8V considering the voltage drops across the two diodes.

Simulation results:

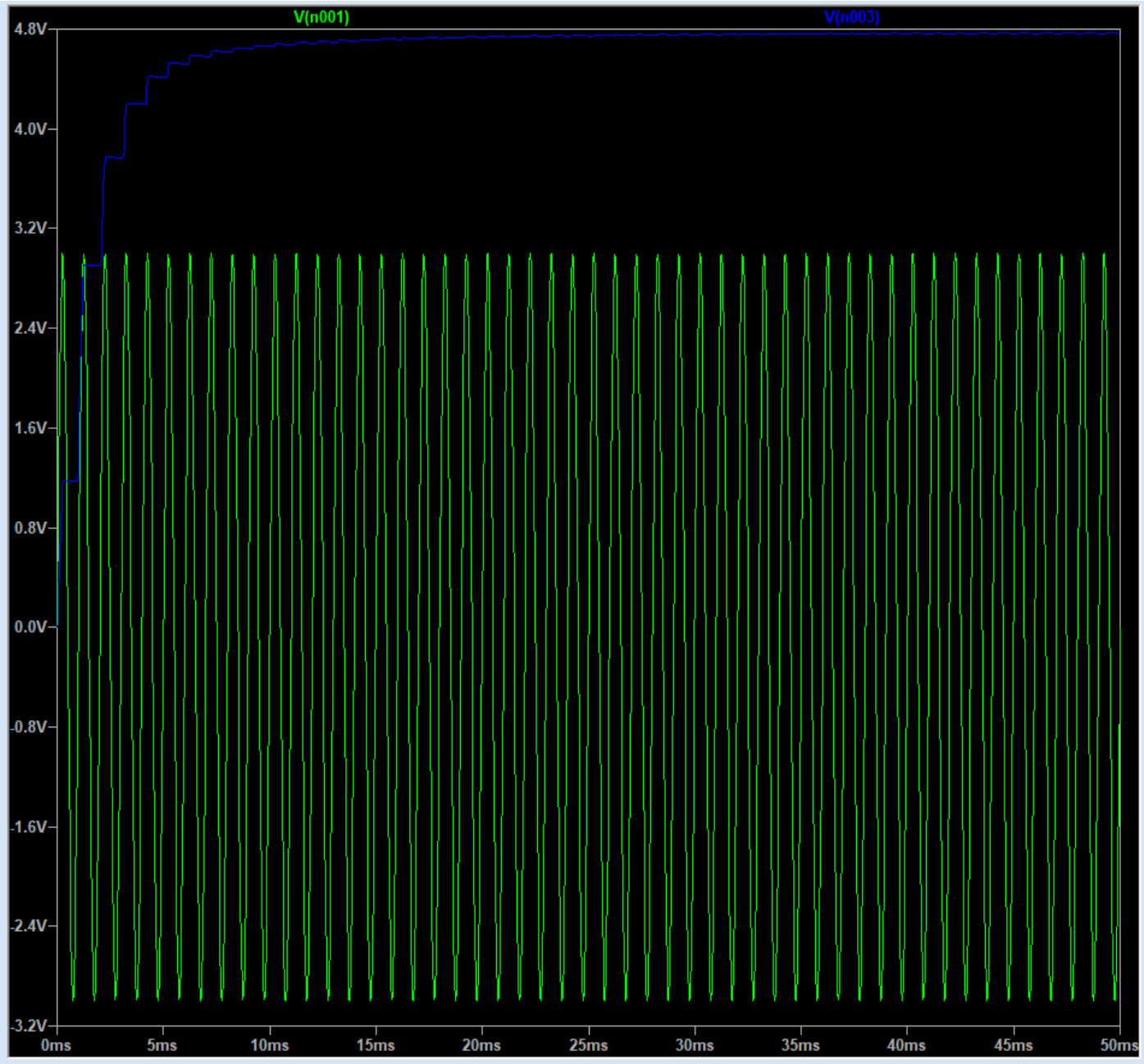

Fig: Simulation result (Waveform) of Voltage doubler circuit. Blue and green signals are the output and input signal respectively.

Real world applications:

Some of the applications of a voltage doubler circuit are:

1. Ion pumps.

2. TV Cathode ray tubes.
3. X-Ray Systems.
4. Copy machine.
5. Radar equipment etc.

06 : Inverter Logic Gate

Application of the diode:

An inverter logic gate circuit outputs a voltage representing the opposite logic-level to its input. Its main function is to invert the input signal applied.

If the applied input is low then the output becomes high and vice versa. An inverter circuit serves as the basic logic gate to swap between the two voltage levels 0 and 1.

Circuit diagram:

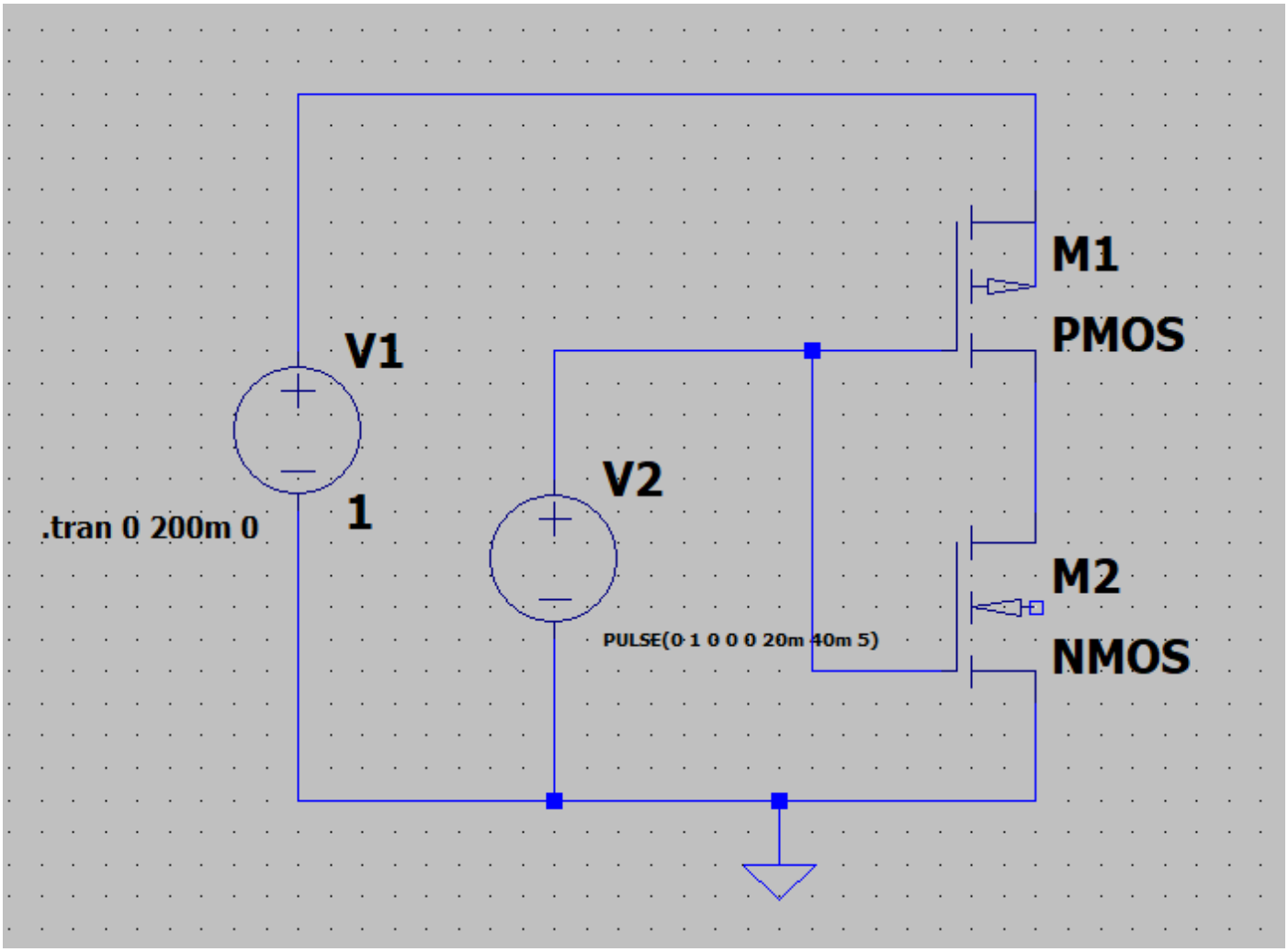

Fig: Circuit diagram of an Inverter logic circuit in LTSpice

Circuit operation:

The inverter circuit consists of PMOS and NMOS FET. The input from V2 serves as the gate voltage for both transistors. The NMOS transistor has input from V_{ss} (ground) and the PMOS transistor has input from V_{dd}. When a high voltage ($\sim V_{dd}$) is given at input terminal of the inverter, the PMOS becomes an open circuit, and NMOS gets switched OFF so the output will be pulled down to V_{ss}.

When a low-level voltage (<Vdd, ~0V) is applied to the inverter, the NMOS gets switched OFF and PMOS gets switched ON. So the output becomes V_{dd} or the circuit is pulled up to V_{dd}.

Expected results:

We expect to see the inverse waveform as output of an input waveform. The highs of the input wave should get inverted and should get depicted as the lows of the output waveform.

Simulation results:

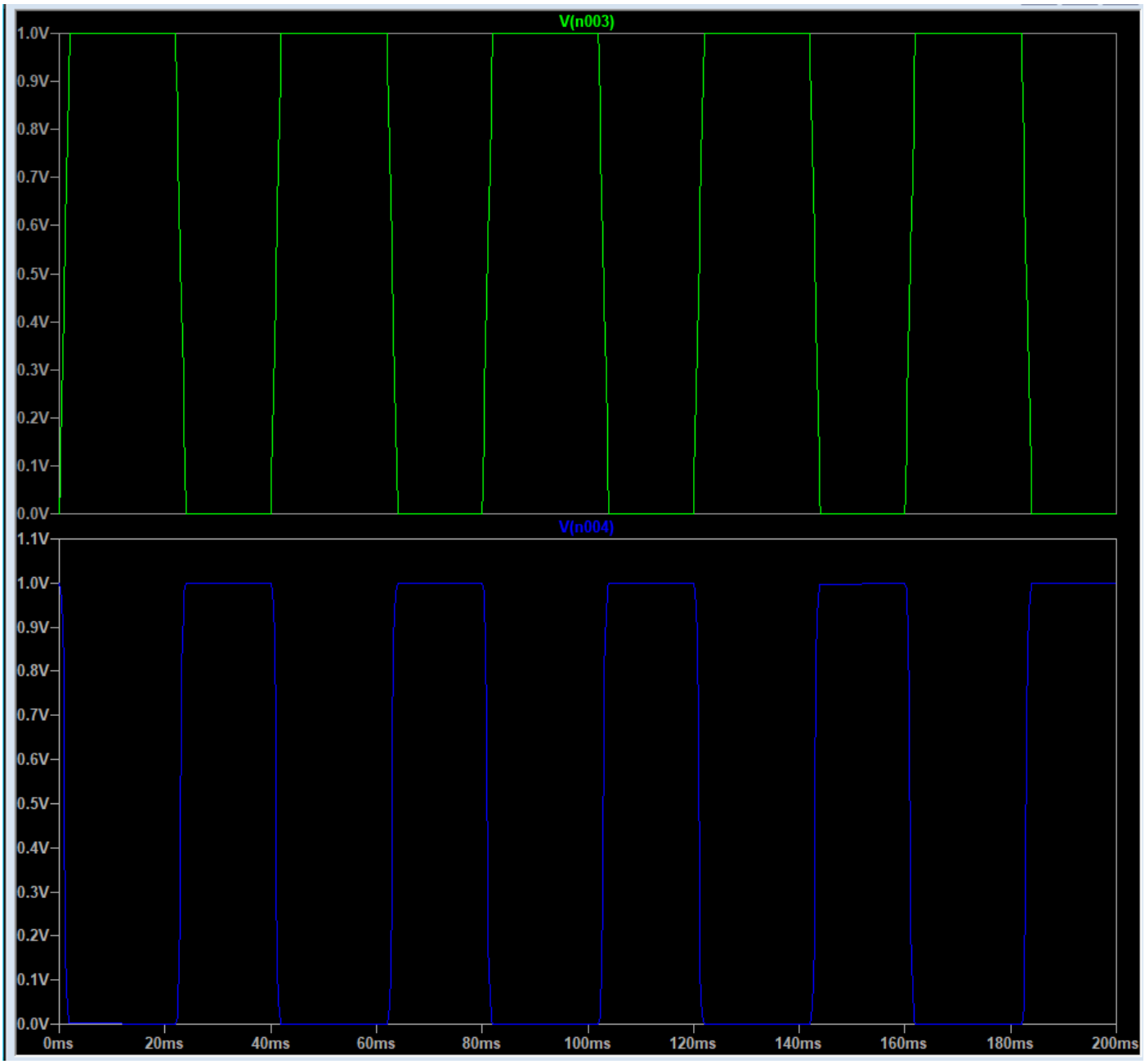

Fig: Simulation result (Waveform) of CMOS inverter logic circuit. Blue and green signals are the output and input signal respectively.

Real world applications:

Some of the applications of CMOS inverter logic gate circuits are:

1. In digital cameras.
2. As transmission gates.
3. For RF circuits and mixed signal devices.

07 : NOR Logic Gate

Application of the diode:

NOR logic gate is such a logic gate which is operate with the help of two input sources and two nMOS and two pMOS connected in parallel and series. It gives input as either high or low.

Precisely, it gives high output when both the inputs are low and in all other cases the output is low.

Circuit diagram:

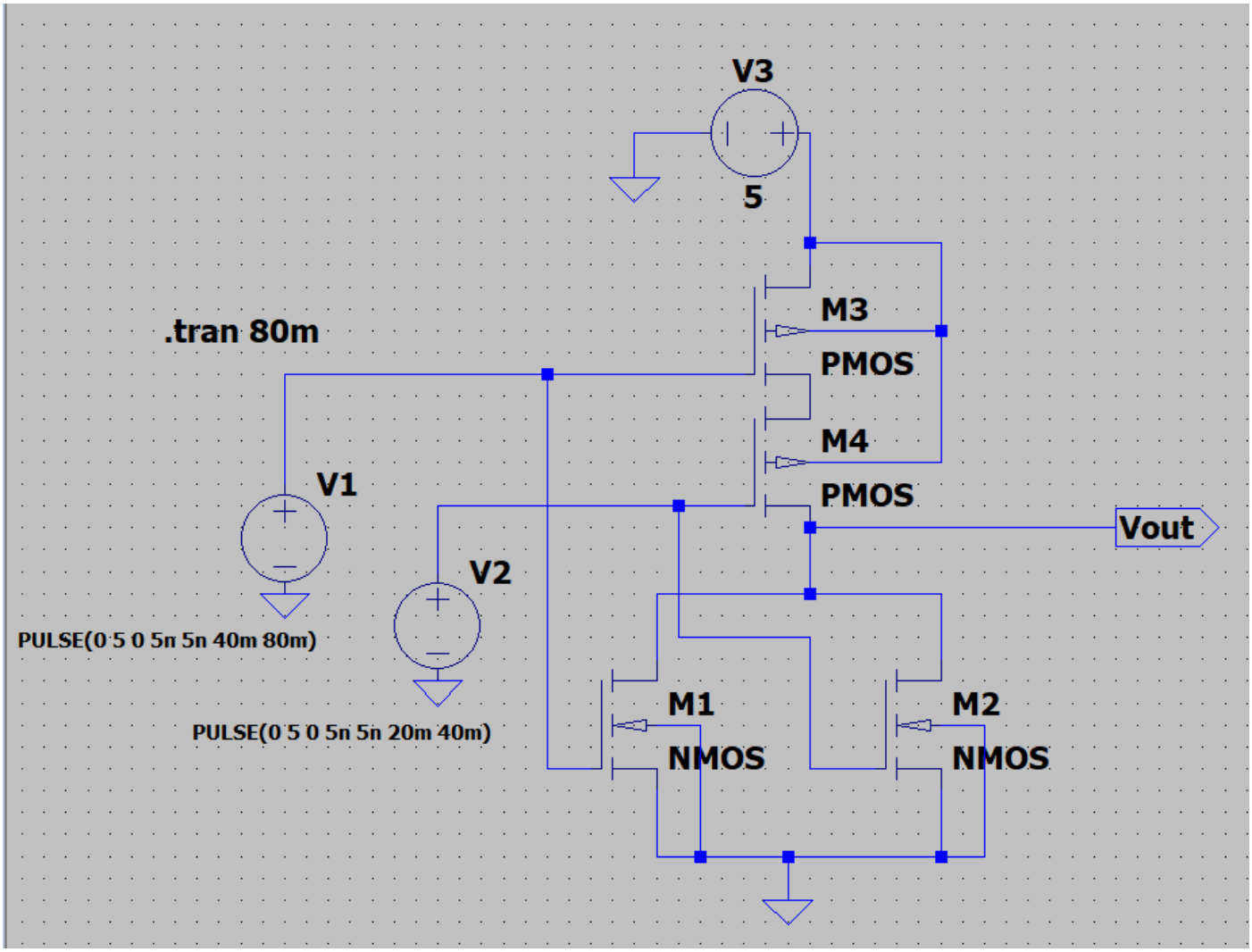

Fig: Circuit diagram of CMOS NOR logic gate in LTSpice

Circuit operation:

The NMOS transistors are in parallel to pull the output low when either input is high. The PMOS transistors are in series to pull the output high when both inputs are low. The output is never left floating.

The above drawn circuit is a 2-input CMOS NOR gate. Now let's understand how this circuit will behave like a NOR gate.

Case-1 : V1 – Low & V2 – Low

V1 – Low: pMOS1 – ON & nMOS1 – OFF

V2 – Low: pMOS2 – ON & nMOS2 – OFF

Path establishes from V_{dd} to V_{out} through the series connected ON pMOS transistors and V_{out} gets charged to V_{dd} level. No path from Vout to ground. Therefore, no discharging and hence V_{out} will be high.

Case-2 : V1 – Low & V2 – High

V1 – Low: pMOS1 – ON & nMOS1 – OFF

V2 – High: pMOS2 – OFF & nMOS2 – ON

In this case path establishes from V_{out} to ground through nMOS2, but no path to V_{dd}. So, V_{out} would get discharged and will be at level Low.

Case-3 : V1 – High & V2 – Low

V1 – High: pMOS1 – OFF & nMOS1 – ON

V2 – Low: pMOS2 – ON & nMOS2 – OFF

The explanation is similar as Case-2. Vout will be at level Low.

Case-4 : V1 – High & V2 – High

V1 – High: pMOS1 – OFF & nMOS1 – ON

V2 – High: pMOS2 – OFF & nMOS2 – ON

No path to V_{dd}. Path establishes from V_{out} to ground. So, V_{out} will be at level Low.

Expected results:

We expect to see an output waveform which shows high value only when both the input is low and in all other cases the output waveform is expected to show low value. The truth table below can depict the result very well where 1 depicts high and 0 depicts low:

V1	V2	V_{out}
0	0	1
0	1	0
1	0	0
1	1	0

Simulation results:

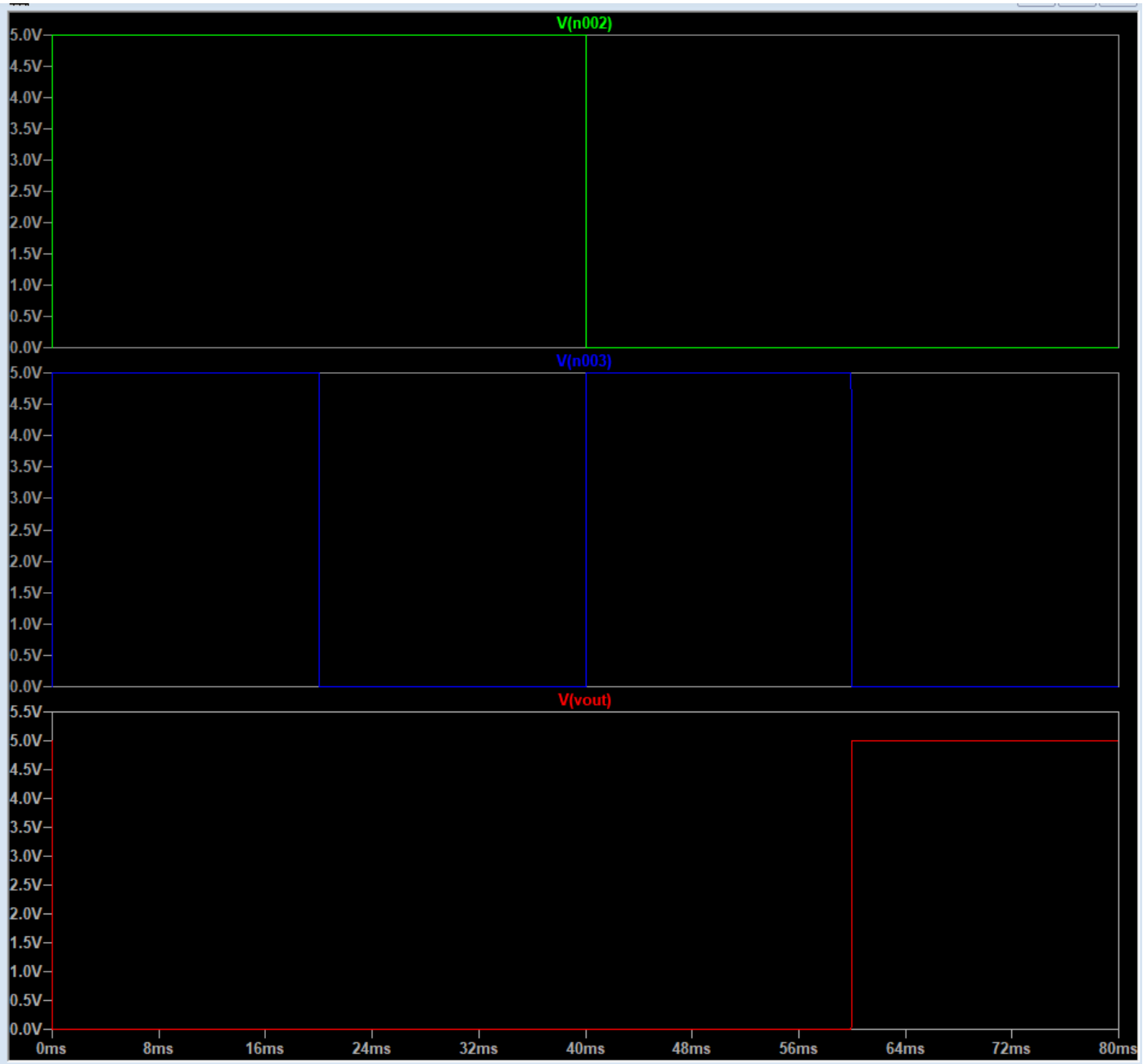

Fig: Simulation result (Waveform) of CMOS NOR logic gate. Blue & green signals are the input signals while red signal is the output signal.

Real world applications:

Some of the real world applications of CMOS NOR logic gate circuits are:

1. Mixer tank.
2. In combinational circuits like half and full adders, etc.

08 : NAND Logic Gate

Application of the diode:

NAND logic gate is made up of two pMOS and two nMOS connected in parallel and series respectively. Here three voltage sources are used namely V1, V2 and V3.

It also gives output only in the form of high or low signals. It returns low only when both the input signals (V1 and V2) are high and in all other cases it returns high.

Circuit diagram:

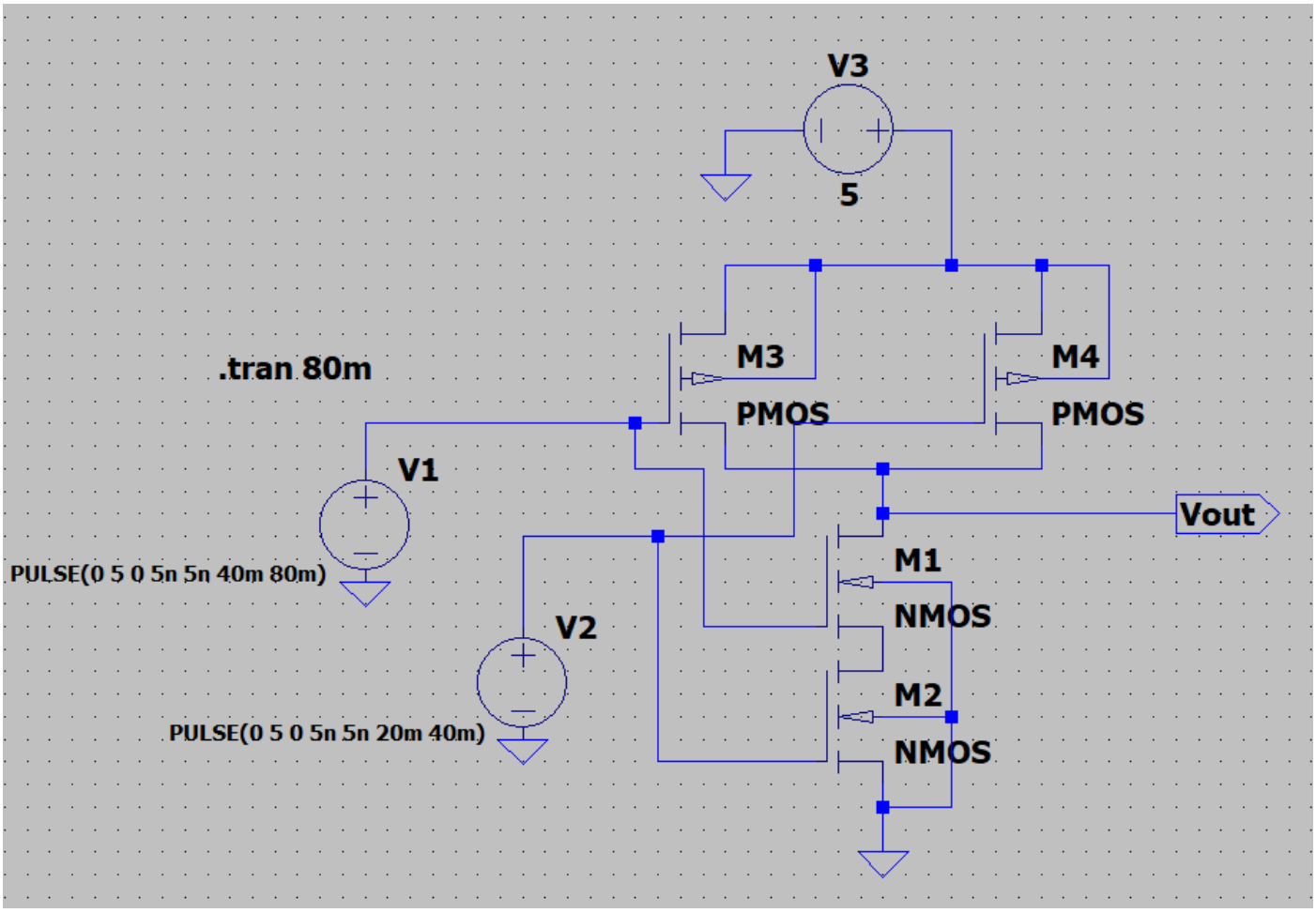

Fig: Simulation result (Waveform) of Voltage doubler circuit. Blue and green signals are the output and input signal respectively.

Circuit operation:

Considering the two level inputs from two input sources, there can be four cases of input as stated below:

Case-1 : V1 – Low & V2 – Low

As V1 and V2 both are low, both the pMOS will be ON and both the nMOS will be OFF. So the output V_{out} will get two paths through two ON pMOS to get connected with V_{dd}. The output will be charged to the V_{dd} level. The output line will not get any path to the ground as both the nMOS are off. So, there is no path through which the output line can discharge. The output line will maintain the voltage level at V_{dd}; so, High.

Case-2 : V1 – Low & V2 – High

V1 – Low: pMOS1 – ON & nMOS1 – OFF

V2 – High: pMOS2 – OFF & nMOS2 – ON

pMOS1 and pMOS2 are in parallel. Though pMOS2 is OFF, still the output line will get a path through pMOS1 to get connected with V_{dd}. nMOS1 and nMOS2 are in series. As nMOS1 is OFF, so V_{out} will not be able to find a path to ground to get discharged. This in turn results the V_{out} to be maintained at the level of V_{dd}; so, High.

Case-3 : V1 – High & V2 – Low

V1 – High: pMOS1 – OFF & nMOS1 – ON

V2 – Low: pMOS2 – ON & nMOS2 – OFF

The explanation is similar as Case-2. V_{out} level will be High.

Case-4 : V1 – High & V2 – High

V1 – High: pMOS1 – OFF & nMOS1 – ON

V2 – High: pMOS2 – OFF & nMOS2 – ON

In this case, both the pMOS are OFF. So, V_{out} will not find any path to get connected with V_{dd}. As both the nMOS are ON, the series connected nMOS will create a path from V_{out} to ground. Since, the path to ground is established, V_{out} will be discharged; so, Low.

Expected results:

We expect to see a wave form which is low only when both the inputs are high otherwise the output is always high. This expected result can be better visualised with the help of a truth table:

V1	V2	Vout
0	0	1
0	1	1
1	0	1
1	1	0

Simulation results:

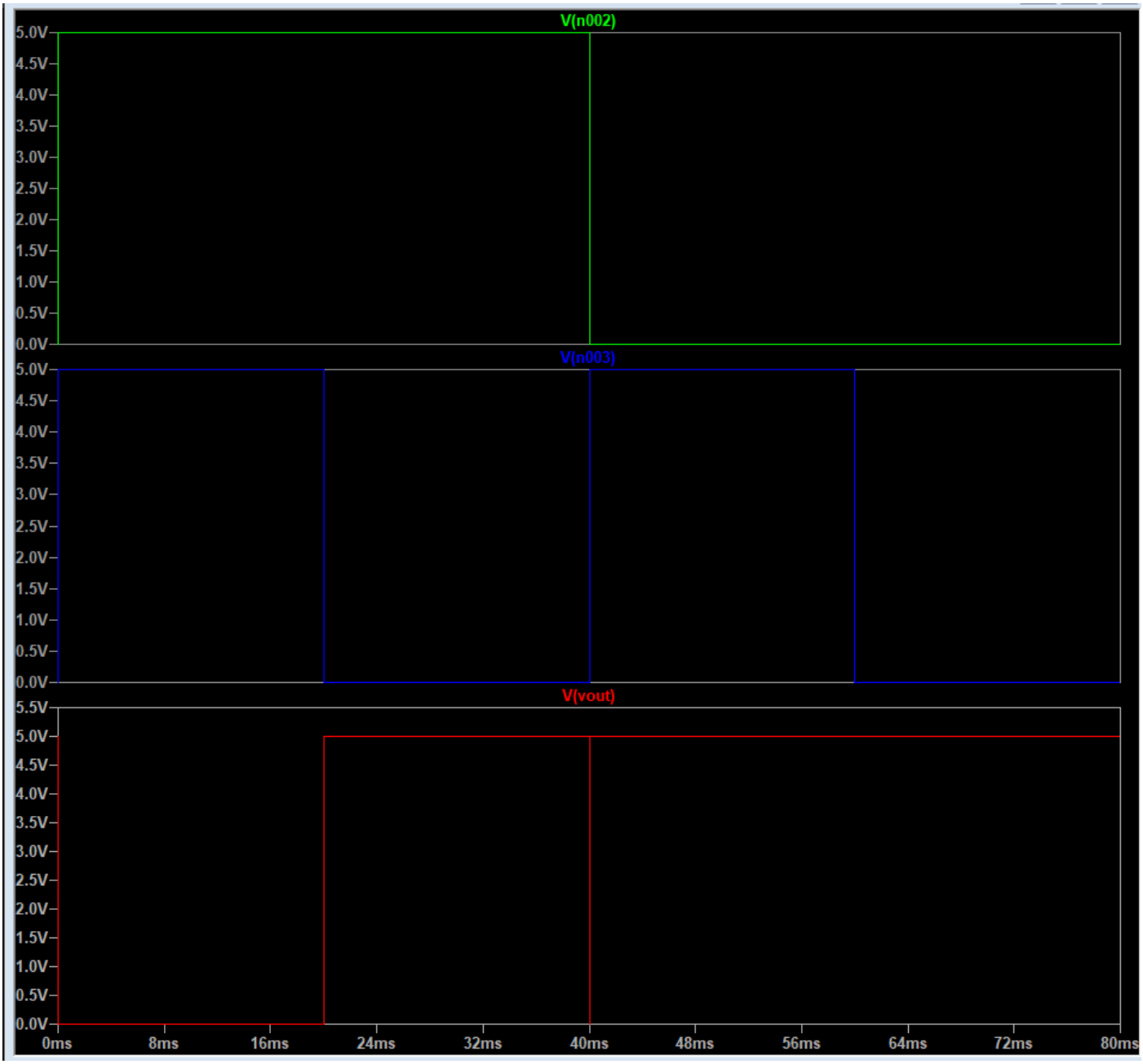

Fig: Simulation result (Waveform) of CMOS NAND logic gate. Blue and green signals are the input signals while the red signal is the output signal.

Real world applications:

Some of the real world applications of CMOS NAND logic gate circuits are:

3. Burglar or theft alarm.
4. Automatic watering system.
5. Light activated theft alarm, etc.