Lab Report: MOSFET Characteristics
Hardware Experiment - 3

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Title of the Experiment: Study the characteristics of enhancement-type MOSFETs.

Objective: The aim of this experiment is to plot:
(i) The output characteristics,
(ii) The transfer characteristics of n and p-channel enhancement-type MOSFETs, and
(iii) The voltage transfer characteristics (VTC) of a CMOS inverter by connecting the n-MOSFET and p-MOSFET.

Apparatus: The equipment or apparatus required for the experiment are:
(i) MOSFET n-type (IRFZ44N) and p-type (IRFZ9540)
(ii) Breadboard
(iii) Resistors (1KΩ)
(iv) Connecting wires
(v) Ammeters (0-10mA/ 0-25mA)
(vi) DC power supply (0-12V) and,
(vii) Multimeter.

1. Output and Transfer Characteristics of NMOS and PMOS

Circuit Diagram:

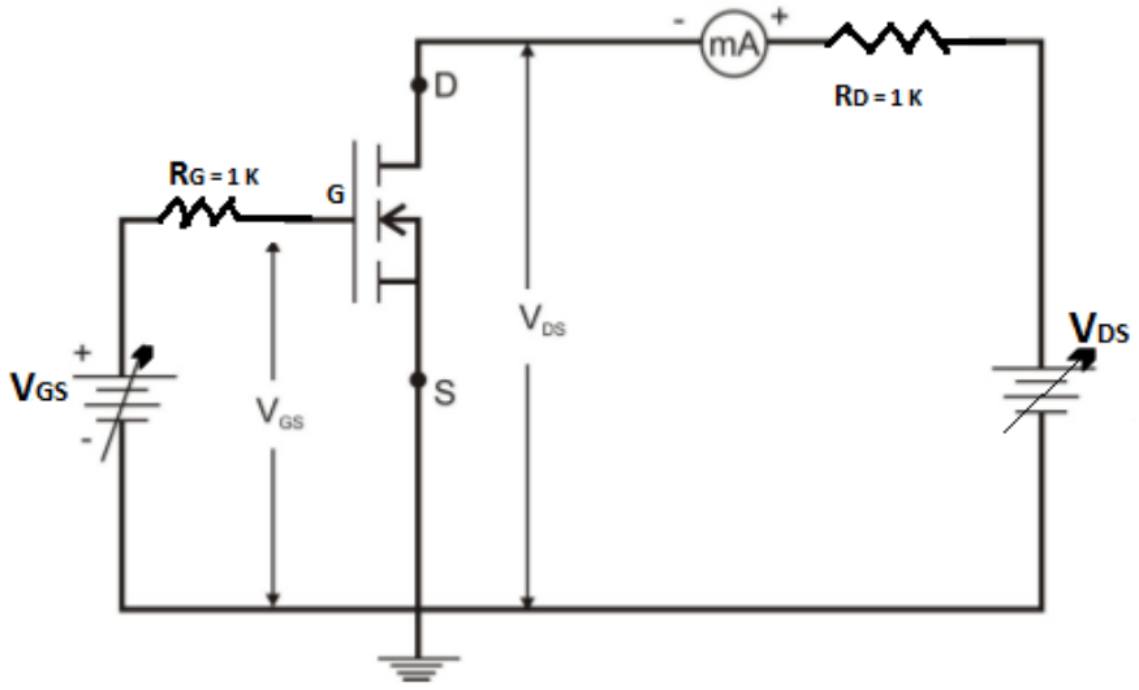


Fig.: Circuit diagram of MOSFET Characteristics

Theory: Here are a few important points about MOSFETs:

- Cut-Off Region: Cut-off region is a region in which the MOSFET will be OFF as there will be negligible current flow through it.
- Ohmic or Linear Region: Ohmic or linear region is a region wherein the current ID increases with an increase in the value of VDS.
- Saturation Region: In the saturation region, the drain current ID is quite constant irrespective of an increase in VDS.

We can represent the above facts into a tabular form as:

MOSFET	**Cut-Off**	**Ohmic/Linear**	**Saturation**
n-channel Enhancement-type	$V_{GS} < V_T$	$V_{GS} > V_T$ and $V_{DS} < V_{GS} - V_T$	$V_{GS} > V_T$ and $V_{DS} < V_{GS} - V_T$
p-channel Enhancement-type	$V_{GS} > -V_T$	$V_{GS} < -V_T$ and $V_{DS} > V_{GS} - V_T$	$V_{GS} < -V_T$ and $V_{DS} < V_{GS} - V_T$

Procedure: Only for Practical application of the circuits in the Laboratory.

I. Output Characteristics: V_{DS} vs I_D for different V_{GS}.

1. Connect the circuit as per the given diagram properly.
2. Keep V_{GS} constant to 1V and sweep V_{DS} and take readings of I_D. Vary V_{DS} in the step of 1V up to 11V and measure the drain currents I_D. Tabulate all the readings.
3. Repeat the above procedure for V_{GS} as 2.5 V, 3 V, 3.5 V, 4 V, 4.5 V and 5 V.
4. Plot the output characteristics V_{DS} vs I_D (for different values of V_{GS}).

II. Transfer Characteristics: V_{GS} vs. I_D for different V_{DS}.

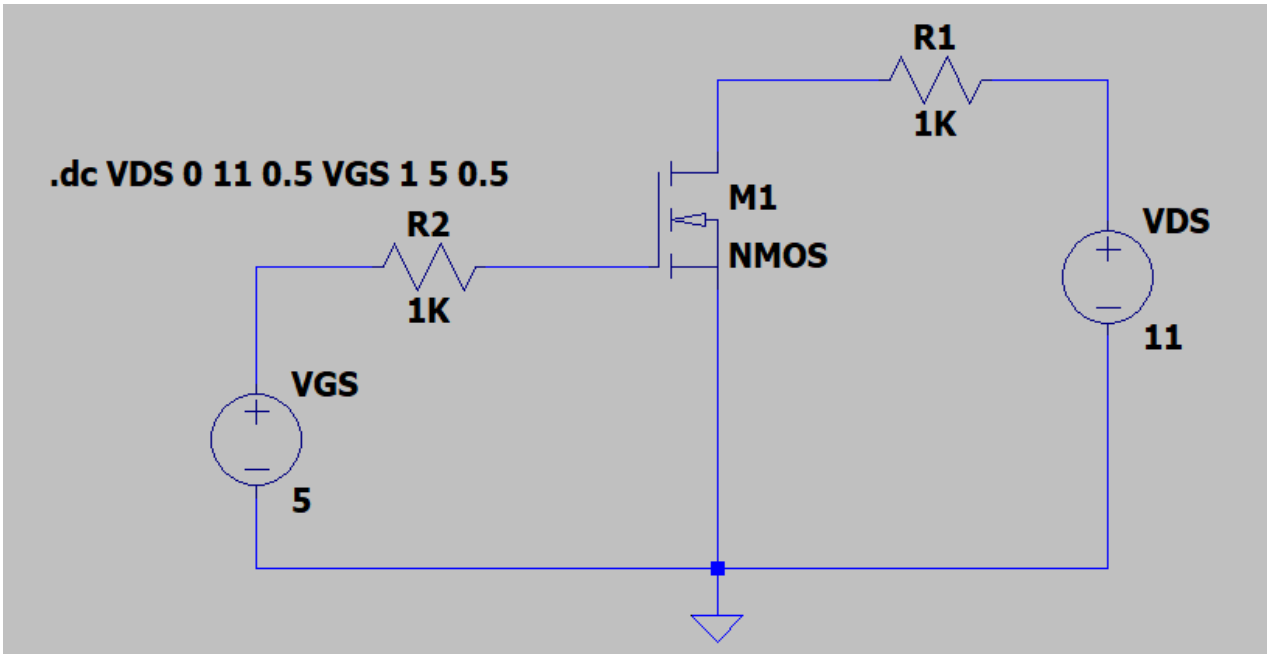
1. Connect the circuit as per the given diagram properly.
2. Set the voltage V_{DS} constant at 3 V, 8 V and 11 V.
3. Vary V_{GS} in the step of 0.5 V from 0 to 11 V and note down the value of drain currents I_D. Tabulate all the readings.
4. Plot the transfer characteristics V_{GS} vs I_D.
5. Calculate V_T, g_m from the graphs and verify it from the datasheet.

Here, I have computed the output and transfer characteristics of both NMOS and PMOS using practical methods and LTSpice software.

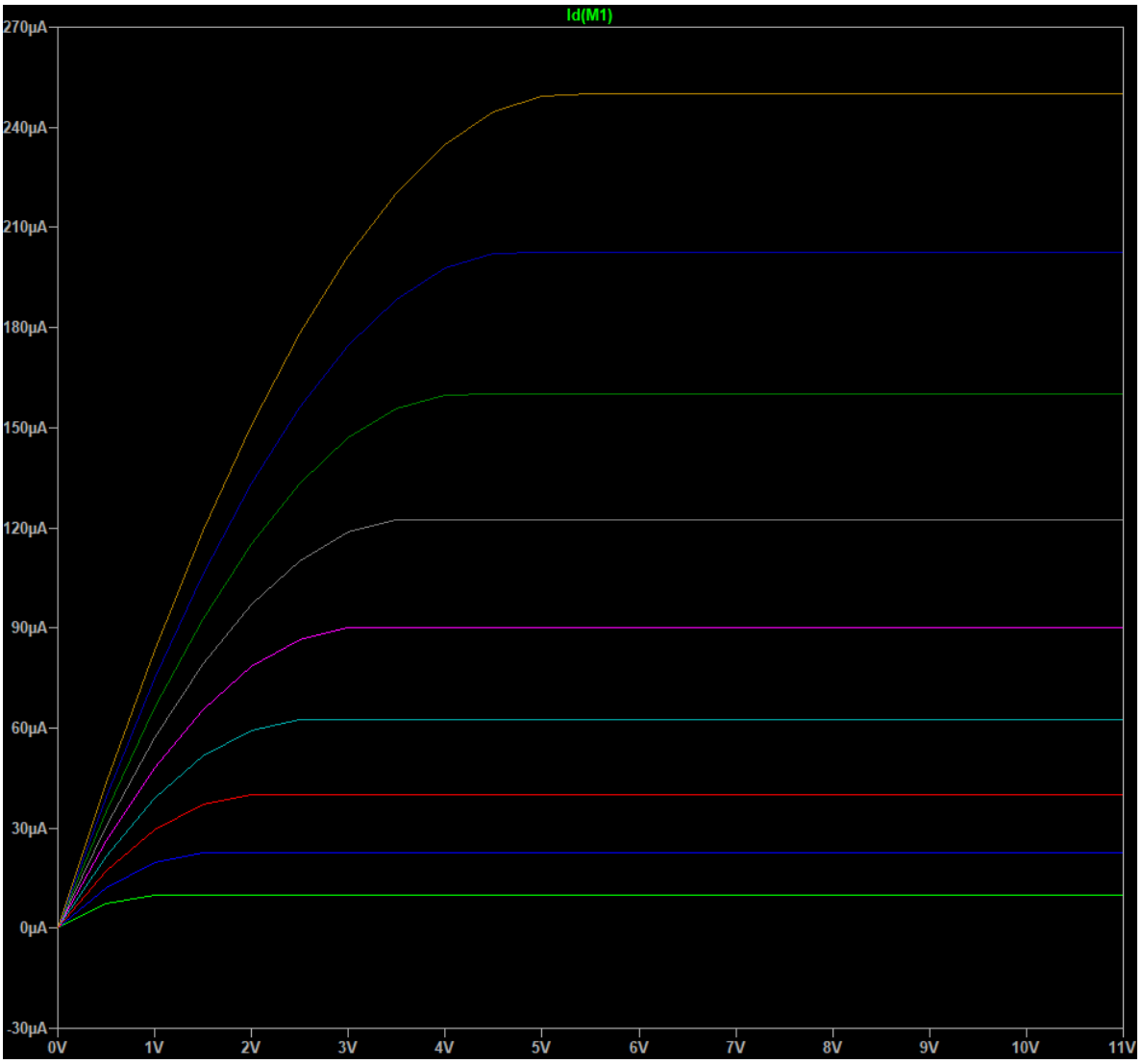
1.A. Output Characteristics of NMOS

- **In LTSpice:**

Circuit diagram:



Graph:



- **Practical with Data**

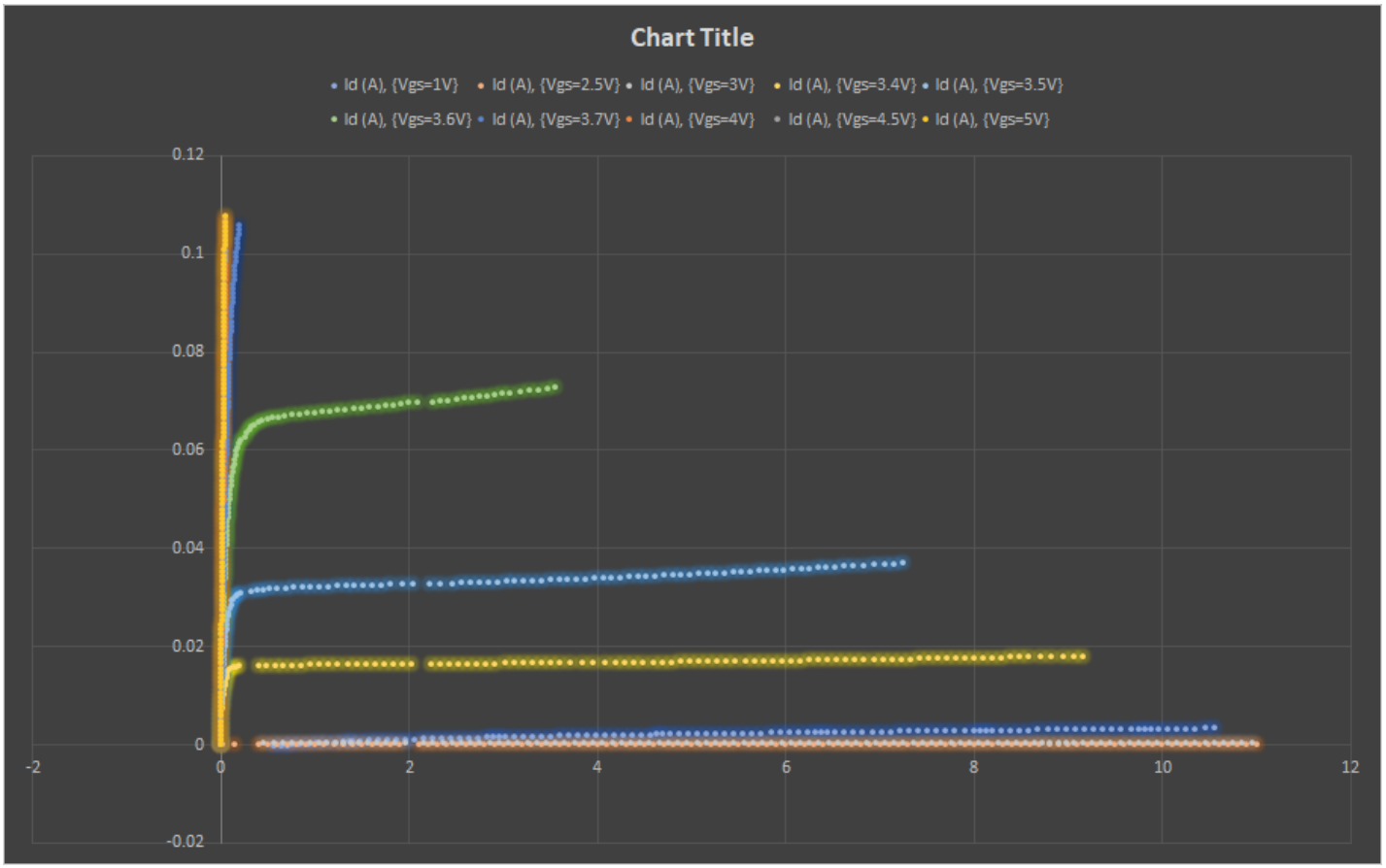
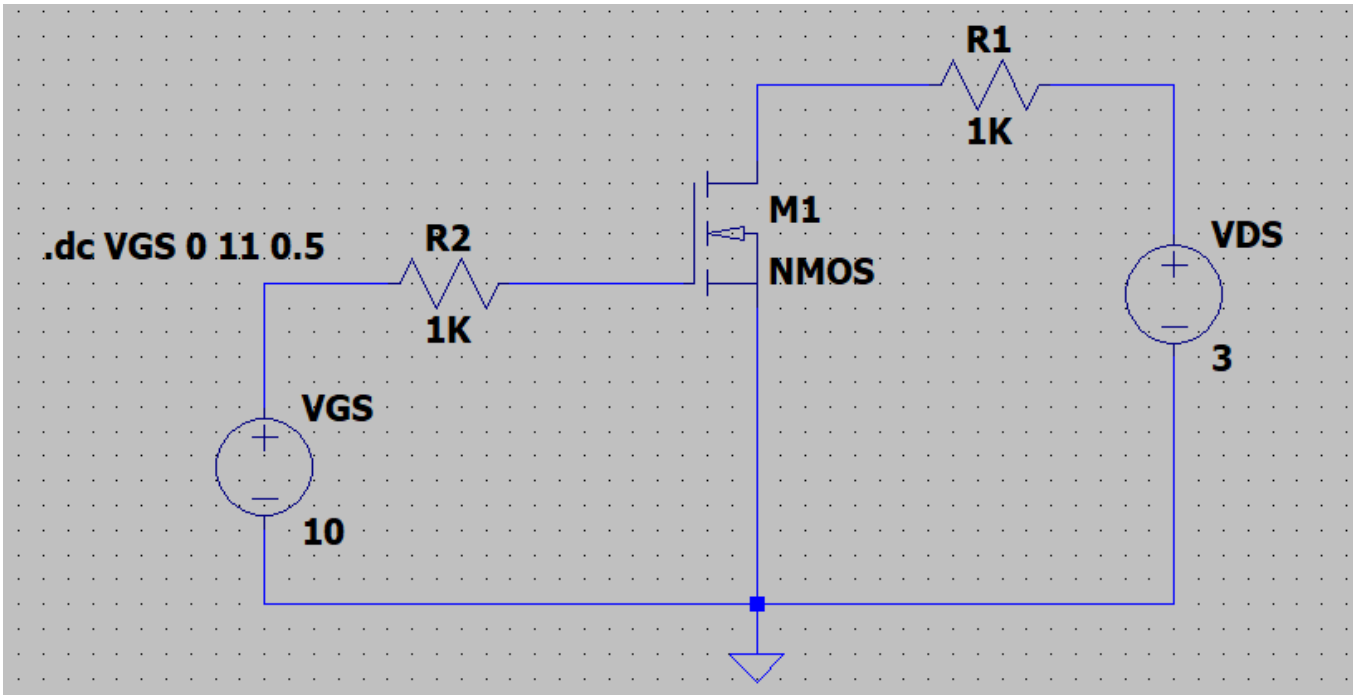


Fig.: Output characteristics of NMOS

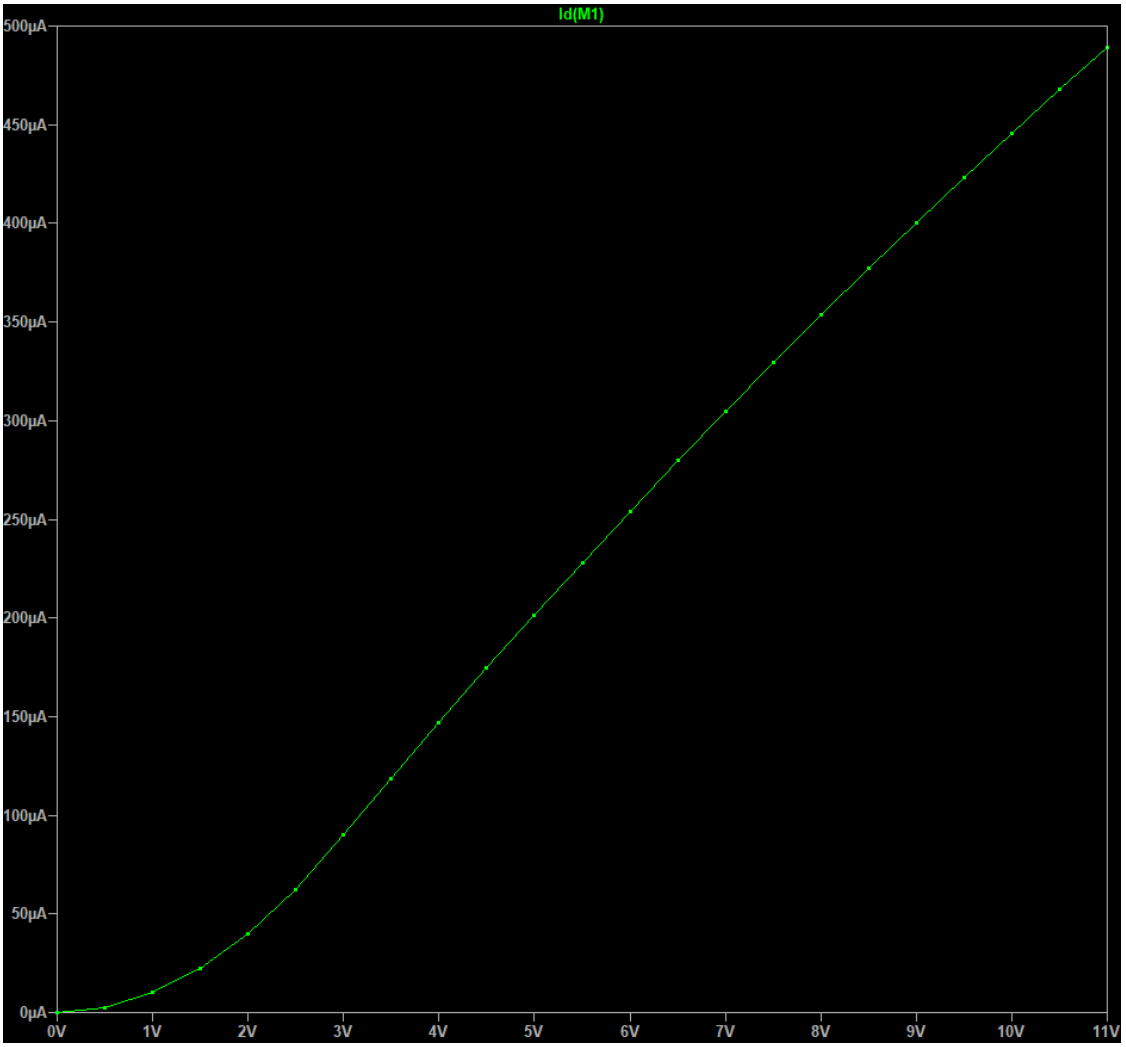
1.B. Transfer Characteristics of NMOS

- **In LTSpice:**

Circuit:



Graph:



- **Practical with Data**

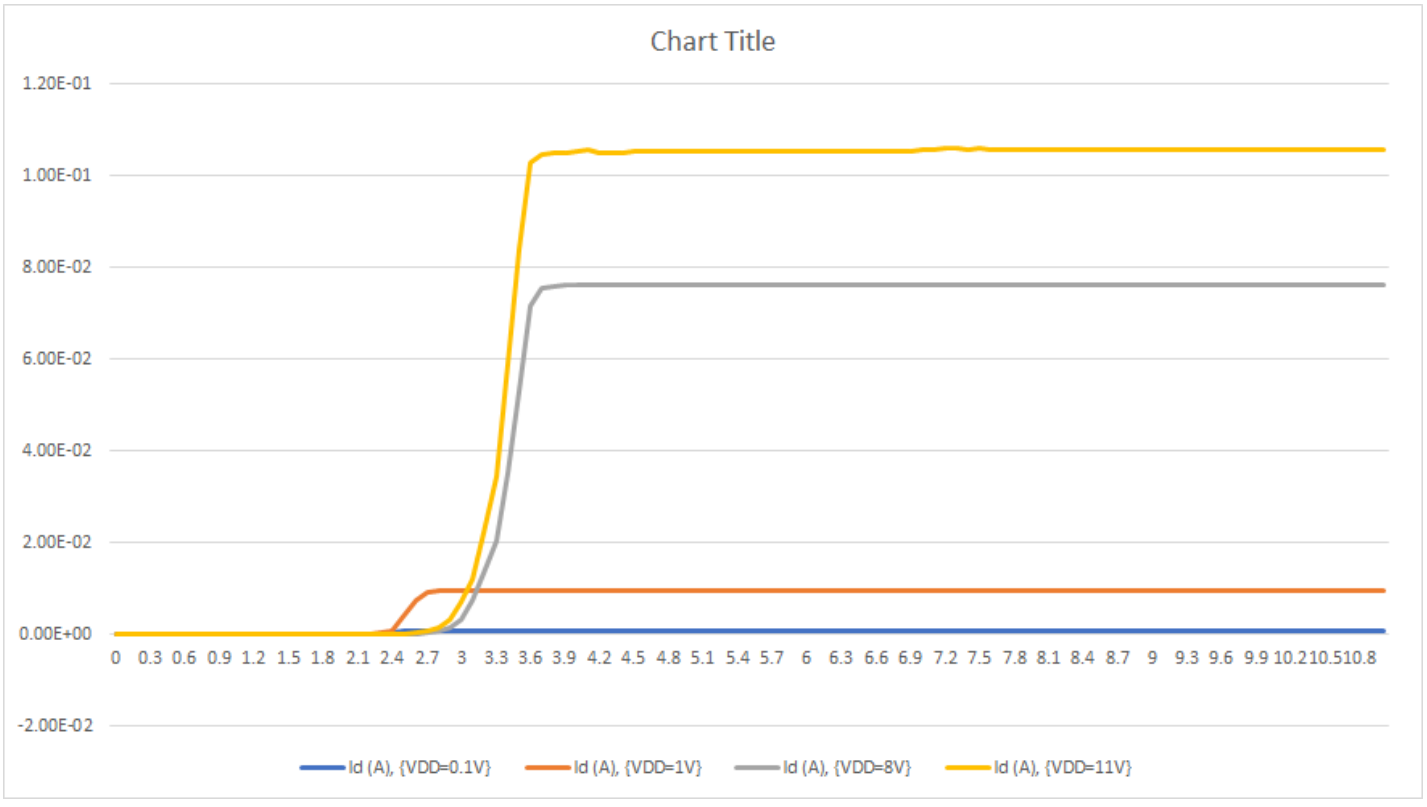
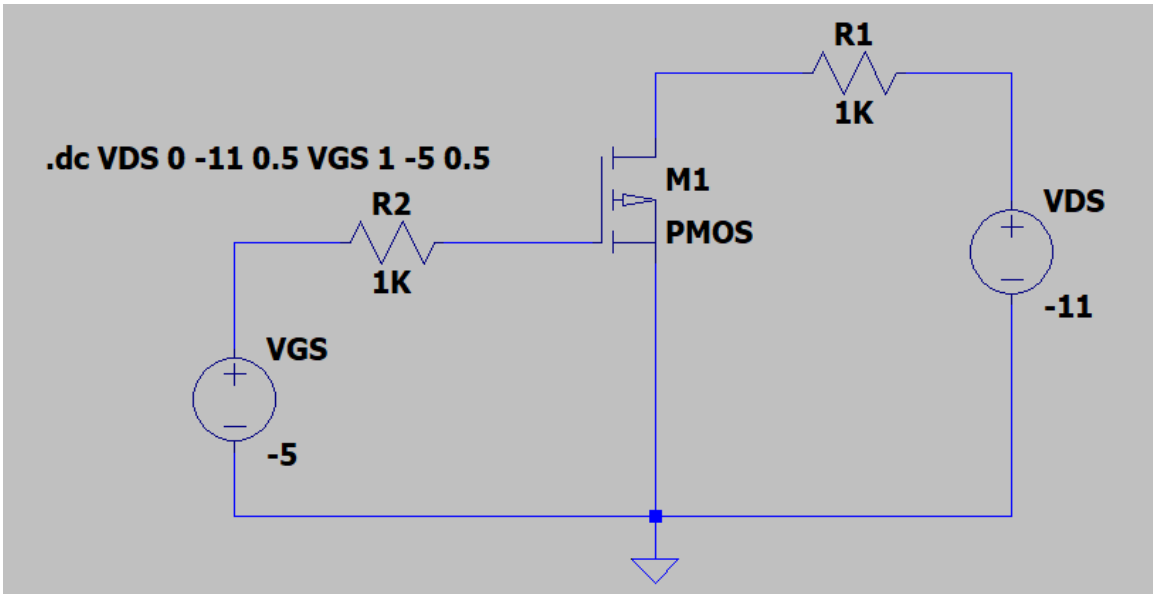


Fig.: Transfer characteristics of NMOS

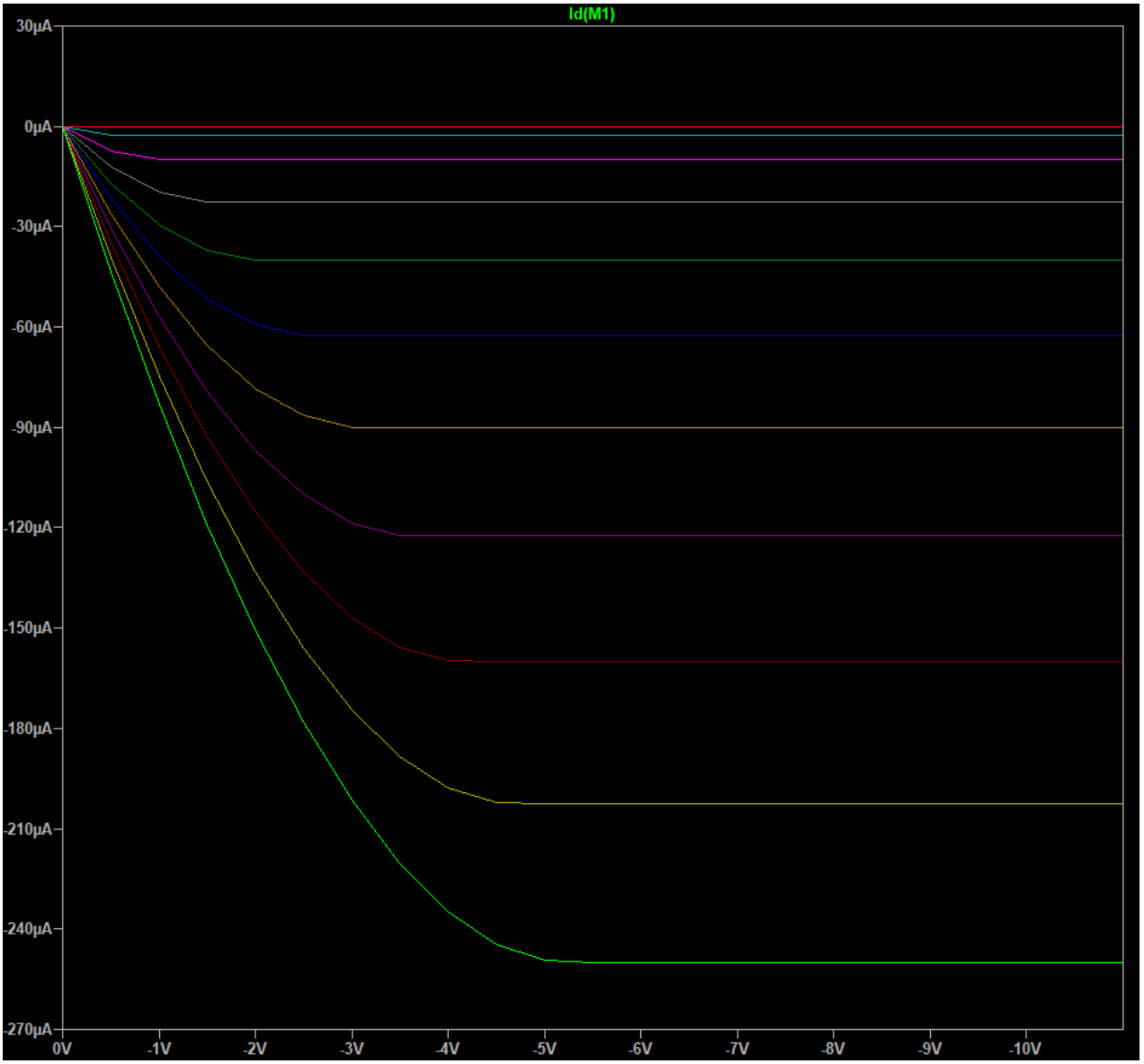
2.A. Output Characteristics of PMOS

- In LTSpice

Circuit:



Graph:



- **Practical with Data**

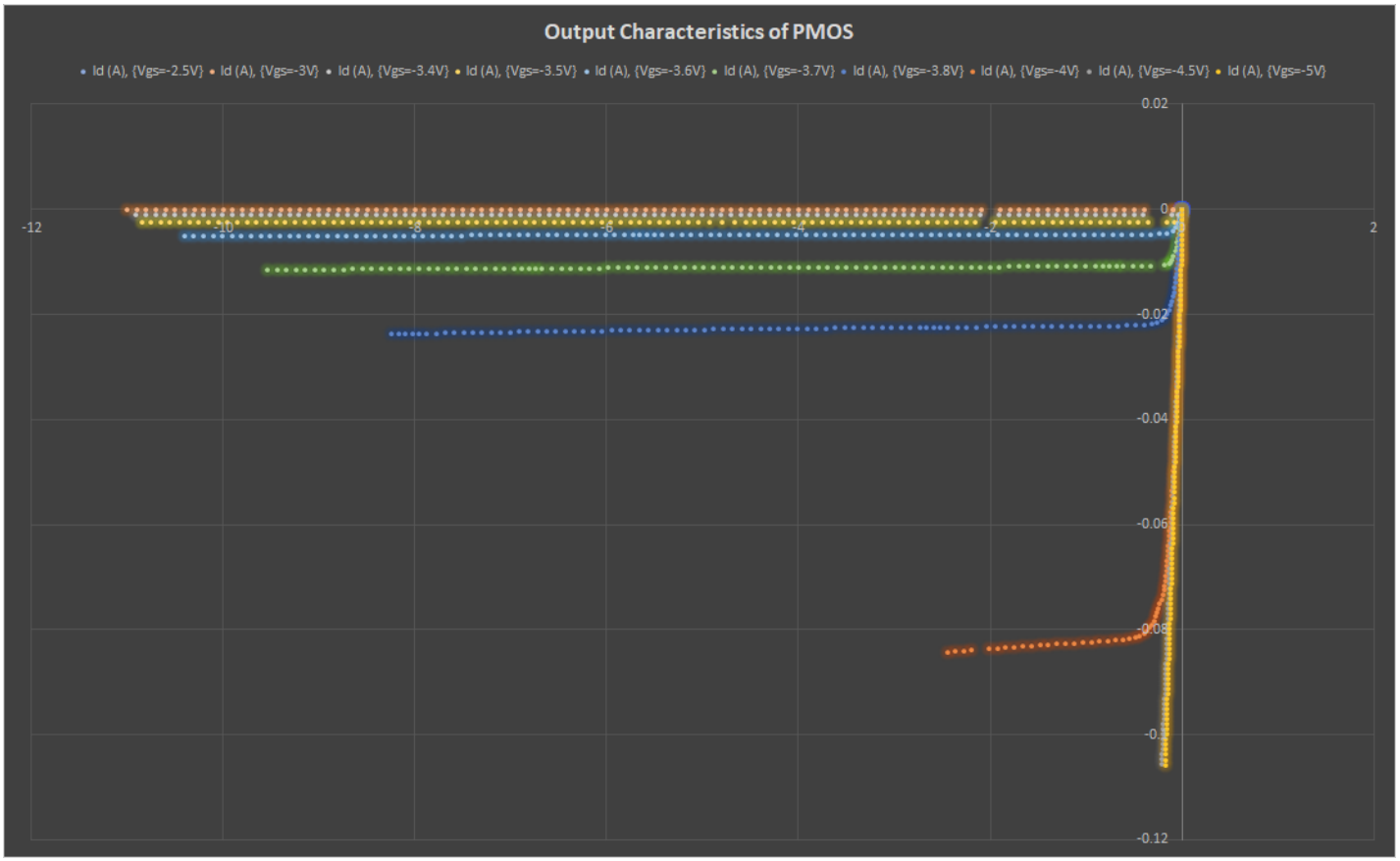
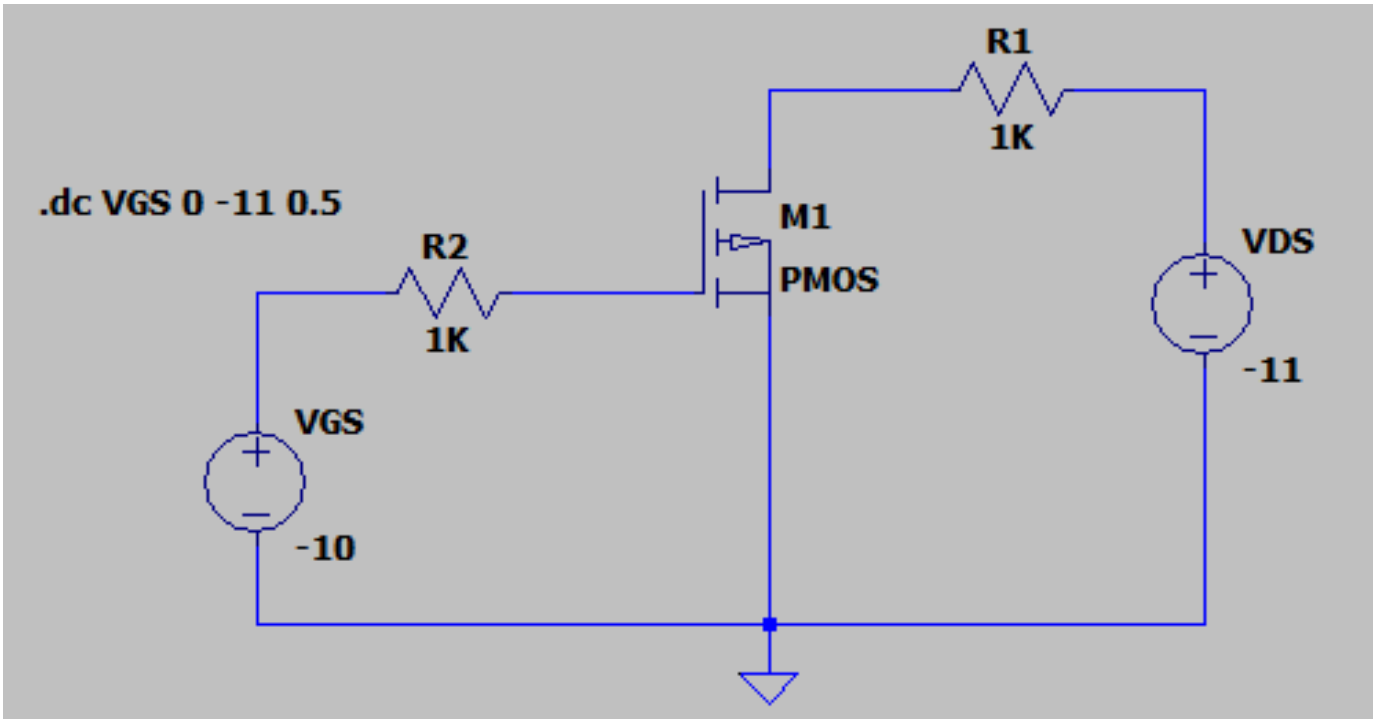


Fig.: Output characteristics of PMOS

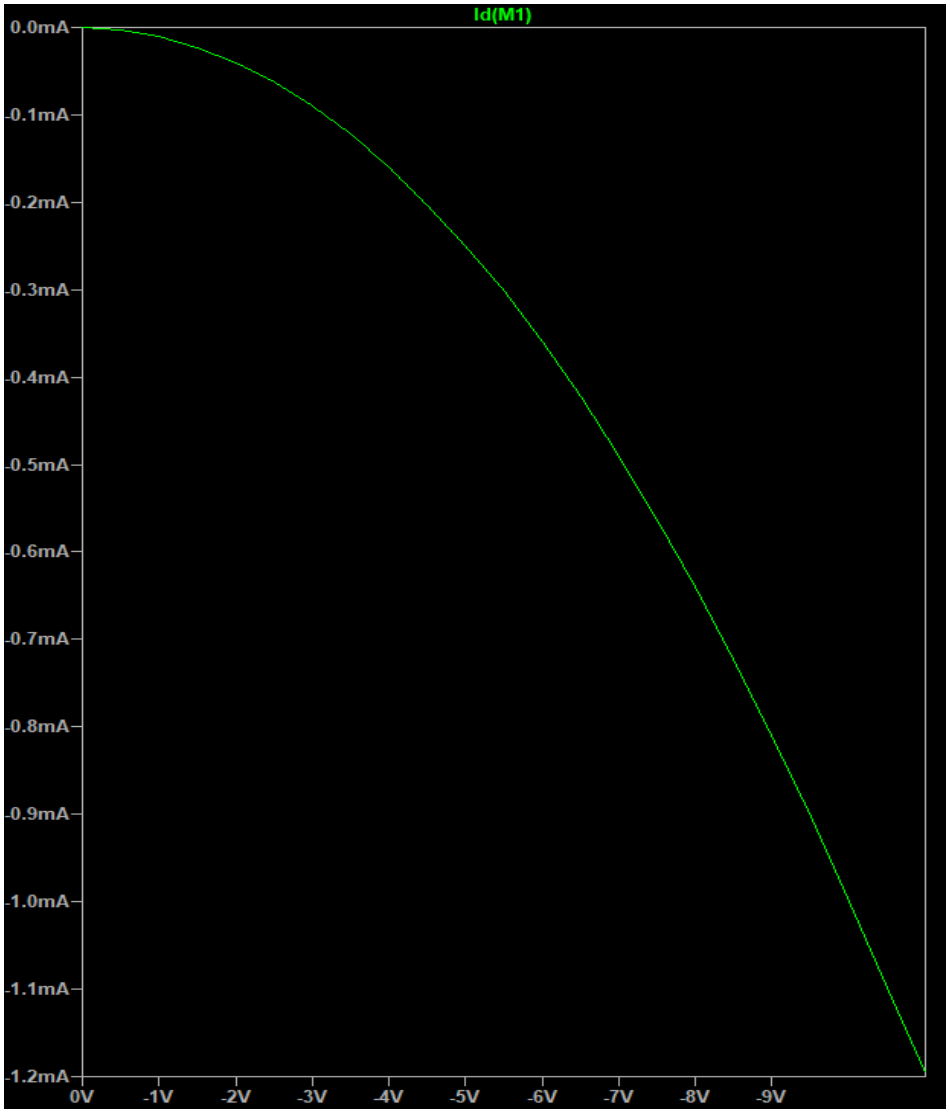
2.B. Transfer Characteristics of PMOS

- **In LTSpice**

Circuit:



Graph:



- **Practical with Data**

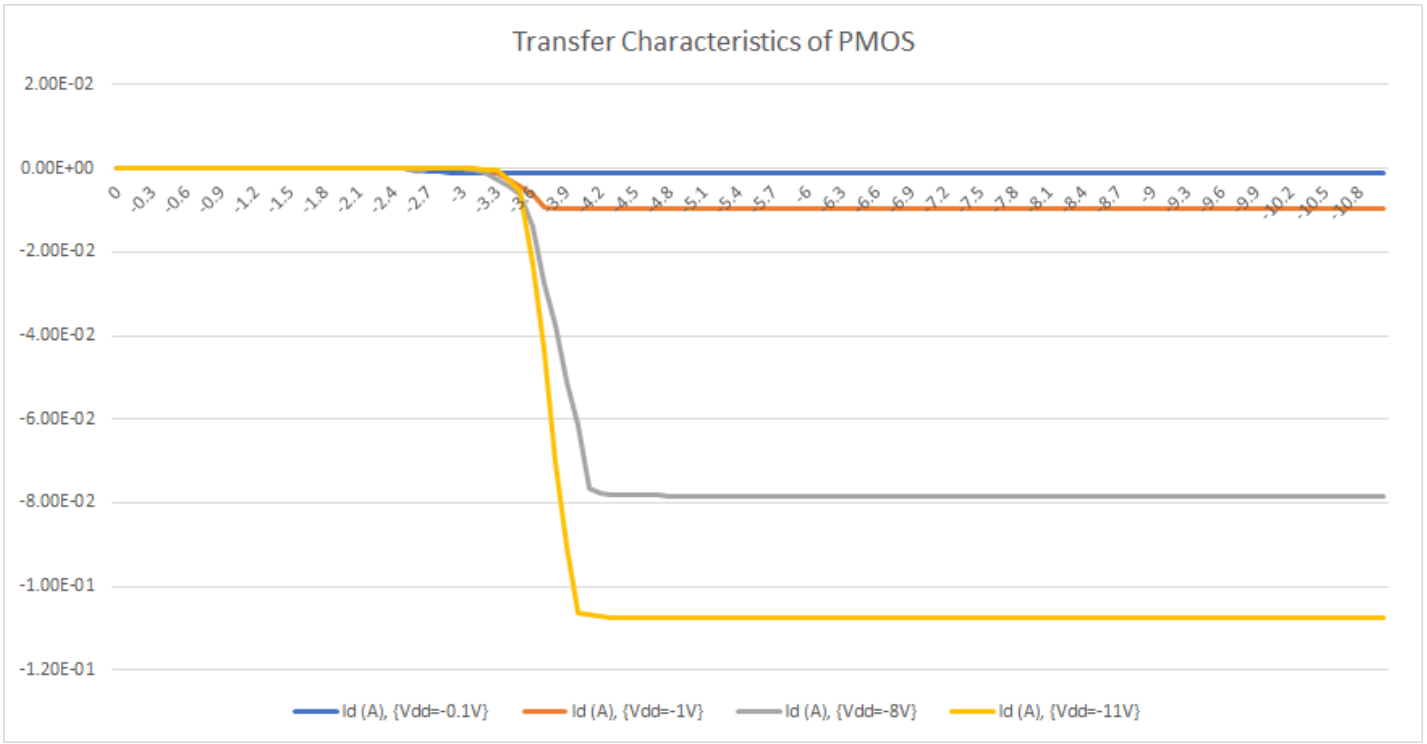


Fig.: Transfer characteristics of PMOS

Calculations: Here I have calculated some important parameters for both NMOS and PMOS.

1. **Threshold voltage (V_T) =** Gate to source voltage at which drain current starts flowing.
2. **Transconductance (g_m) =** Ratio of small change in drain current (ΔI_D) to the corresponding change in gate to source voltage (ΔV_{GS}) for a constant V_{DS}.
3. **Output drain resistance (r_0) =** It is given by the relation of small change in drain to source voltage (ΔV_{DS}) to the corresponding change in Drain Current (ΔI_D) for a constant V_{GS}.

Result:

	V_T	g_m	r_0
PMOS	-2.5V	3.11 millisiemens	10.827 Ohm
NMOS	2.2V	1.74 millisiemens	0.477 Ohm

3. Voltage Transfer Characteristics of a CMOS inverter

Theory: A CMOS inverter consists of a PMOS and an NMOS transistor connected in series. The drain and gate terminals of the two transistors are connected. The supply voltage VDD is connected to the PMOS source terminal and the NMOS source terminal is connected to ground. The voltage Vin is applied at the gate terminals and Vout is the output voltage at the drain terminals. The input/output characteristics of a CMOS inverter is called voltage transfer characteristics and it has a sharp transition region, which makes it energy-efficient during switching between low and high voltage levels. At low input voltage circuit output high voltage and vice-versa, thereby it acts as an inverter.

Circuit diagram:

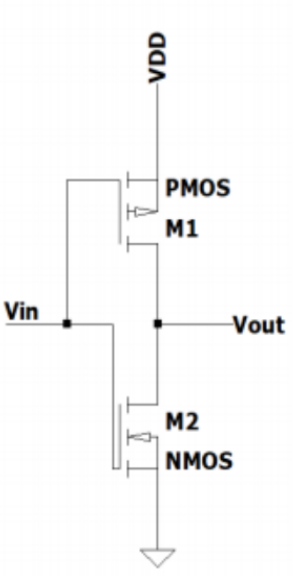
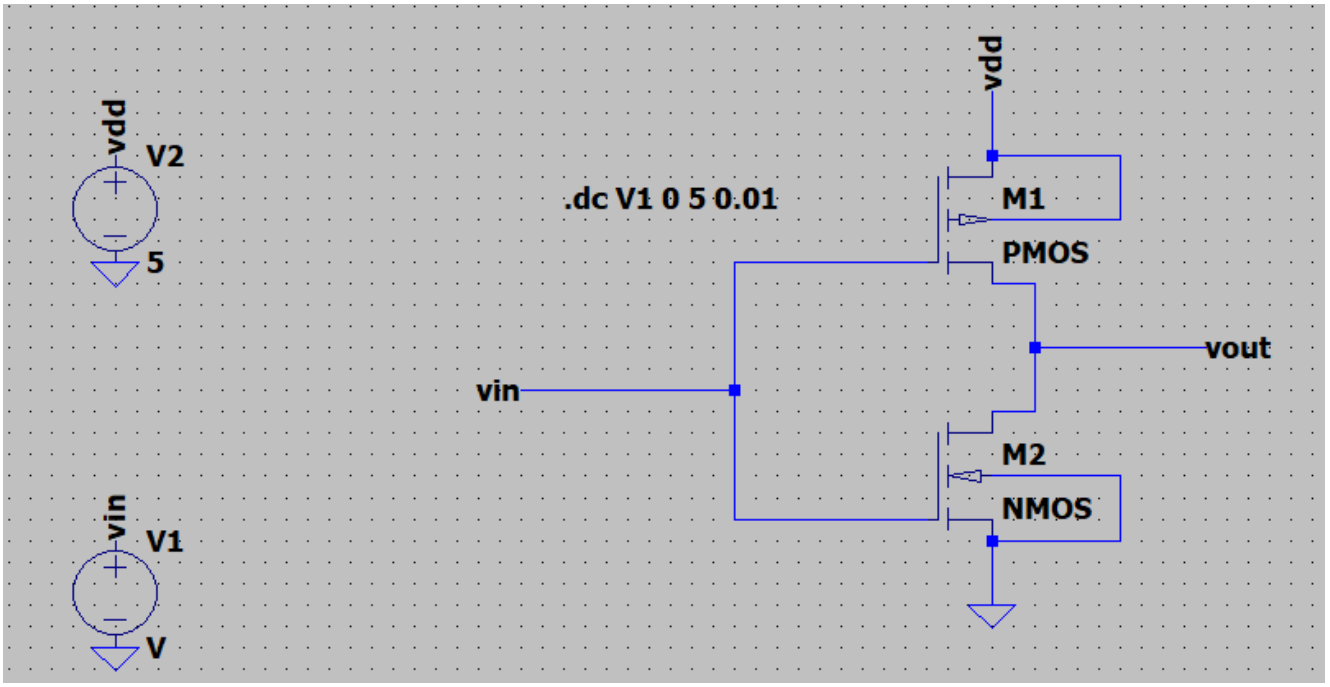


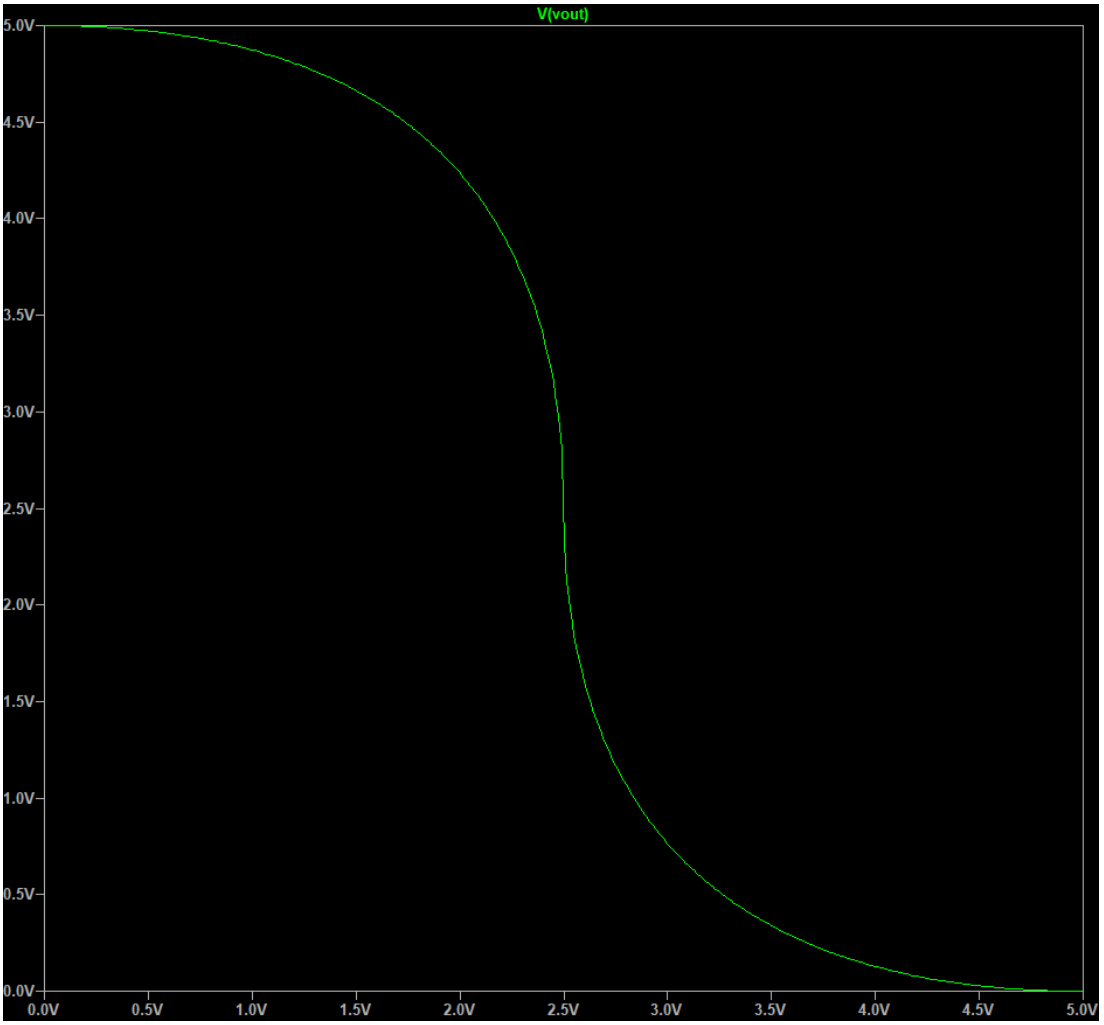
Figure 3: CMOS inverter

- **In LTSpice**

Circuit:



Graph:



- **Practical with Data**

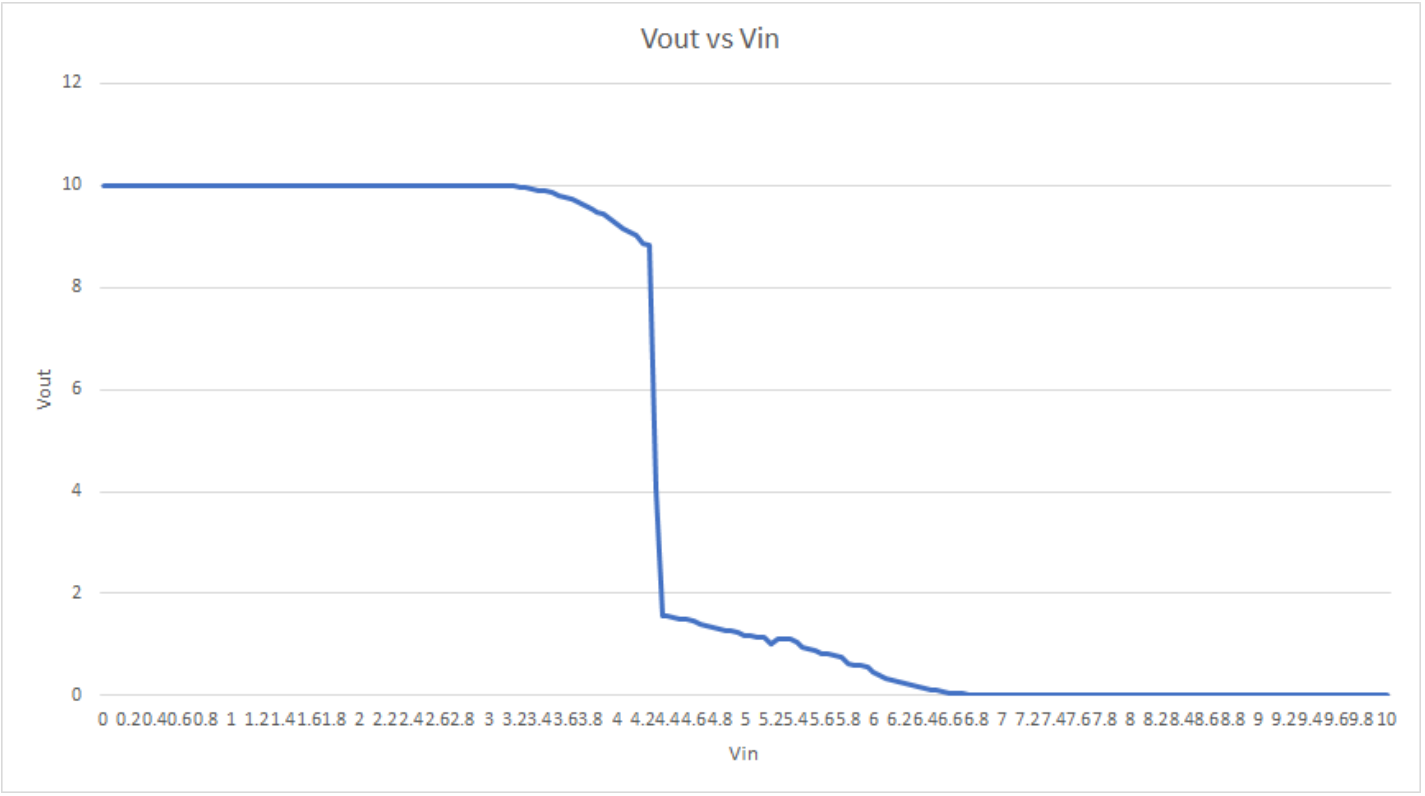


Fig.: Voltage transfer characteristics of CMOS inverter