REVISION HISTORY

Revision	Description	Date	Drawn	Checked
Ver 2.0	Initial Version	2017-11-27	HJ	

Schematics Index:

Xunlong Software Co.,Limited
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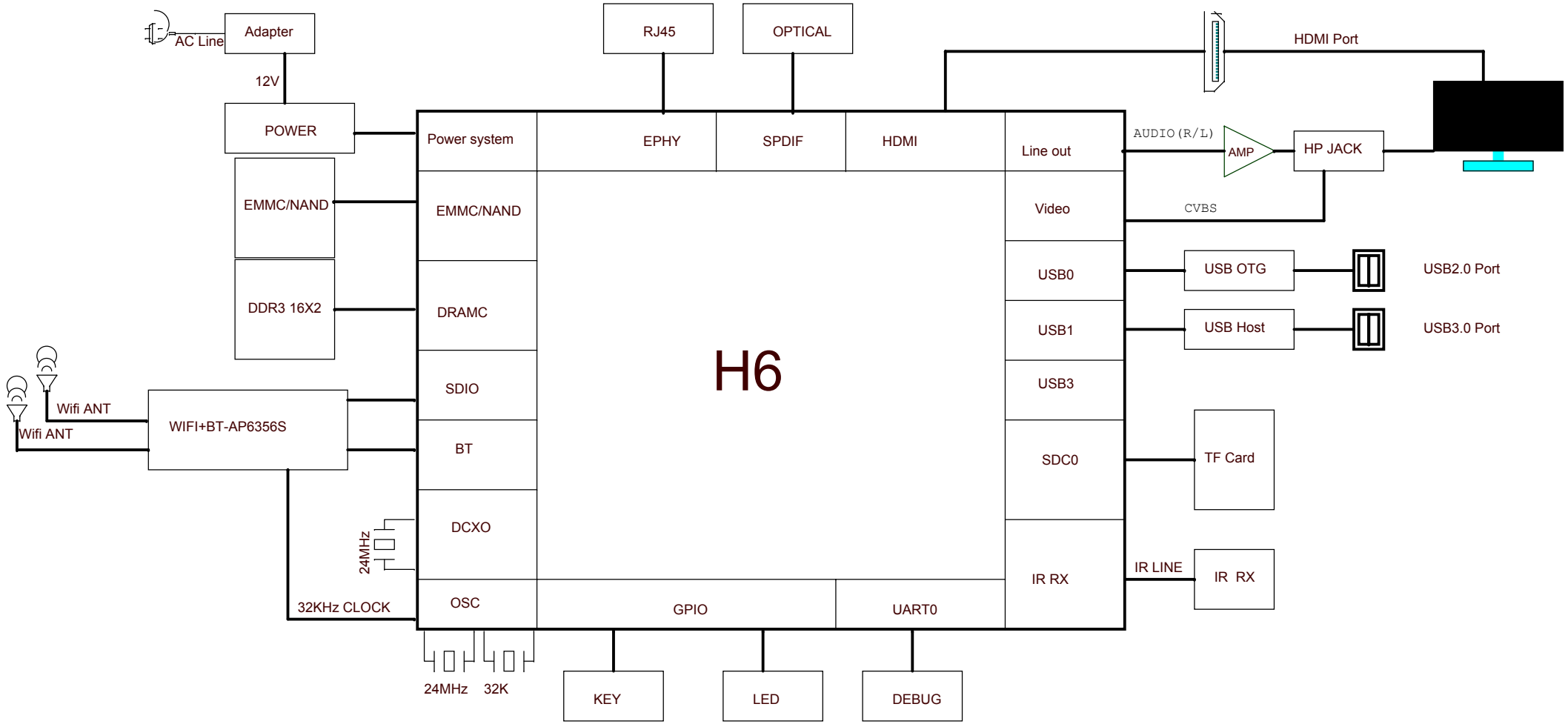
BLOCK



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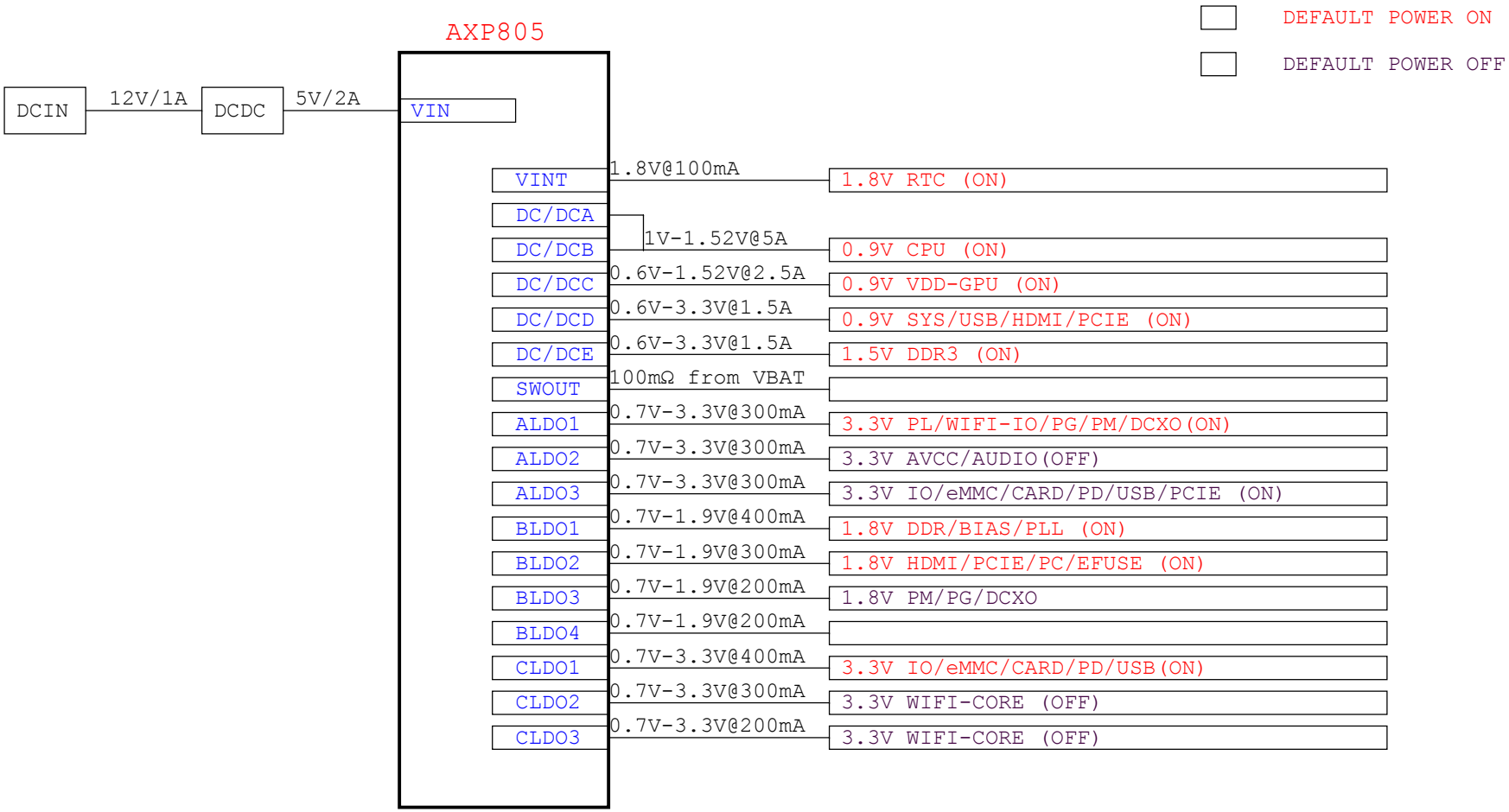
POWER TREE



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GPIO ASSIGNMENT

PIN	Define	CFG	Function
PC0	NAND_WE	2	NAND/eMMC
PC1	NAND_ALE/SDC2_DS	2/3	
PC2	NAND_CLE	2	
PC3	NAND_CE0	2	
PC4	NAND_RE/SDC2_CLK	2/3	
PC5	NAND_RB0/SDC2_CMD	2/3	
PC6	NAND_DQ0/SDC2_D0	2/3	
PC7	NAND_DQ1/SDC2_D1	2/3	
PC8	NAND_DQ2/SDC2_D2	2/3	
PC9	NAND_DQ3/SDC2_D3	2/3	
PC10	NAND_DQ4/SDC2_D4	2/3	
PC11	NAND_DQ5/SDC2_D5	2/3	
PC12	NAND_DQ6/SDC2_D6	2/3	
PC13	NAND_DQ7/SDC2_D7	2/3	
PC14	NAND_DQS/SDC2_RST	2/3	
PC15	NAND_CE1	2	
PC16	NAND_RB1	2	

PIN	Define	CFG	Function
PD0			
PD1			
PD2			
PD3			
PD4			
PD5			
PD6			
PD7			
PD8			
PD9			
PD10			
PD11			
PD12			
PD13			
PD14			

PIN	Define	CFG	Function
PD15			
PD16			
PD17			
PD18			
PD19			
PD20			
PD21			
PD22			
PD23			
PD24			
PD25			
PD26			

PIN	Define	CFG	Function
PG0	SDC1_CLK	2	WIFI+BT
PG1	SDC1_CMD	2	
PG2	SDC1_D0	2	
PG3	SDC1_D1	2	
PG4	SDC1_D2	2	
PG5	SDC1_D3	2	
PG6	UART1_TX	2	
PG7	UART1_RX	2	
PG8	UART1_RTS	2	
PG9	UART1_CTS	2	
PG10	PCM2_SYNC	2	
PG11	PCM2_CLK	2	
PG12	PCM2_DOUT	2	
PG13	PCM2_DIN	2	
PG14			

PIN	Define	CFG	Function
PF0	SDC0_D1	2	CARD0
PF1	SDC0_D0	2	
PF2	SDC0_CLK/UART0_TX	2/3	
PF3	SDC0_CMD	2	
PF4	SDC0_D3/UART0_RX	2/3	
PF5	SDC0_D2	2	
PF6	SDC0-DET	2	

PIN	Define	CFG	Function
PH0	CPUX-UTX	2	
PH1	CPUX-URX	2	
PH2			
PH3			
PH4			
PH5			
PH6			
PH7	SPDIF_OUT	3	
PH8	HSCL	2	HDMI
PH9	HSDA	2	
PH10	HCEC	2	

PIN	Define	CFG	Function
PL0	PMU-SCK	3	
PL1	PMU-SDA	3	
PL2	RECOVERY	2	
PL3	LINK-LED	1	
PL4	PWR-LED	1	
PL5	USB0-DRVVBUS	1	
PL6	MUTE	1	
PL7	STATUS-LED	1	
PL8			
PL9	IR-RX	2	
PL10	BT-WIFI-ON	1	
PM0	WL-WAKE-AP	0	WIFI+BT
PM1	BT-WAKE-AP	0	
PM2	AP-WAKE-BT	1	
PM3	WL-REG-ON	1	
PM4	BT-REG-ON	1	

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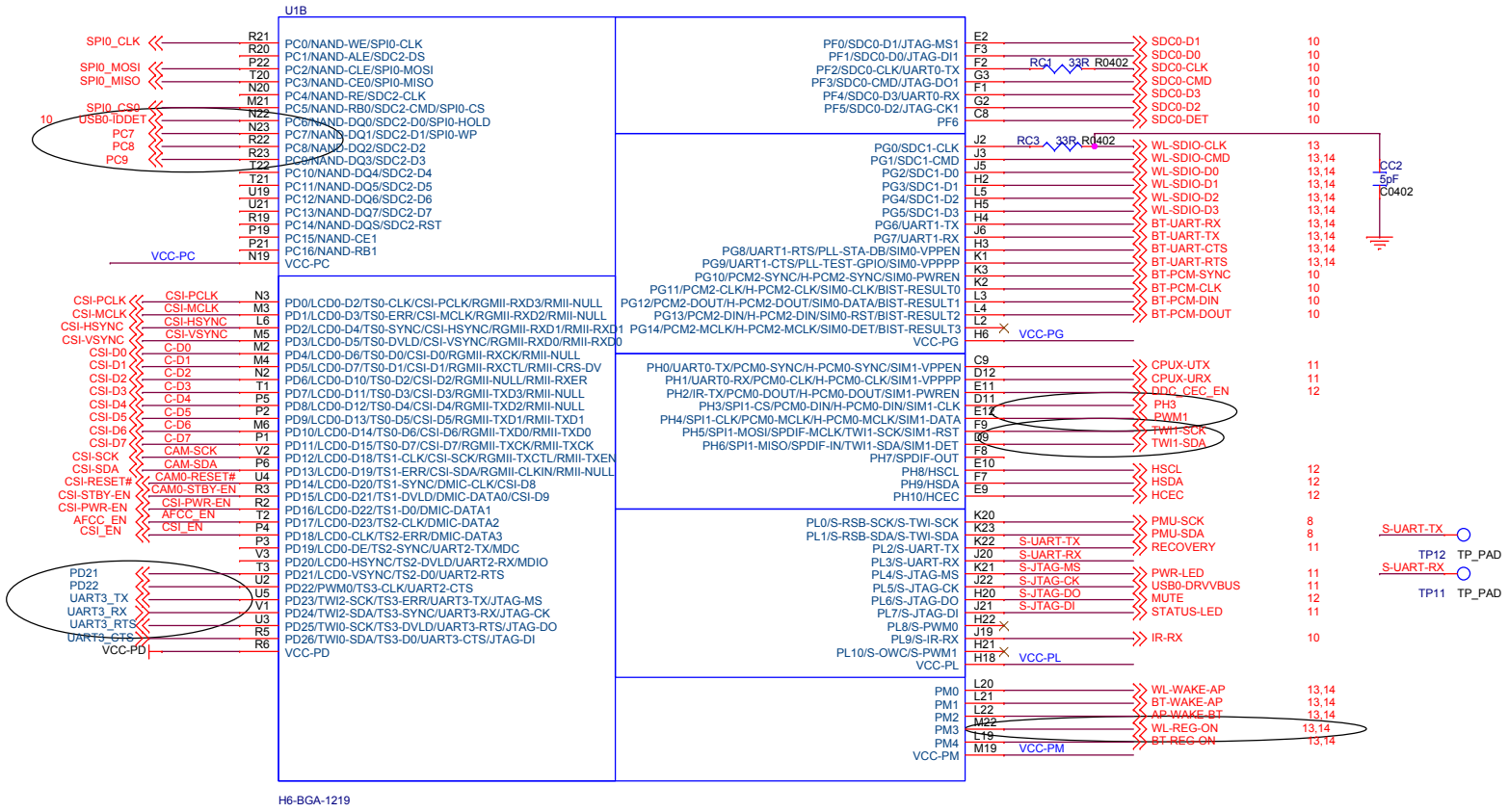
PC,PD, 部分IO口不具备中断功能
PF,PG,PH,PL,PM，部分IO口有中断功能



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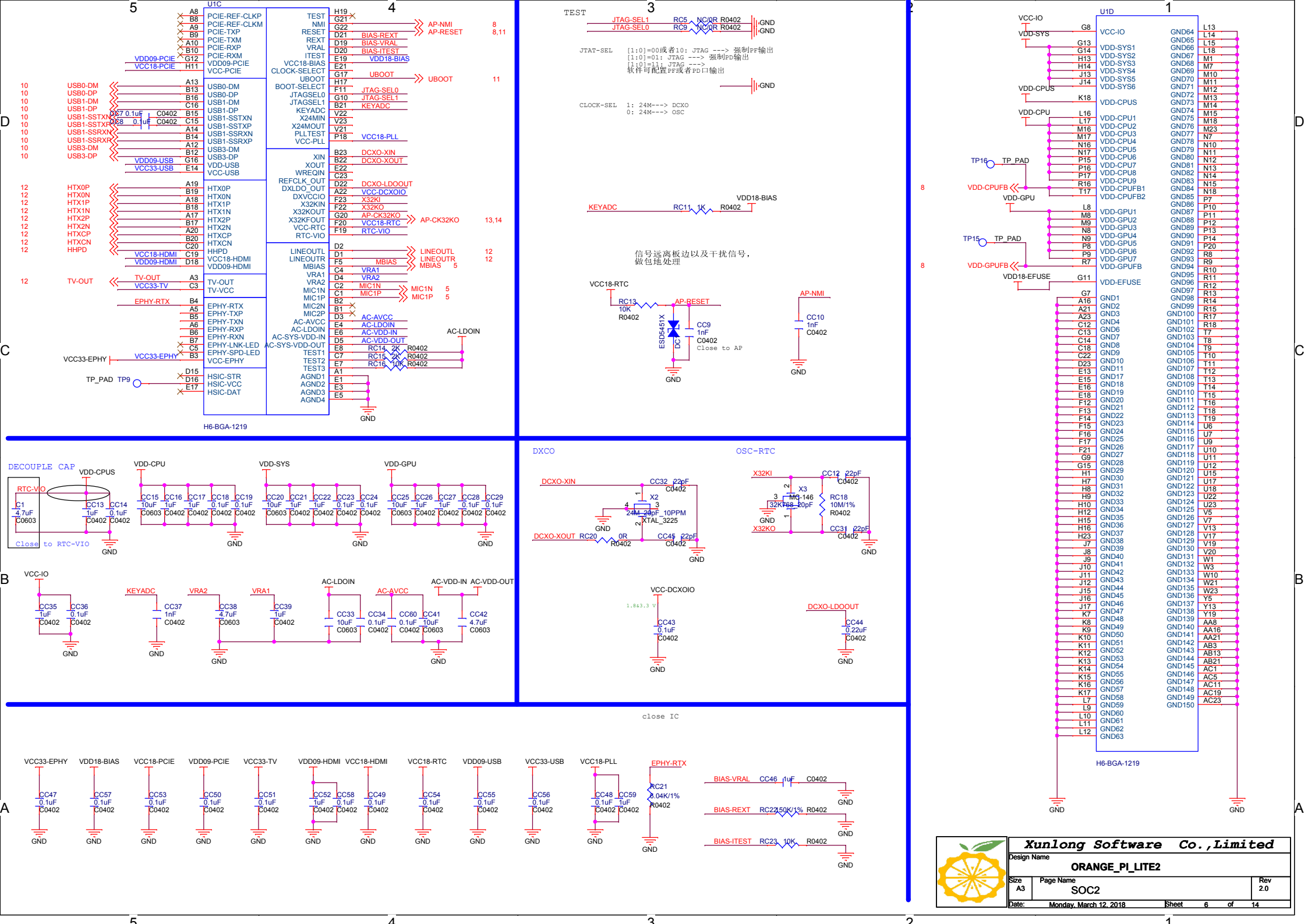
U1C
H6-BGA-1219
U1D
H6-BGA-1219
TEST
JTAG-SEL1
JTAG-SEL0
JTAT-SEL [1:0]=00或者10: JTAG ---> 强制PF输出
[1:0]=01: JTAG ---> 强制PD输出
[1:0]=11: JTAG --->
软件可配置PF或者PD口输出
CLOCK-SEL 1: 24M---> DCXO
0: 24M---> OSC
KEYADC
VDD18-BIAS
信号远离板边以及干扰信号，
做包地处理
VCC18-RTC
AP-RESET
AP-NMI
ESD5451X
Close to AP
DECOUPLE CAP
RTC-VIO
Close to RTC-VIO
VDD-CPUS
VDD-CPU
VDD-SYS
VDD-GPU
DXCO
OSC-RTC
DCXO-XIN
DCXO-XOUT
X32KI
X32KO
VCC-IO
VCC-DCXOIO
DCXO-LDOOUT
close IC
EPHY-RTX
BIAS-VRAL
BIAS-REXT
BIAS-ITEST
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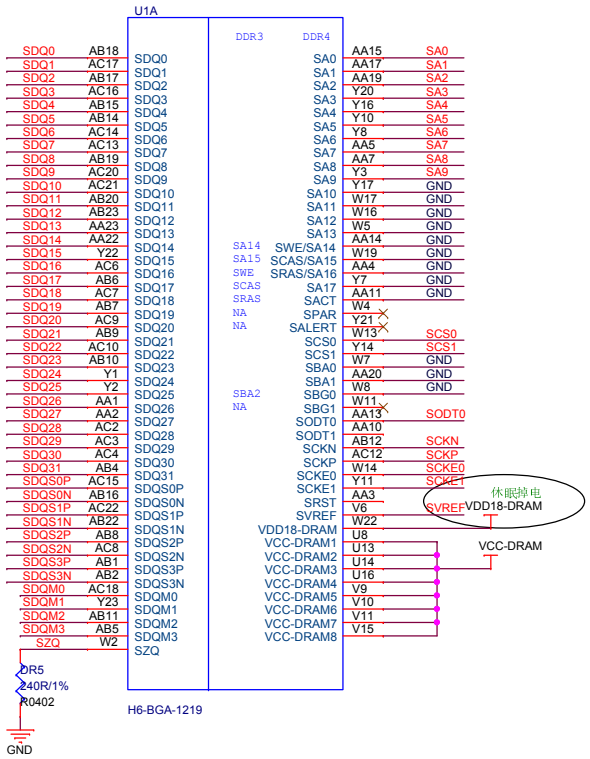
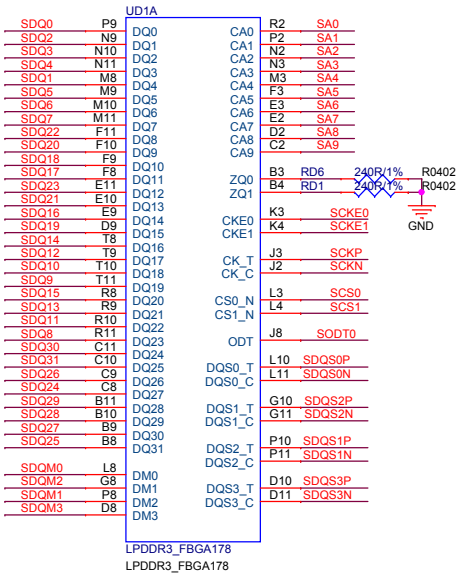
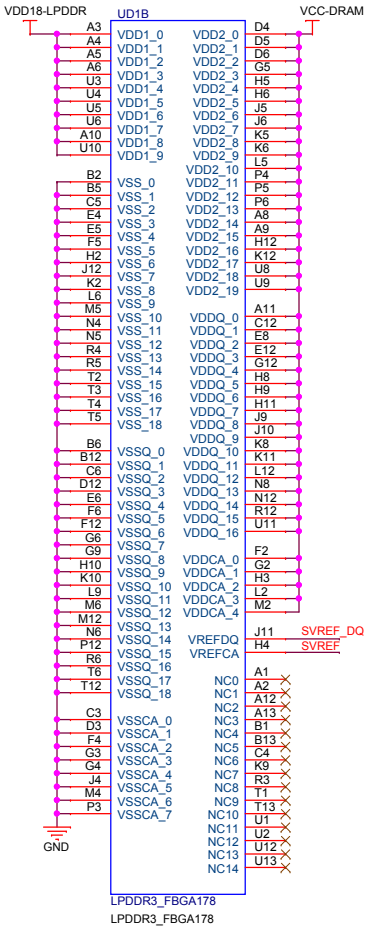
LPDDR3

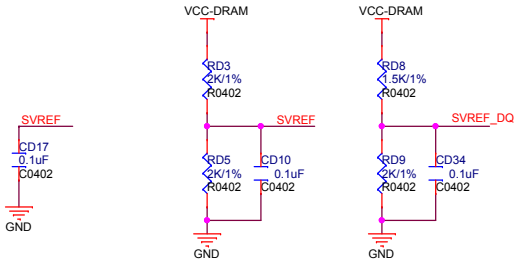


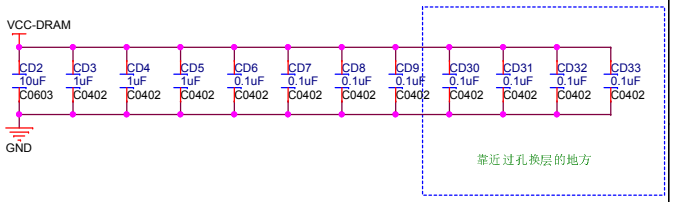


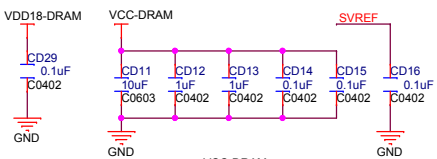
LPDDR3_FBGA178

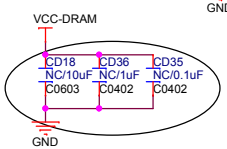


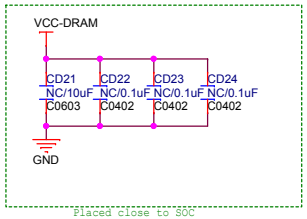
LPDDR3_FBGA178

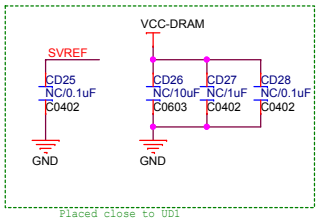


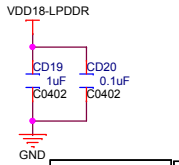


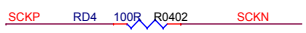












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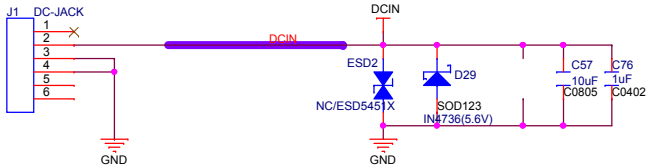
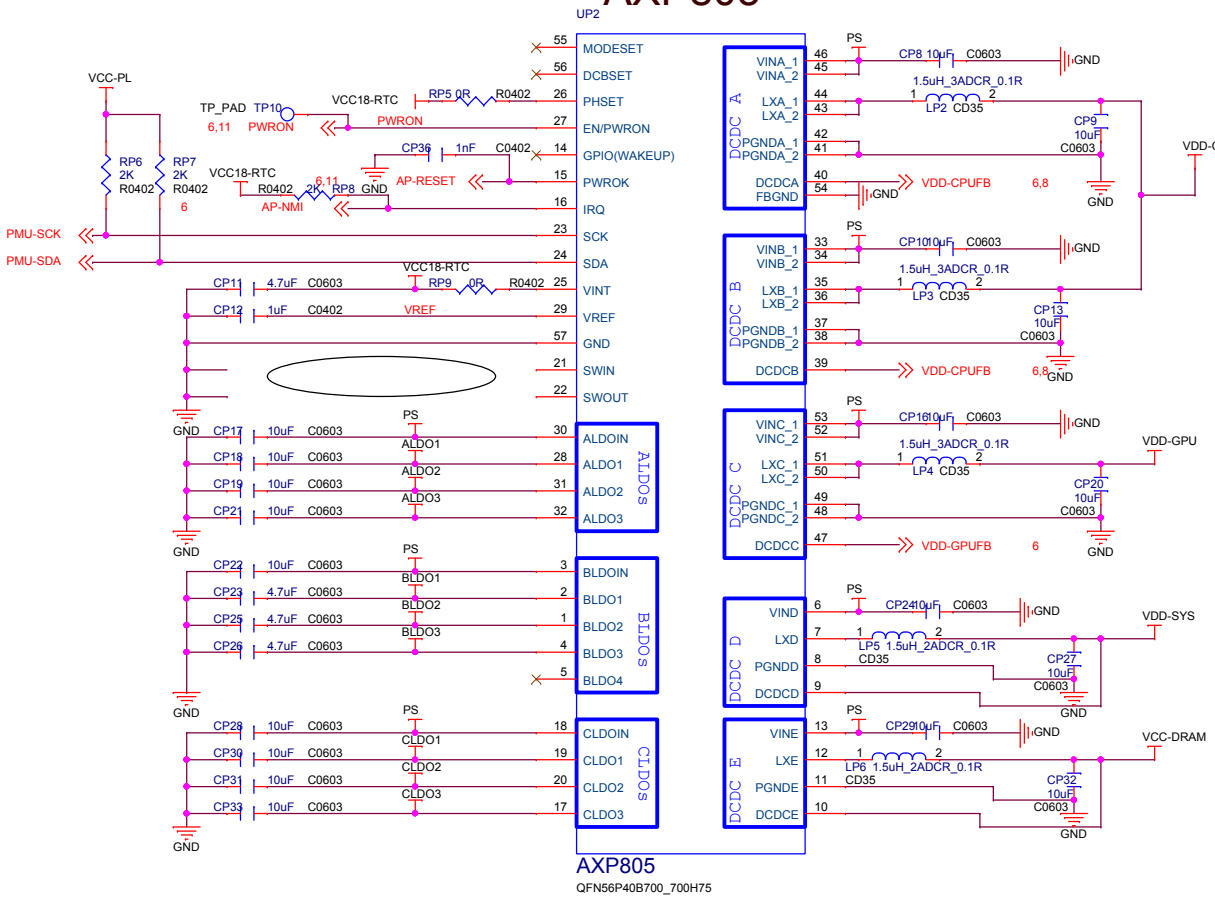
DCIN

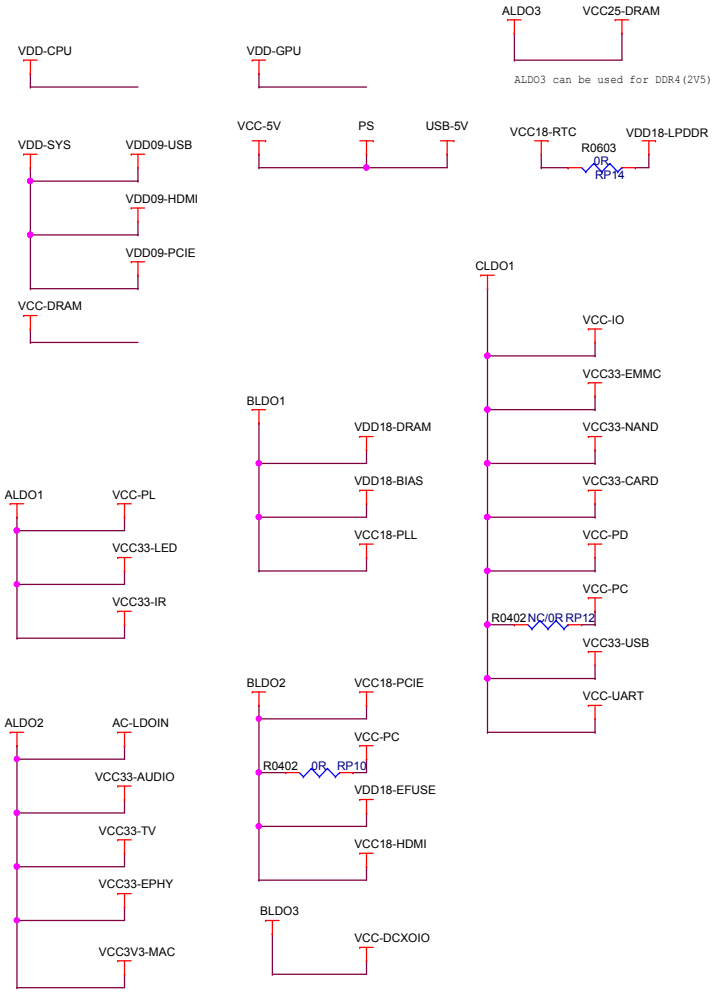


PMIC

AXP805



AXP805
QFN56P40B700_700H75



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eMMC

NAND

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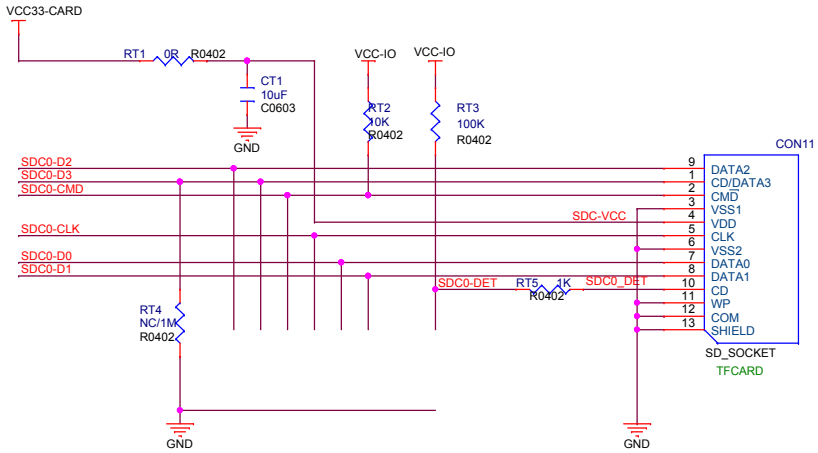
5 4 3 2 1

SPDIF

5 SDC0-D1
5 SDC0-D0
5 SDC0-CLK
5 SDC0-CMD
5 SDC0-D3
5 SDC0-D2
5 SDC0-DET

CARD



USB

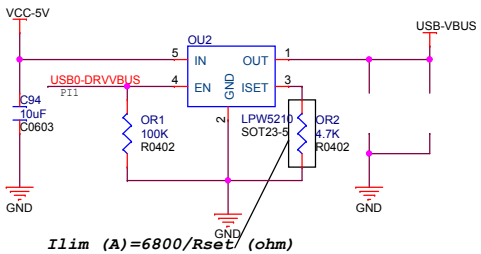
Differential pairs
Z0= 90 ohm

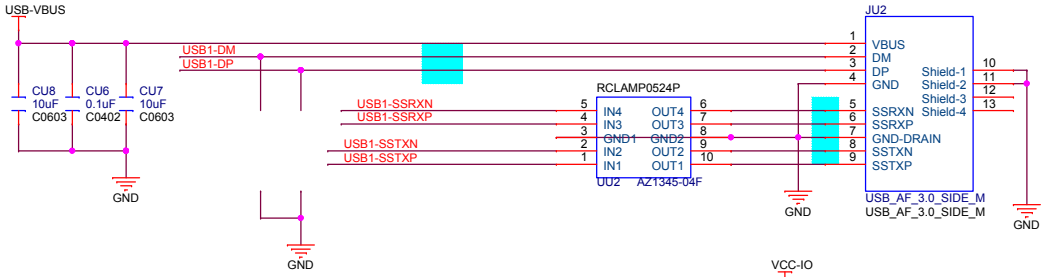
6 USB0-DRVVBUS

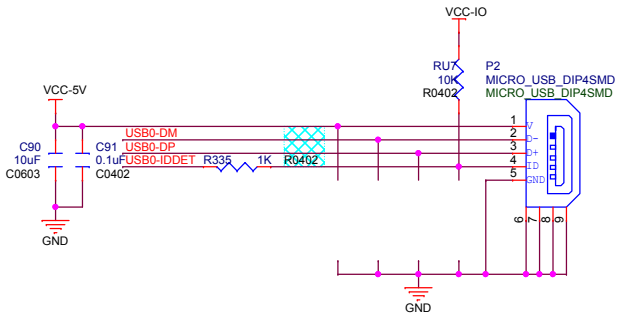
10 USB0-DM
10 USB0-DP
10 USB0-IDDET

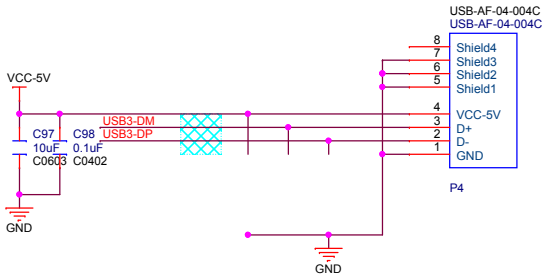
10 USB1-DM
10 USB1-DP
10 USB1-SSTXN
10 USB1-SSTXP
10 USB1-SSRXN
10 USB1-SSRXP

10 USB3-DM
10 USB3-DP









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5 4 3 2 1

Audio

6 LINEOUTL
6 LINEOUTR
12 MUTE

MUTE — TP27 TP_PAD
LINEOUTL — TP23 TP_PAD
LINEOUTR — TP24 TP_PAD
GND — TP26 TP_PAD

CSI-RESET# — CAM0-RESET#
CSI-STBY-EN — CAM0-STBY-EN
CSI-PWR-EN — CSI-PWR-EN
CSI-SCK — CAM-SCK
CSI-SDA — CAM-SDA
CSI-PCLK — CSI-PCLK
CSI-MCLK — CSI-MCLK
CSI-HSYNC — CSI-HSYNC
CSI-VSYNC — CSI-VSYNC
CSI-D0 — C-D0
CSI-D1 — C-D1
CSI-D2 — C-D2
CSI-D3 — C-D3
CSI-D4 — C-D4
CSI-D5 — C-D5
CSI-D6 — C-D6
CSI-D7 — C-D7
AFCC_EN — AFCC_EN
CSI_EN — CSI_EN

CON1
FPC24-05PH-BOT
FPC24-05PH-BOT

DCIN
C-D2
C-D1
C-D3
C-D0
C-D4
CSI-PCLK R69 22R R-PCLK R0402
C-D5
C-D6
CSI-MCLK R70 22R R-MCLK R0402
C-D7
AFCC_EN
CSI_EN
CSI-HSYNC
CAM0-STBY-EN
CSI-VSYNC
CAM0-RESET#
CAM-SCK
CSI-PWR-EN
CAM-SDA
DCIN

CSI-PCLK — C124 NC C0402 — GND
Close to AP

VDD1V5-CSI=1.5V
VCC-CSI =2.8V

Video

Z0= 37.5ohm

6 TV-OUT — TV-CVBS TP25 TP_PAD
RA13 75R/1% R0603 — GND

6 HTX0P
6 HTX0N
6 HTX1P
6 HTX1N
6 HTX2P
6 HTX2N
6 HTXCP
6 HTXCN
5 HSCL
5 HSDA
6 HHPD
5 HCEC

5 DDC_CEC_EN

HDMI

Differential pairs
Z0= 100 ohm

VCC-IO — RH1 10K R0402 — QH1 — HSCL — BSN20 SOT-23 — HDMI-SCL
HDMI-5V — RH2 1.8K R0402
DDC_CEC_EN — RH12 0R R0402
VCC-IO — RH10 NC/0R R0402 — HDMI-5V
RH3 10K R0402 — QH2 — HSDA — BSN20 SOT-23 — HDMI-SDA
RH4 1.8K R0402
VCC-IO — RH6 56K/1% R0402 — QH3 — HCEC — BSN20 SOT-23 — HDMI-CEC
D36 IN5819SL SOD123 — VCC-IO
RH7 56K/1% R0402
VCC-5V — D35 IN5819SL SOD123 — HDMI-5V

UH1 AZ1345-04F
HTX2P — IN1 OUT1 — HTX2P
HTX2N — IN2 OUT2 — HTX2N
GND1 GND2
HTX1P — IN3 OUT3 — HTX1P
HTX1N — IN4 OUT4 — HTX1N
RCLAMP0524P

UH2 AZ1345-04F
HTX0P — IN1 OUT1 — HTX0P
HTX0N — IN2 OUT2 — HTX0N
GND1 GND2
HTXCP — IN3 OUT3 — HTXCP
HTXCN — IN4 OUT4 — HTXCN
RCLAMP0524P

HDMI-CEC
HDMI-SCL
HDMI-SDA
HHPD — RH5 10K R0402
RH8 0.1uF C0402
ESD5451X
DH1 DH2 DH3 DH4 DH5
GND

HDMI-5V

JH1
HDMI_19plug type C
HDMI\YKF45-7012-1
D2P
G_D2
D2N
D1P
G_D1
D1N
D0P
G_D0
D0N
CLKP
G_CLK
CLKN
CEC
NC
SCL
SDA
G_DDC/CEC
+5V
HOT_PLUG_DET
SHIELD1 SHIELD2 SHIELD3 SHIELD4

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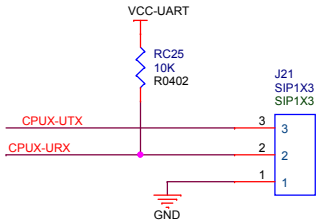
EPHY-FE

Differential pairs
Z0= 100 ohm

VCC33-EPHY
VCC-EPHY-LED
VCC33-EPHY

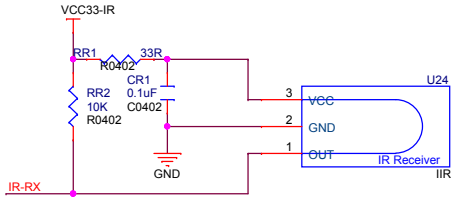
5 CPUX-UTX
5 CPUX-URX
5 PWR-LED
5 STATUS-LED

DEBUG



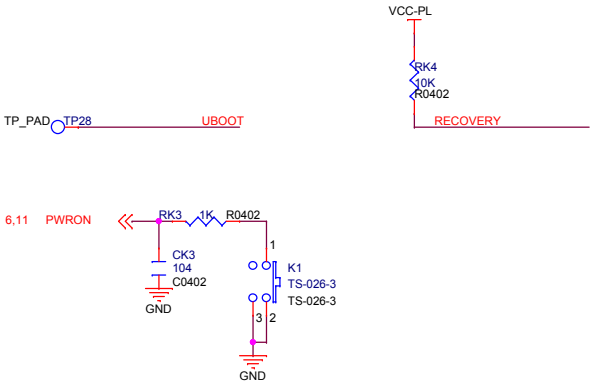
6,8 AP-RESET
6 UBOOT
5 RECOVERY

IR



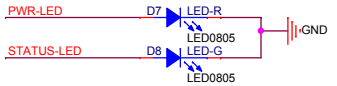
5 IR-RX
5 MBIAS
5 MIC1P
5 MIC1N

KEY

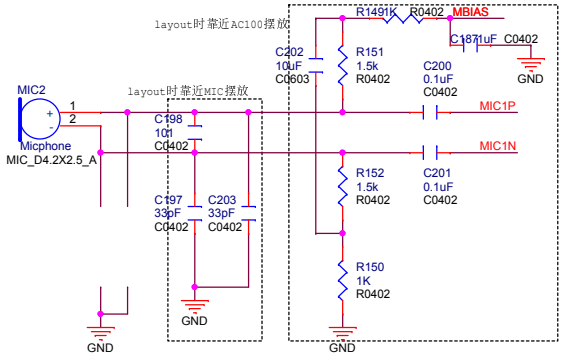


MASK1 MASK2 MASK3 MASK4
SMD SMD SMD SMD

LED



MIC



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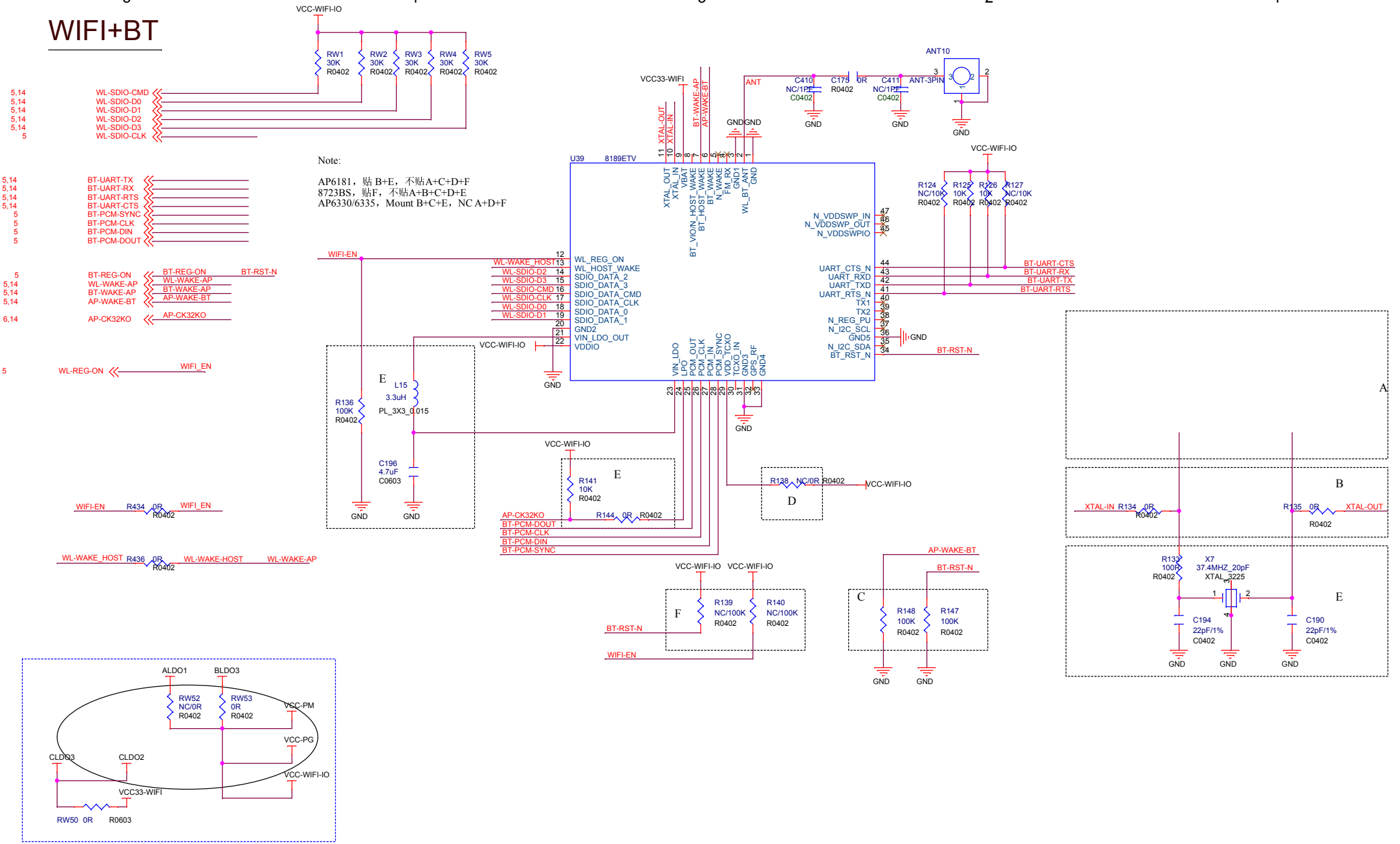
WIFI+BT



RW51 RW45 RW46 RW50 RW52 RW53

不带蓝牙遥控	IO为1.8V	NC	NC	NC	0R	NC	0R
	IO为3.3V	NC	NC	NC	0R	0R	NC
带蓝牙遥控	IO为1.8V	0R	NC	NC	NC	NC	NC
	IO为3.3V	0R	0R	0R	NC	NC	NC

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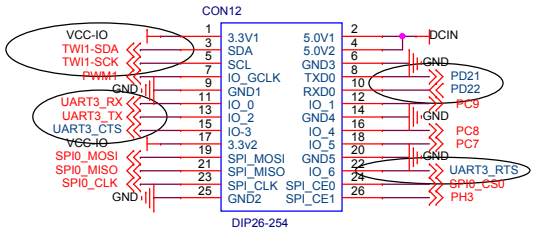
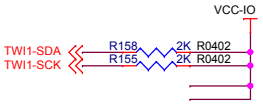
Ext Port

Ext





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