

# Ajay Harikumar

San Jose, CA 95134  
T: 408-621-8444

E: [ajay.harikumar@gmail.com](mailto:ajay.harikumar@gmail.com)

Linkedin: <http://linkedin.com/in/ajayharikumar>

## Objective

Use my diverse technical skills and business acumen to make impactful change using technology. Looking for senior positions in startups. I prefer working on Python/R and Go-lang. Green card/authorized to work in US.

## Skills

18 years Software Engineering experience including Architecture, Design, Coding/Software development, Product Ownership, Building Teams, new Project/Business proposals.

Five patents, IDF in pipeline, external and internal papers  
(<https://scholar.google.com/citations?user=eNafY6MAAAAJ&hl=en>)

## Skill Matrix

Expert	<b>C, Systems, Runtime</b>	Binary translation, BIOS, Simulators, Performance analysis and Optimizations
Good	<b>Python</b> , Algorithms/Data structures, x86 assembly	Code optimizations and Computer Architecture
Previous work experience	C++, Android system and app development, R	Virtualization, EFI
Personal projects	<b>Go-lang</b> , HTML5	Web backend
Hobby	R, Python	Quantitative Analysis
Soft skills	Highly results oriented, mentoring, idea generator, diverse technical and business interests	

## Education

<b>MS in Software Systems</b>	BITS Pilani, India.	7.4 aggr	2005-07
<b>B.Tech in Electrical and Electronics</b>	Kerala University, India	7.5 aggr	1992-96

## Experience

<b>Staff Software Engineer</b>	<b>Intel</b> (2012 to present)	<b>Binary Translation</b> – Feature development and algorithms for performance improvements for various Binary Translation (BT) projects. Responsibility includes architecture, design and software development (C lang). Projects are - <b>App level BT</b> Security project for Control Flow Integrity protection against various malware attacks like ROP and Stack Pivoting on Windows. Currently used by McAfee for identification of zero-day attacks and feeding into their virus definitions. Personally responsible for 2X speedup and 50% memory reduction in product - <b>Android</b> : Enabling same project on Android - <b>Processor</b> : Working with Processor Architects on a hardware-software co-design project to increase IPC using BT
<b>Platform Architect</b>	<b>Intel</b> (2009 to 2012)	Owned System performance in Platform Architecture team for Intel tablets/phones. Performance projections (for CPU, Gfx, Memory) on Intel and competitive platforms using in-depth architectural knowledge, simulations, experiments (e.g.

# Ajay Harikumar

		<p>identifying and meeting Windows 8 Metro UI performance requirements). More than 50 million tablets that I have worked on, have been sold</p> <p>Created SDV (Software Dev Vehicle) for graphics driver development by extending an FPGA emulator with Qemu VMM and bus functional models. Successfully rendered images using extremely complex flow between App/Driver ↔ VMM ↔ BFM ↔ IP (Verilog-FPGA)</p>
Senior Research Scientist	<b>Intel Labs</b> (2005-2008)	Architecting, designing and prototyping Platform and security features for Intel platforms. Virtualization/Partitioning, OS integrity analysis etc.
Senior Software Engineer	<b>Intel</b> (2002-2005)	Owned <b>BIOS</b> (UEFI – C and ASM) for many Intel Server Platform generations including development, project management and coordination with multi-site teams
Senior Software Engineer	<b>Virtio</b> (Synopsis) (2000-2001)	Instruction Set <b>Simulators</b> (C/C++ language) for a startup with radical idea of creating platforms and running simulations in browsers
Senior Software Engineer	<b>Philips</b> (1999-2000)	Developed bit/cycle accurate, behavioral and functional simulation models for Processors including MIPS and DSP (C/C++ and Linux)
Software Engineer	<b>Accord</b> (1997-1999)	HP: <b>Automotive software</b> (Ford and Mazda cars) (C/ASM) Defense: Light Combat Aircraft <b>Avionics</b> (ADA and i386)

## Links

LinkedIn: <http://linkedin.com/in/ajayharikumar>  
 Web: <http://ajayharikumar.com>  
 Github: <https://github.com/ajayhk>

## References

Available on request

## Other activities

- Reviewer and contributor to Intel's biggest Tech conf (**DTTC**), reviewer and organizer for **HIPC**
- **5 patents, one external paper (VDAT 2000) and four internal papers**
- Industry talk at HIPC 2010
- **Conceptualized and conducted site wide Innovation Contest**. Over 170 teams participated with winner getting funding for prototyping and project
- **Expert at "Meet the Experts" at Intel Developer Forum 2005**
- Volunteer at Sacred Hearts and other charitable organizations
- Started site Gaming Chapter and game room with high-end gaming PCs sparking site-wide interest in PC gaming
- **Quantitative Analysis – Using R and Python**, developed stock trading algorithms; **ranked 17<sup>th</sup> best performance** among 300 entries