Ajay Harikumar

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EXPERIENCE AND SKILLS

Domains 20+ years' experience in software industry including **AI/Machine Learning, Distributed Deep Learning, System Software and Architecture**, Performance Analysis and Optimization, Binary Translation, Modeling/Simulations, H/w-S/w co-design. 10 patents

Languages **C/Modern C++**, Python

PROFESSIONAL EXPERIENCE

Principal Engineer ***Intel*** ***2017-current***

Distributed Deep Learning on Intel Nervana AI Training Chip[1]

- Expert on Distributed Deep Learning including scaling, full-stack integration, performance and convergence
- Tech-lead for system software team (10 member) owning **Distributed Training** incl. arch/design, code, collective kernels, Hw/Sw co-design, requirements, customer interaction, projections, roadmap, hiring
- Achieved **world-class scaling performance (95%)** on Data and Model Parallelism (Intel AI DevCon Keynote[2])
- ML Frameworks (TensorFlow, PaddlePaddle), CNNs, RNNs/LSTMs, Transformer full-stack bring-up

Manager / Senior Staff S/w Engineer ***Intel*** ***2012-2016***

- **Promoted to Manager** of system software team. Managed team of 8 software engineers + Product manager for two products that did malware detection (Return Oriented Programming/Stack Buffer Overflow attacks) using Control Flow Integrity (CFI) with Binary Translation (BT). One product used by McAfee for identifying malware and feeding into their virus definitions. Other product protects apps incl. Microsoft Office, Google Chrome, Firefox, Acrobat PDF viewer against many Zero-day attacks (e.g.[3]). Detection tested on malware in VirusTotal, McAfee DB samples. **Performance overhead of Binary Translation reduced from 3-4x to 10%**
- Tech lead (software dev/perf improvement) for multiple BT projects incl. Android malware detection, h/w BT. Created Perf Framework for identifying performance bottlenecks and regressions (not possible with tools like Intel VTune). **50% memory reduction and 2x perf speedup**

Staff Software Engineer ***Intel*** ***2009-2012***

- **Platform Architect** owning Power/Performance for Intel Mobile Platforms (Smartphones, Netbooks, Tablets)
- Owned System performance in Platform Architecture team for Intel tablets/phones. Performance projections (for CPU, Gfx, Memory) on Intel and competitive platforms using in-depth architectural knowledge, simulations, experiments
- Created SDV for graphics driver development with FPGA emulator with Qemu and bus functional model (BFM)

Senior Software Engineer ***Intel*** ***2002-2008***

- **Research Scientist** in Intel Labs researching on System Architecture including System Partitioning & Security including early version of Intel SGX[4]
- Modeling features including bringing up **two Partitions running Windows and Linux in parallel** on same desktop
- **EFI/BIOS Software Engineer** in Server BIOS team. Delivered **first ever EFI server BIOS** and future generations for various Intel Server Platforms released 2002-05

Senior Software Engineer ***Virtio (startup acquired by Synopsys)*** ***2000-2001***

- Created Instruction Set Simulators (C/C++) with radical idea of creating and running simulation platforms in browsers

[1] https://www.intel.ai/intel-nervana-neural-network-processors-nnp-redefine-ai-silicon
[2] https://www.forbes.com/sites/moorinsights/2018/06/01/intel-shows-off-its-ai-chips-and-chops
[3] https://blog.trendmicro.com/trendlabs-security-intelligence/high-profiled-cyber-theft-against-banks-targeted-swift-systems
[4] https://software.intel.com/en-us/sgx

Senior Software Engineer ***Philips Semiconductors*** ***1999-2000***

- Developed bit/cycle accurate, behavioral and functional simulation models for Processors including MIPS and DSP (C/C++ and Linux). First SystemC modeling of retargetable reconfigurable DSP[5]

Senior Software Engineer ***Accord Software*** ***1997-1999***

- **Hewlett Packard:** Automotive software (Ford and Mazda cars) (C/x86 Assembly)
- **Aeronautical Development Agency:** Mission Computer software/Avionics for Light Combat Aircraft[6] (ADA/i386)

EDUCATION & CERTIFICATIONS

Masters in Software Systems **BITS Pilani, India**
Bachelors in Electrical & Electronics **Kerala University, India**

Algorithms and Data Structures Coursera
CS231n: Convolutional Neural Networks for Visual Recognition Stanford Online

AWARDS / PATENTS / OTHERS

Patents: **10 patents.** https://scholar.google.com/citations?user=eNafY6MAAAAJ&hl=en
Side Projects: Stock trading algorithms **ranked 17th best returns** among 300 entries; Reddit image downloader (github)
Conferences: Reviewer/contributor to Intel tech conf (**DTTC**), reviewer and organizer for **HiPC**, paper at **VDAT** 2000, talk at **HiPC** 2010, Expert at "Meet the Experts" at **Intel Developer Forum** 2005
Recognition: **Two promotions** in 4 years and **excellent ratings** in last 5 reviews. Multiple Dept. recognition awards
Github: https://github.com/ajayhk
Website: https://ajayhk.github.io

References available upon request

[5] https://www.design-reuse.com/news/25707/intel-buys-silicon-hive.html
[6] https://en.wikipedia.org/wiki/HAL_Tejas