Department Of Electronics Engineering

Indian Institute of Technology (Indian School of Mines), Dhanbad

B.Tech. Final Year Project

Schmitt Trigger using Dual output Second Generation Current Controlled Conveyor

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Certificate

This is to certify that **"Schmitt Trigger using Dual output Second Generation Current Controlled Conveyor"** is submitted by Ajay Jagannath (18JE0049), Akash Anand (18JE0054) and Venna Brahma Koti Reddy (18JE0913) under the supervision of Prof. Sajal Kr. Paul in the academic year 2021-22 as per the guidelines given by Department of Electronics Engineering of IIT(ISM), Dhanbad.

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Abstract

As the world of Electronics is headed towards an era of scaling down, the need of the hour is low power, low voltage but high-speed circuits that maintain a constant bandwidth and quality factor. Traditional voltage-based circuits no longer cut it in this world and there is a need for a shift to more power efficient logic model. The current mode circuits tick all the boxes and are becoming viable options of replacing the traditional voltage mode circuits. Schmitt Trigger is type of comparator circuit with a high static noise margin that has widespread applications in improving the noise immunity of the circuit and pulse shaping of the signal. Various circuits of Schmitt trigger using different building blocks are already in widespread use but we aim to implement Schmitt Trigger using current mode circuit, focused on reducing the power dissipation loss and improving the slew Rate. This report presents the Schmitt trigger circuit using CCCII and its application in reversing the effect of a software induced switch bouncing, which has practical implications on logical circuits in real life. The threshold values of the hysteresis loop can be controlled by the external bias current which helps in making the time for switching of the Switch Debouncing circuit tuneable. Moreover, we can design both the inverting and non-inverting Schmitt trigger using a single CCCII block.

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Chapter 1: Introduction

1.1 Schmitt Trigger

Schmitt trigger is an electronic circuit that will trigger a change in output when there is a significant change in the input signal. The main appeal of the Schmitt trigger is its ability to work on two different threshold levels and its **hysteresis** property which is vital in the suppression of noise in various analogue as well as the digital circuits.

Schmitt trigger provides a means of improving the sensitivity of the circuit from the electromagnetic interference that meaning they enhance the **static noise margin** of the circuit at the cost of the power and certain additional delay. Schmitt trigger is also known as a bi-stable circuit because of its capability to work on two different threshold values. Because of two different threshold voltages, the Schmitt trigger will switch the output when the input is less or greater than the lower or the upper threshold voltage levels respectively and in between the voltage levels Schmitt trigger will **retain the output value**.
This is the characteristic that primarily helps with noise suppression.
Schmitt triggers can also be used for **reshaping of the pulses**.

A Schmitt trigger is basically a comparator circuit with the positive feedback signal which means that the loop gain of the circuit is greater than one. The feedback is used for the reason of providing different threshold voltages to the Schmitt trigger in order to have the hysteresis property. Schmitt trigger functions as a signal restoring circuit which means that they can be used to filter out the original input signal information present by eliminating the noise content from it.

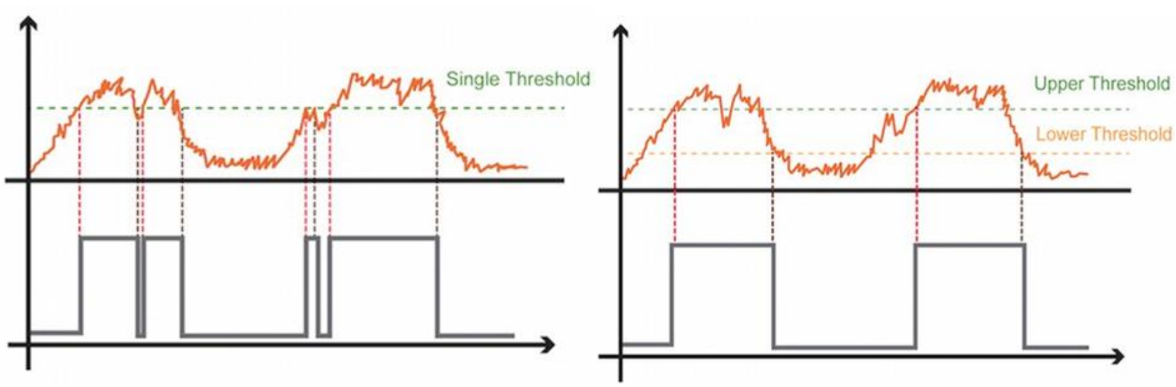

Figure 1. Comparison of Noise Suppression of Simple Comparator and Schmitt Trigger

The Hysteresis loop is the transfer characteristics of the Schmitt trigger drawn by varying the output voltage of the Schmitt trigger with respect to the input DC voltage. Hysteresis is the dependence of the state of a system on its history due to the Schmitt trigger has positive feedback. For this reason, at any particular input, we may be able to observe more than one output value.

The Schmitt Trigger has a wide range of applications which will be covered in the latter part of the project.

1.1.1 Operational Amplifier based Schmitt Trigger

Initially the Schmitt trigger was created using the op-amp. Positive feedback was given to the output voltage and to the non-inverting input with a resistor between them and another resistor between the Vin and the non-inverting input.

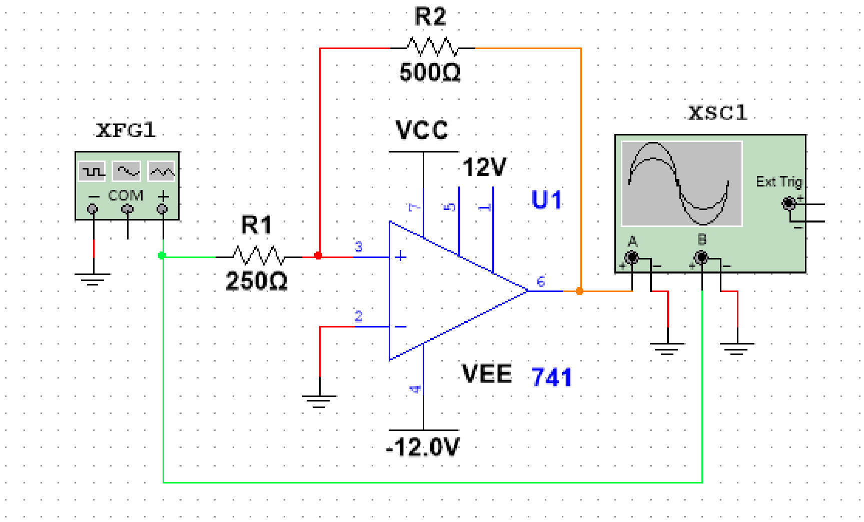

Figure 2. Circuit Diagram for Schmitt trigger using op-amp.

If the Voltage at the non-inverting terminal is positive then the input voltage is equal to the upper threshold voltage which is given by:-

For $V_+ > 0$,

$$V_{in} = V_{UT} = V_{SAT}.\frac{R1}{R2}$$

Whereas, if the Voltage at the non-inverting terminal is negative then the input voltage is equal to the lower threshold voltage given by:-

For $V_+ < 0$,

$$V_{in} = V_{LT} = -V_{SAT}.\frac{R1}{R2}$$

We built the circuit of Schmitt trigger using op-amp in Multisim, simulated it and the following results were obtained: -

$$V_{in} = V_{UT} = \pm\frac{V_{SAT}}{2}$$

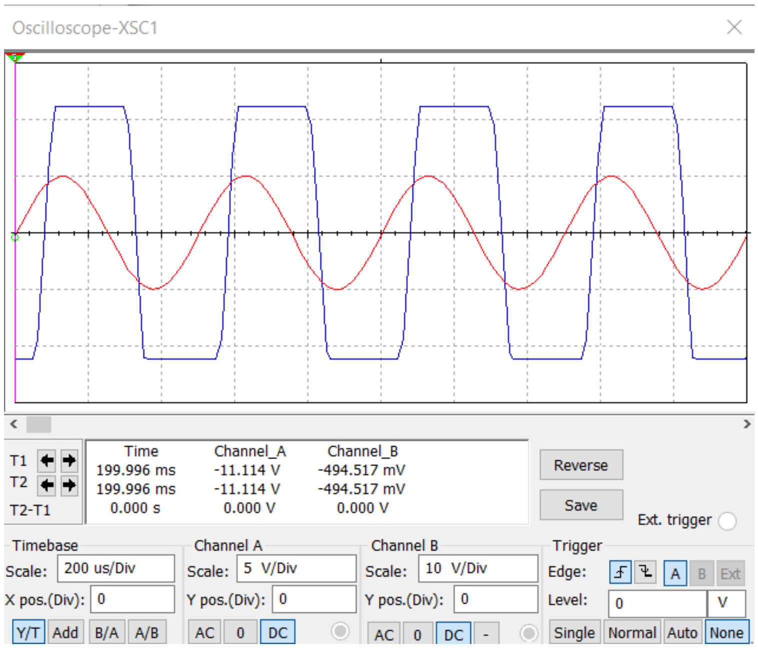

Figure 3. V_{in} Vs Time & V_{out} Vs Time

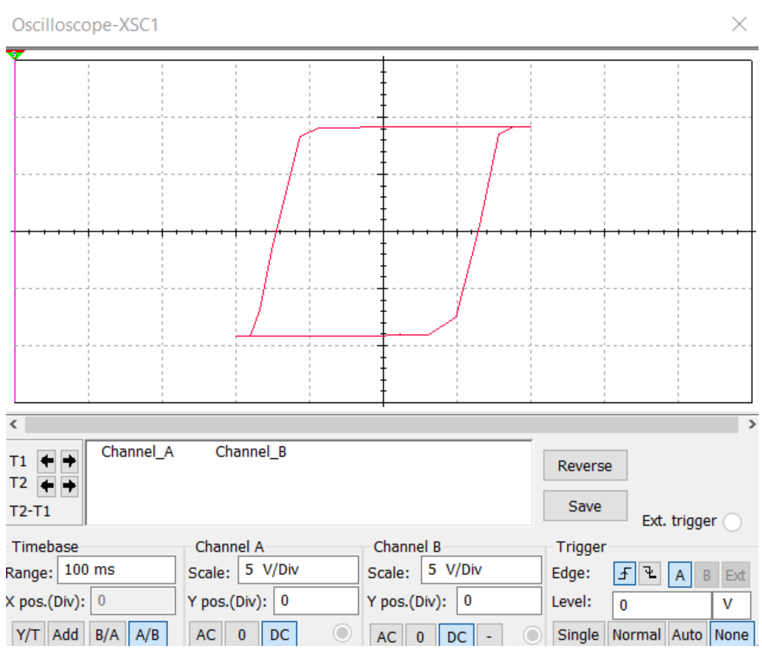

Figure 4. Hysteresis Graph (Transfer Characteristics V_{out} vs V_{in})

1.2 Current Mode Circuits

All of these conventional analog circuits were voltage mode circuits where the circuit performance is determined in terms of voltage level at various nodes including the input and the output nodes. Current mode circuits have various advantages over voltage mode circuits such as:-

I. Relatively high slew rate.
II. Low-power consumption
III. Low-voltage operation
IV. Less number of passive components are required to perform a specific function.
V. They show high performance in terms of speed, bandwidth and accuracy.

Due to these reasons, we preferred current conveyor as building block for the Schmitt trigger.

1.2.1 Second Generation Current Conveyor (CCII)

The CCII is a three-terminal device with the terminals designated as x, y, z. It has one high and one low impedance input. A current-conveyor circuit can provide a higher voltage gain over a larger signal bandwidth under small or large signal conditions than a corresponding op-amp circuit in effect a higher gain-bandwidth-product.

Port Y exhibits infinite input impedance, port X exhibits a zero-input impedance and port Z is a high impedance output port.

The ideal characteristic representation of the second generation current conveyor (CCII) is given by:-

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix}$$

1.2.2 Schmitt trigger using second generation current conveyor (CCII)

With a decrease in the output voltage, there's an increase in the current i_x, since the voltage v_x, decreases ($v_x = v_y$). The current i_z increases by the same factor as i_x resulting in another increase v_z. In a real CCII the output voltage is limited by the power supply. Hence the circuit will show only two stable states equal to $+V_{sat}$ and $-V_{sat}$ with the output saturation currents.

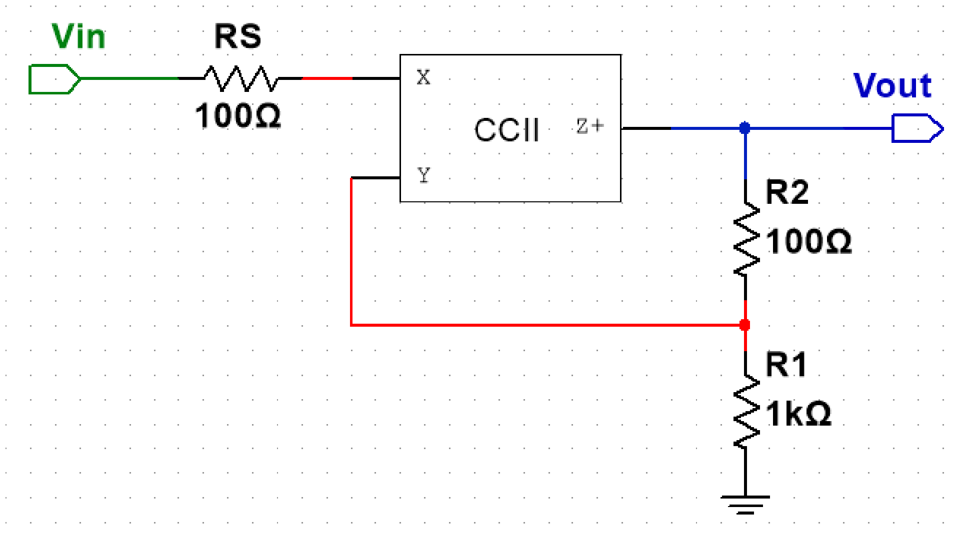

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Figure 5. Circuit Diagram of Schmitt Trigger using CCII

The output current I_z from the above circuit is given by:-

$$I_z = \pm \frac{V_{sat}}{R_1 + R_2}$$

The two threshold voltages V_{LT} and V_{HT} can be found by assuming first that v_z, is set to the stable V_{sat}. To change this stable state, the current i_x, must satisfy the relation

$$i_x \geq i_z \qquad => \qquad \frac{v_{in} - v_y}{R_S} \geq -\frac{V_{sat}}{R_1 + R_2}$$

Hence V_{HT} is given by:-

$$V_{UT} = \frac{R_1 - R_S}{R_1 + R_2} V_{sat}$$

Following the same procedure but starting with the other stable state, we find V_{LT}:-

$$V_{LT} = \frac{R_1 - R_S}{R_1 + R_2} V_{sat}$$

From this we can obtain the hysteresis loop by plotting transfer characteristics to resemble Schmitt trigger.

Chapter 2: Literature Review

The topology in [1] is realized using one CCII+ and three resistors. This circuit required lesser supply voltage as compared to op-amp/voltage mode circuits but since it has three passive components so there is an high power dissipation. Moreover, since the amplitude and frequency are controlled by passive components, whose values have to be altered, so IC fabrication is difficult. The circuit proposed in [2], the Schmitt trigger circuit using Operational Transresistance Amplifier (OTRA), has one active block, i.e., OTRA, and one resistor. This circuit gave the hysteresis in both clockwise and counter clockwise manner but since it also has passive components so IC fabrication is difficult. The topology in [3], is realized using Voltage Differencing Transconductance Amplifier (VDTA) which has one resistor and one VDTA. In this circuit, the threshold values could be changed dynamically by changing the bias current but this circuit was not lossless. The Schmitt trigger circuit in [4], is realized using Current Differencing Transconductance Amplifier (CDTA) consisting of two resistors and one CDTA. It is built using 180nm technology using MOS. However, this circuit also has the same advantage and disadvantage as was with the Schmitt trigger using VDTA, as described above. The topology in [5], further improved and was proposed using Current Controlled Current Differencing Transconductance Amplifier (CCCDTA) which has no resistor and one CCCDTA. The topology is built using 0.35μm Taiwan Semiconductor Manufacturing Company (TSMC) technology. The input resistance values and the threshold values can be controlled by the bias current. Moreover, since no passive component is involved so IC fabrication is easier. The proposed circuit in [6], is realized using Multiple Output Current through Transconductance Amplifier (MO-CTTA) with no resistors and one MO-CTTA. The hysteresis and magnitude in this circuit can be independently/electronically controlled but the highest frequency is restricted at up to several megahertz range only. The topology in [1] also mentioned the Schmitt trigger circuit using Z-Copy Current Differencing Transconductance Amplifier (ZC-CDTA) which has two resistors and one ZC-CDTA. The topology is built using 180 nm Generic Process Design Kit (GPDK) technology. This circuit can operate at a very low voltage of 0.85 V. But the problem with this circuit is that it contains two passive components.

Chapter 3: Objective of Study

The main objective is to implement a Current Controlled Conveyor based Schmitt trigger with high speed, low voltage, low power, high bandwidth and better hysteresis width compared to traditional Schmitt Triggers, which will result in increased noise immunity for the digital as well as analogue circuits. The Schmitt trigger will provide additional tuneability of the lower and upper threshold currents, able to implement both clockwise and counter-clockwise hysteresis loops.

One of the several applications of the Schmitt Trigger will be studied by implementing switch debouncing of a software bounced signal using a RC circuit and the Schmitt trigger, where the switching of the output signal can be controlled by the user.

Chapter 4: Methodology

4.1 Current Controlled Conveyor

The Current Controlled Conveyor (CCCII) is a modified version of the Current Conveyor (CCII) such that the X input port has a variable intrinsic resistance that can be controlled by the input bias current. Further it can be designed to have dual outputs.

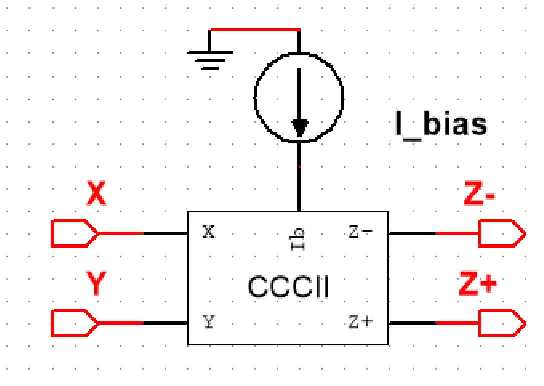

Figure 6. Schematic representation of CCCII.

The ideal characteristics of CCCII is given by,

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & R_X & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix}$$

Where,

$$R_X = \frac{1}{\sqrt{8\mu_n C_{OX}(\frac{W}{L})I_B}}$$

Solving the matrix, we obtain the port relationships.

$I_Y = 0$ $\qquad$ $I_{Z^+} = I_X$

$V_X = V_Y + I_X R_X$ $\qquad$ $I_{Z^-} = -I_X$

The main difference between the CCCII and the CCII is the presence of a **tuneable intrinsic resistance** at the terminal X which can be controlled by an additional output called the bias current. We can use this to our advantage to design circuits that are more efficient than CCII circuits.

4.2 Construction of CCCII

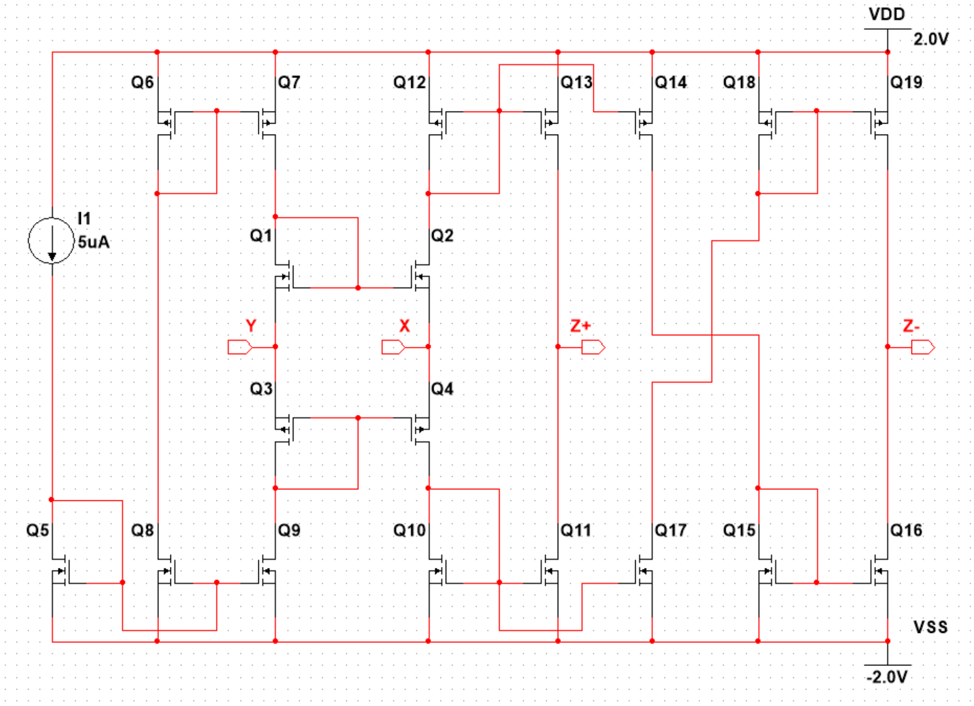

Figure 7. Internal Structure of CCCII.

A dual output Current Controlled Conveyor consists of Several CMOS Transistors in the form of current mirrors connected to supply voltage and a tuneable external input current.

4.3 Study of Port Relationships

4.3.1 *Current at X & Z Ports*

We can verify the port relationships by giving a **varying DC current** source to the Port X while grounding Port Y, Z+ and Z- for a **fixed bias current** of 5 µA.

Table 1. Variation of Port Parameters with change in Input Current

Input to Port X	I_X	I_{Z^+}	I_{Z^-}	I_Y
5µA	5µA	5µA	-5µA	-3.88pA
40µA	40µA	40µA	-40µA	-3.88pA
75µA	75µA	69.5µA	-58.5µA	-3.88pA
100µA	100µA	85.9µA	-64.4µA	-3.88pA

The Relationship $I_X = \pm I_Z$ holds for input current in the range of **1µA to 40µA**, after which there is a deviation from the ideal characteristics.

I_Y remains constant for a particular bias current value.

4.3.2 *Current at Port Y and the Intrinsic Resistance*

R_X remains constant for fixed bias current values.

$V_X = V_Y + I_X R_X$

By grounding port Y and giving a constant DC current of **5µA**, we can find the value of internal resistance as a function of input bias current using

$$R_X = \frac{V_X}{I_X}$$

Table 2. Variation of Parameters with change in Input Bias Current

Input Bias Current	I_Y	V_X	R_X
5µA	-3.88pA	177mV	35.4KΩ
20µA	0A	136mV	27.2KΩ
50µA	212nA	133mV	26.6KΩ
100µA	1.62µA	119mV	23.8KΩ
200µA	3.94µA	106mV	21.2KΩ

As the input bias current keeps increasing, the value of R_X decreases. This is consistent with the theory where Rx has an inverse dependence on I_B.

The value of I_Y increases with the increase of input bias current. **This is not a desired behaviour**. For values of bias current above 100µA, the value of I_Y is significantly non-zero that the port parameters no longer hold true.

Therefore, we fix the range of Input bias current to be in the range of **5µA to 50µA** for the port parameters of the CCCII to hold true.

4.4 Schmitt Trigger Using DOCCCII

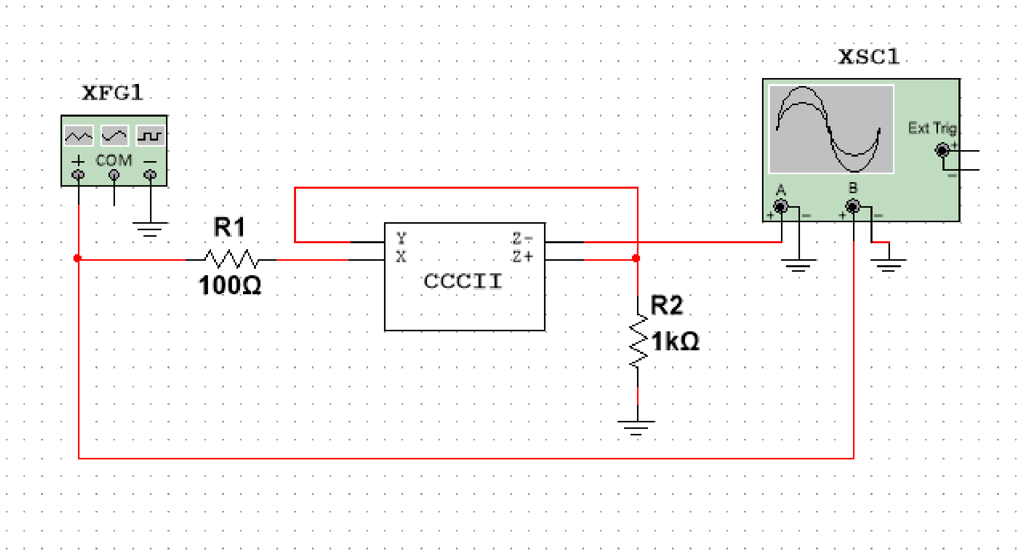

Figure 8. Construction of Schmitt Trigger using CCCII

A simple Schmitt trigger can be constructed using dual input CCCII but shorting the Y and Z+ port and connecting it to the ground using a resistor and giving an input voltage through a resistor to X port and taking the output from port Z-. This will lead to **Clockwise Hysteresis** where the output is positive when the input is positive and vice versa.

For a **Counter-Clockwise Hysteresis**, we just have to Switch the ports Z+ and Z-. Hence, we can say that we obtain a dual output Schmitt Trigger using CCCII.

4.4.1 Simulation Parameters

We will simulate the above designed CCCII based Schmitt trigger in Multisim using

Supply Voltage: ±2V

Input Voltage: $0.5V_P$, 2KHz Sinusoidal Wave.

Input Bias Current: 5µA

R1=100Ω

R2=1000Ω

4.5 CW Loop Schmitt Trigger

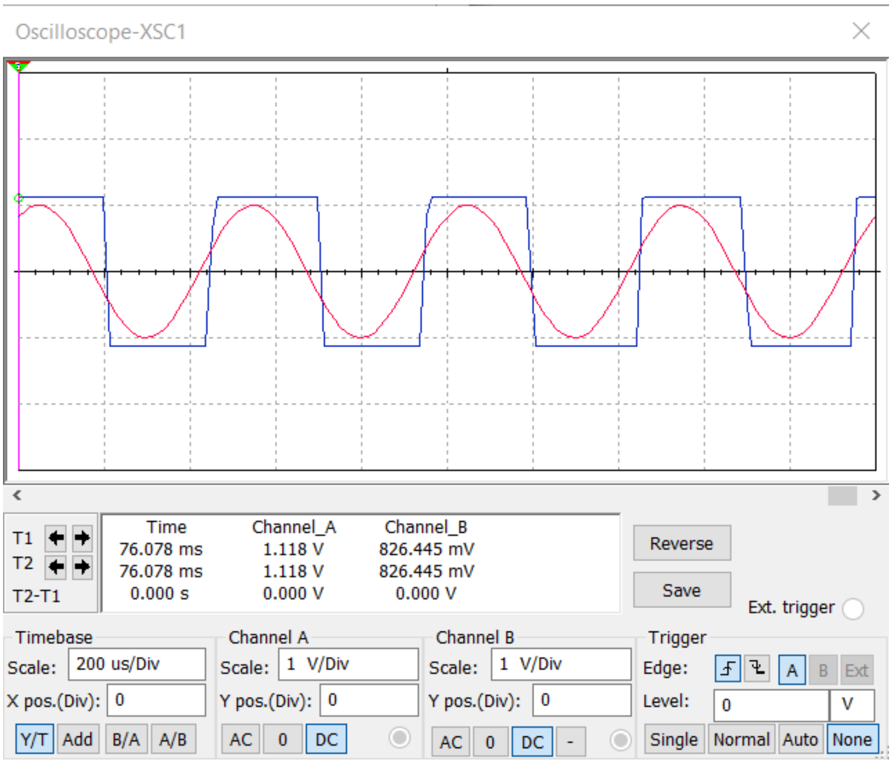

Figure 9. Transient Analysis of Input and Output

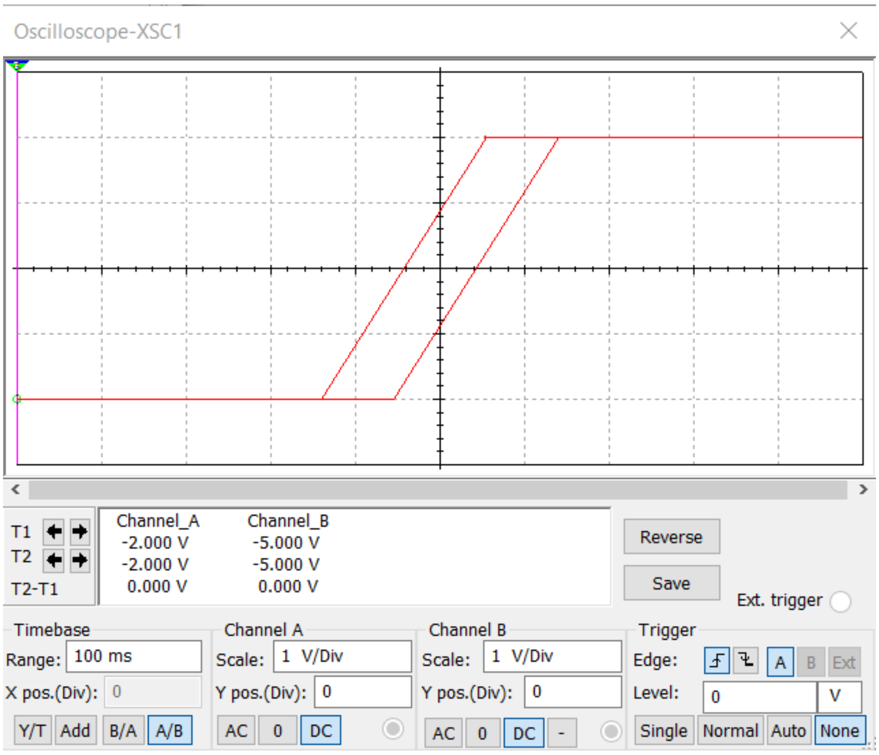

Figure 10. Transfer Characteristics of CW Hysteresis

4.6 CCW Loop Schmitt Trigger

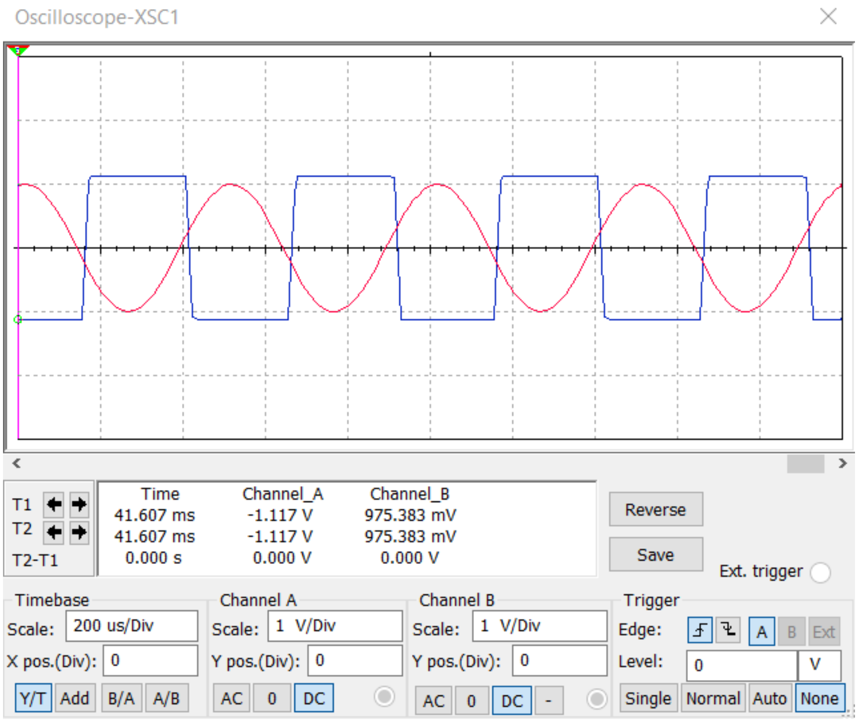

Figure 11. Transient Analysis of Input and Output

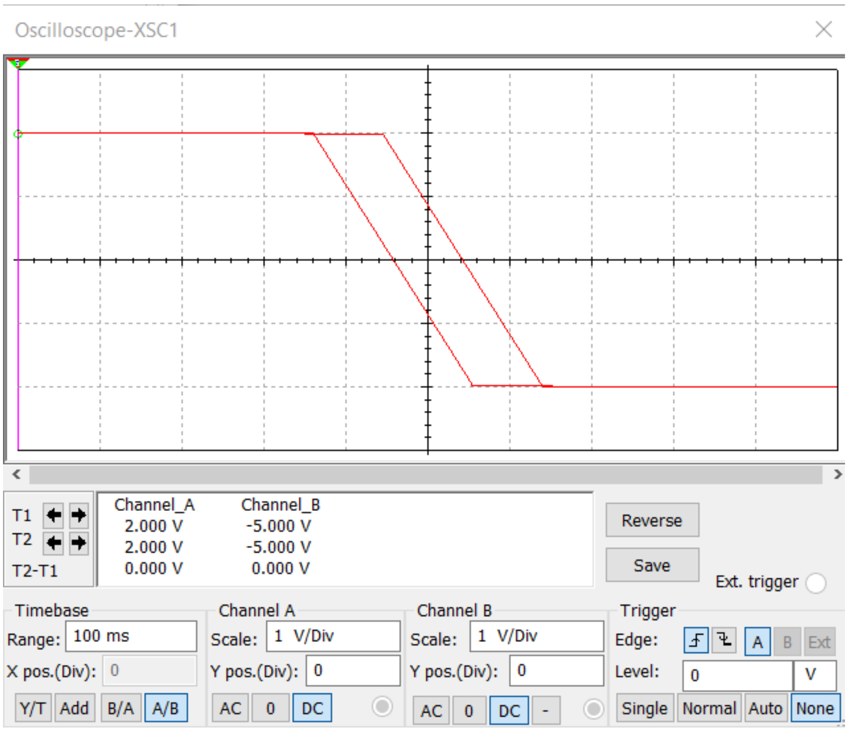

Figure 12. Transfer Characteristics of CCW Hysteresis

4.7 Tuning the Schmitt trigger

From the CCCII based Schmitt Trigger's circuit diagram, we can say that

$$I_X = \frac{V_{in} - V_X}{R1} \qquad\qquad I_{Z+} = \frac{0 - V_{Z+}}{R2}$$

Using the characteristic properties of CCCII and the above 2 equations and assuming saturation voltage of MOS used to be $\pm V_{SAT}$, we get

For $V_X > V_Y$,

$$V_{in} = V_{UT} = +V_{SAT} . \frac{R2}{R1 + R2 + R_X}$$

For $V_X < V_Y$,

$$V_{in} = V_{LT} = -V_{SAT} . \frac{R2}{R1 + R2 + R_X}$$

Therefore, we changing the value of input bias current, we can change the value of R_X, thereby changing the value of V_{UT} & V_{LT}. This means that for a Schmitt trigger with all its components fixed, we can **dynamically control the lower and upper threshold** values externally.

Tabulating the lower and upper threshold voltages from the hysteresis loop for varying input bias current keeping the other parameters fixed (as defined earlier).

Table 3. Variation of Threshold Voltages with change in Input Bias Current

Bias Current	R_X	V_{UT}- **Theoretical**	V_{UT}- **Practical**	V_{LT}- **Theoretical**	V_{LT}- **Practical**
1µA	62.60KΩ	+31.8mV	+35.6mV	-31.8mV	-35.6mV
2µA	50.50KΩ	+38.7mV	+40.3mV	-38.7mV	-40.3mV
5µA	35.71KΩ	+55.4mV	+48.9mV	-55.4mV	-48.9mV
10µA	28.87KΩ	+66.7mV	+54.0mV	-66.7mV	-54.0mV
20µA	26.66KΩ	+72.0mV	+57.4mV	-72.0mV	-57.4mV
50µA	26.10KΩ	+73.5mV	+58.9mV	-73.5mV	-58.9mV

As the value of bias current increases, the upper and lower threshold voltages also increase.

4.8 Improvements Offered by CCCII based Schmitt Trigger

Fewer passive components: In practical scenarios, passive components always lose energy while in use. We hence, need to minimize their use to prevent excessive attenuation. We can hence say that CCCII Schmitt Trigger will have lower power dissipation than CCII Schmitt Trigger

Control $\boldsymbol{V_{UT}}$ & $\boldsymbol{V_{LT}}$ values with external bias current: The threshold voltage values can be altered without changing the circuit parameters by changing the bias current I_B. Hence, The Schmitt Trigger can be said to be **Tuneable.**

Dual Output Circuit: Both inverting and non-inverting Schmitt trigger can be designed using a single CCCII block to provide both Clockwise and Counter-Clockwise Hysteresis.

Chapter 5: Application

5.1 Switch Debouncing

In this section, we will study the practical issue that occurs while switching and see how the Schmitt Trigger can help solve the issue.

5.1.1 Switch Bouncing

When a button of a switch is pressed, two metal contacts come into contact and the switch is toggled. Practically, this process isn't instantaneous. The metal contacts (connected to springs) move in and out of contact for a small time (called transient period) before settling into the final state.

In this transient period, multiple transition occurs similar to a ball falling from a height. While, this transient time is very quickly for human perception, one single switching causes multiple triggering, damaging the circuit in the long run and also causes errors in logical circuits.

A Schmitt Trigger will help in removing these multiple transitions.

Although, switch bouncing is a hardware phenomenon, for the sake of the experiment we recreate switch bouncing using Multisim Software (using Voltage Controlled SPST Bounce switch).

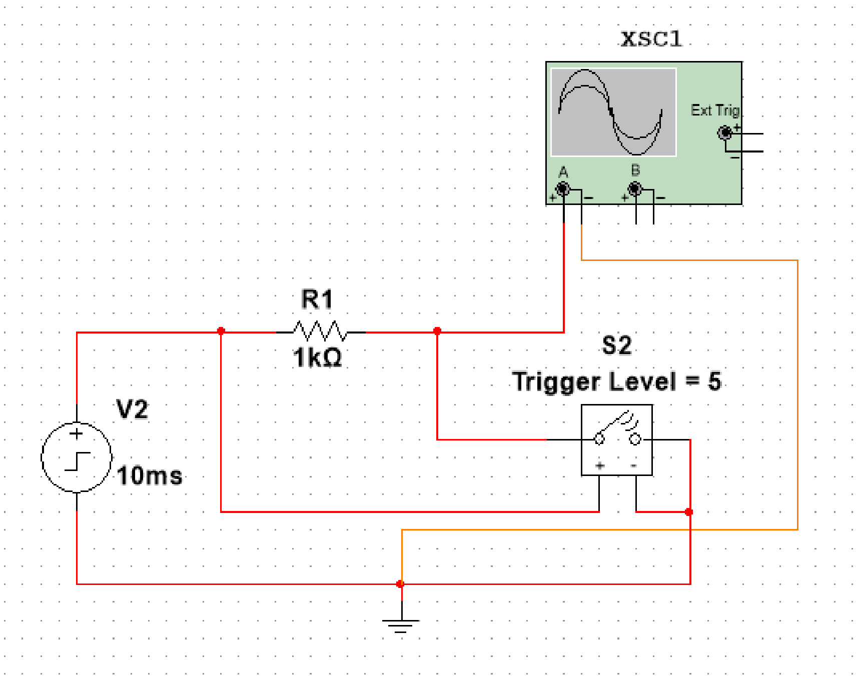

Figure 13. Circuit diagram for Switch Bouncing.

Using a Step Voltage moving from 4V to 6V after 10ms, with step up time of 10ns which trigger the switch at 5V such that

Time	Bounce state
0.0	0
0.2m	1
0.3m	0
0.6m	1
0.8m	0
1.8m	1
2.0m	0

Figure 14. Configurable Bounce Pattern

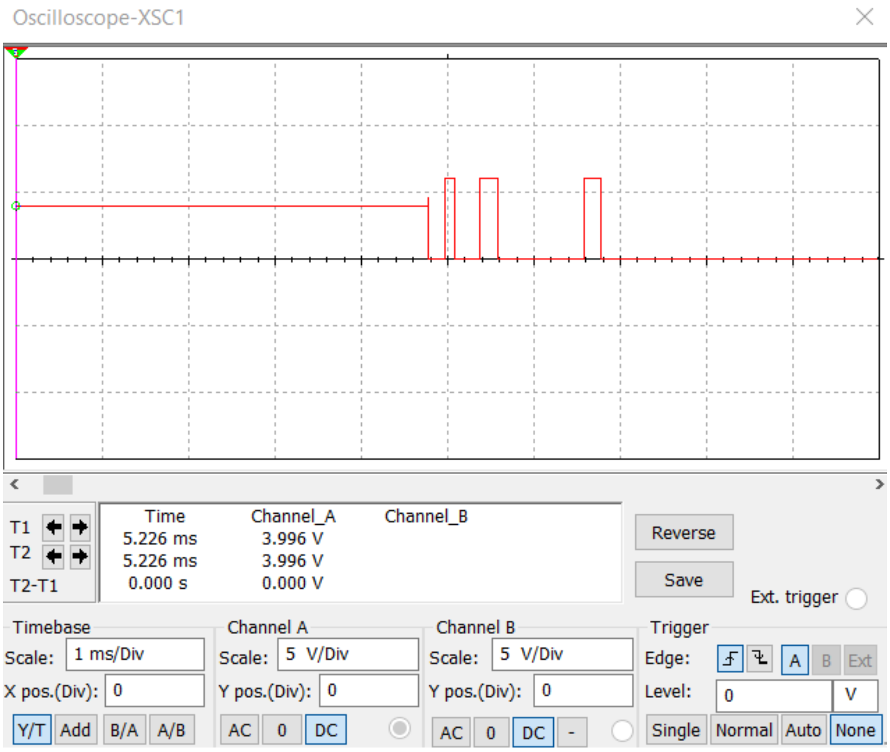

Figure 15. Software Switch Bouncing Result

Switch bouncing is not a major problem when we deal with the power circuits, but it causes problems while we are dealing with the logical or digital circuits like a counter, where then the results turn out to be wrong.

5.1.2 Switch Debouncing

Switch debouncing is the removal of multiple triggering that occurs during switch bouncing. It is a 2-stage process

A. Pass the Signal Through a **RC Circuit** which removes the multiple fluctuations from high to low within the transient time due to the charging/discharging of the capacitor.
B. Pass this Signal through a **Schmitt Trigger** which suppresses noise to give a debounced signal.

5.1.3 Stage A

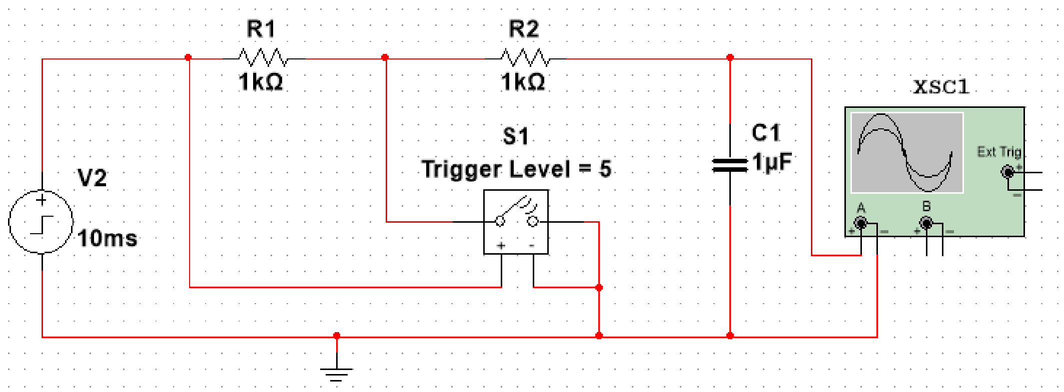

Figure 16. Circuit Diagram for Stage A.

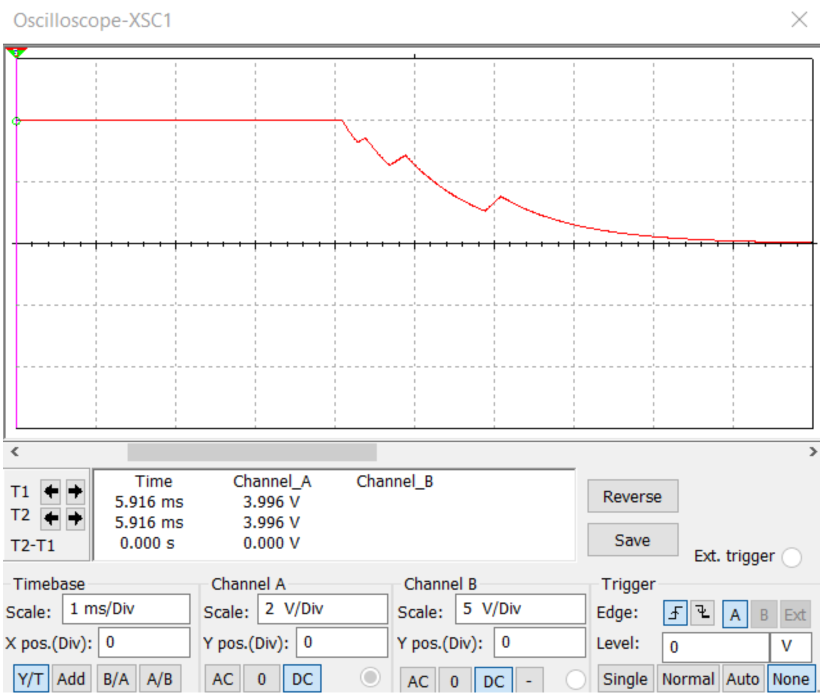

Figure 17. Output After RC Filtering

5.1.4 Stage B

The VSS has to set as a positive value such that the V_{LT} is between 4V to 0V, so that the transition will occur from $V_{SATH}\ to - V_{SATL}$ when the input to Schmitt Trigger transitions from High to Low.

The VDD has to set such that $V_{UT} > 4V$ so that the output does not transition back to V_{SATH} at any point during the transition from high to low.

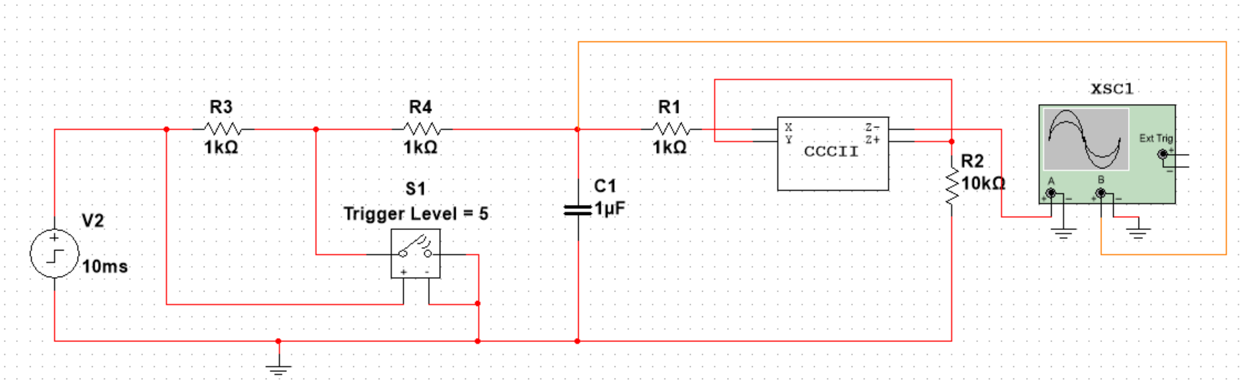

Figure 18. Final Switch Debouncing Circuit

At any point during the transition when $V_{in} < V_{LT}$, the output becomes V_{SATL} and maintains the value for the remainder of the time as $V_{in} > V_{UT}$, will not be satisfied by the circuit.

Hence, we obtain a Debounced Output Signal.

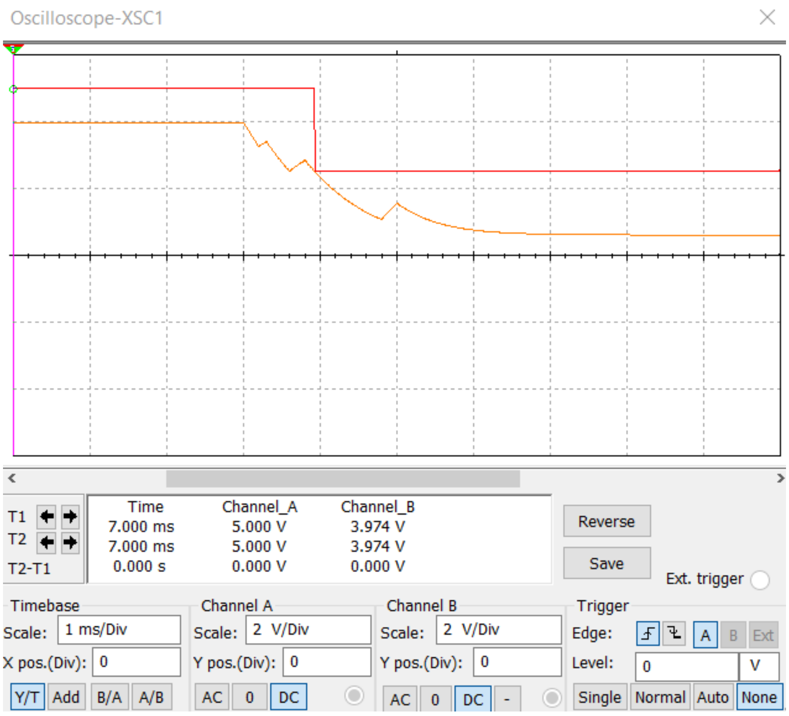

Figure 19. Transient Analysis of Output of Stage A and Output of Stage B

5.1.5 Feature of CCCII Based Schmitt Trigger

An Addition Advantage of using CCCII based Schmitt Trigger is the **ability to control the point during the transition time at which the switching occurs**.

This can be achieved by the means of changing the value of V_{LT} by changing the value of Input bias current I_B as already established. Since, the output of Stage A can be approximated to transition linearly from logic High to Low, by controlled the value of V_{LT}, the exact time of which of output logic from High to Low can be Controlled.

From the previous setup, if the value of I_B is reduced, then the value of V_{LT} reduces and the transition will occur later than the previous case as shown in the figure below.

Figure 20. Debounced Signal for different value of I_B

Hence, Switch Debouncing is a great practical application of Schmitt Trigger, which is enhanced by the additional tuneability of the CCCII based Schmitt Trigger.

Chapter 6: Comparison with Previous Works

Table 4. Comparison of Proposed Dual Output Schmitt Trigger

Ref	Building Block	Implemented with IC/Technology	Construction using BJT/MOS	Supply Voltage	Active Blocks	Resistances	Dual output
[1]	CCII+	-	MOS	5V	1	3	No
[3]	VDTA	ALA400	MOS	3.5V	1	1	Yes
[2]	OTRA	AD844	MOS	10V	1	1	No
[4]	CDTA	0.18µm	MOS	2.5V	1	2	No
[5]	CCCDTA	0.35µm TSMC	MOS	1V	1	0	No
[6]	MO-CTTA	AD844	MOS	5V	1	0	Yes
[1]	ZC-CDTA	0.18µm GPDK	MOS	0.85V	1	2	No
Our Work	CCCII	-	MOS	2V	1	2	Yes

Compared to CCII+, our work has lower power dissipation, lower supply voltage and has dual output.

Compared to VDTA, our work has higher power dissipation but lower supply voltage.

Compared to OTRA, our work has higher power dissipation but lower supply voltage and has dual output.

Compared to CDTA, our work has lower supply voltage and has dual output.

Compared to CCCDTA, our work has higher power dissipation and higher supply voltage but has dual output.

Compared to MO-CTTA, our work has higher power dissipation but lower supply voltage.

Compared to ZC-CDTA, our work has higher supply voltage but has dual output.

Chapter 7: Conclusion

This Project represents the work on the construction of a Schmitt Trigger using CCCII and its advantages over traditional Voltage mode Schmitt Triggers and Simple CCII Schmitt Trigger. CCCII was constructed using CMOS Transistors and its Port Parameters were verified and the safe region of operation was determined. Using this CCCII, Schmitt Trigger was constructed and the transient analysis and Hysteresis characteristics were observed for both the Clockwise (non-inverting) and Counter-Clockwise (inverting) Loop. The Value of Lower and Upper Threshold voltages were found to be tuneable by varying the value of the input bias current I_B and the relationship was found to be directly proportional.

Switch Debouncing of a software simulated Bounced Signal was performed using the said CCCII based Schmitt Trigger with the help of a RC Filter Circuit. The time of Transition of output (i.e., Switching of Circuit) was controlled using the input bias Current I_B.

Hence, Schmitt Trigger using Dual output Second Generation Current Controlled Conveyor was studied and implemented and its application was realised.

Chapter 8: Future Scope

I. Establishing the relationship between the theoretical and obtained value of the Intrinsic Resistance at Port X of the Current Controlled Conveyor by determining the MOS parameters.

II. Using No Passive Components in the construction the Schmitt Trigger, thereby drastically reducing the power dissipation when the circuit is in operation. This will also make fabrication of ICs Simpler and Faster.

III. Reducing the Supply Voltage of the CMOS Circuit to reduce Power Consumption of the circuit while in operation.

IV. Fabricating the Circuit using Software such as Cadence Virtuoso and Implementing a CMOS technology of parameter $\lambda/2$ less than 180nm.

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