**Ajay Kumar Jaiswal**

Phone : +358 406342621

Email ID : [ajayjaiswal12nov@gmail.com](mailto:ajayjaiswal12nov@gmail.com)

Address : Oulu, Finland

**SUMMARY**

DFT Verification specialist and dedicated team player with extensive knowledge of DFT concepts and hands-on expertise with the complex SoC verification and implementation of various advanced techniques to reduce verification efforts and better coverage completion.

**Highlights**

* Total 8+ years of industrial experience as **DFT Verification Engineer**
* Providing technical support and leading DFT verification tasks with young team members for end-to-end DFT verification activity closure
* Expertise on developing HVM reset test pattern and verify all the possible scenarios to access clock, power, reset bring-up.
* Good knowledge on SOC and IP DFT verification flow
* Experience on JTAG, TAP, TAPLink, BSCAN, DPD IP, IDV, STF, REGSCAN, CRAM Unload verification and architecture
* GPIO and PLL verification by using JTAG
* Implementing random and directed testcases for completing functional and code coverage 100%
* Creating the class-based verification environment using SV, OVM, UVM
* Implementing Makefile to run different testcases and code coverage setup
* Experience on VCS, DVE, Verdi, Questasim and various pre/post-Si validation tools
* Provided pre-amble and mid-amble patterns to MBIST and Post-Si Test team
* Direct experience in silicon bring-up and post-si debug/diagnosis on remote ATE

**TECHNICAL SKILLS**

* Hardware Languages : Verilog, System Verilog
* EDA Tools : VCS, DVE, Verdi, Questasim
* Protocol Knowledge : JTAG, STF, TAP2SB, AXI4lite, AHB
* Scripting Languages : TCL, Perl, Makefile, Python basics
* Version Control tools : ClearCase, GIT and ICM, P4
* Programing Skills : C, C++
* Verification Methodology : UVM, OVM

**WORK HISTORY**

* Nokia Networks and Solutions: 0 years 6 month. Oulu, Finland (Currently Working)
* Intel Technologies: 2 years 3 months. Bangalore, India
* Eximius Design (Wipro): 4 months. Bangalore, India
* Altran (Capgemini Engg.): 2 years 6 months
* Wipro: 2 years 3 months. Pune, India

**EDUCATION**

* PG-Diploma in VLSI & Embedded Systems (2014) from CDAC Noida
* B. Tech. in Electronics & Communication Engineering (2013) from UPTU

**PROFESSIONAL EXPERIENCE**

**Project 1: NextGen 5G Antenna systems**

**Duration: June’22-Currently on going**

**Description:** Top level verification tasks of 5G antenna SOC

**HDL:** Verilog/VHDL

**Methdology:** UVM

**EDA Tool:** VCS, Verdi, Questasim, DVT

**Responsibilities:** Working on testability and DnT features for the complex antenna top level SoC. Responsibilities includes develop and debug verification testcases and test plan and debug the directed and random test scenarios. Connectivity checks to all the blocks of SoC using TAP.

**Project 2: Regscan and CRAM unload design verification of FPGA tile using DFT Techniques**

**Duration: Oct’21-June’22**

**Description:** Regscan (debug feature) is to check IPs having scan registers can write/read/shift data to IOs. CRAM unload is a process to read the data from CRAM which were loaded by using backdoor access.

**HDL:** Verilog

**Methdology:** UVM

**EDA Tool:** VCS, Verdi

**Responsibilities:** Leading a small team of 3 engineers and defining day to day tasks with the help of management and making sure to be on track and smooth closure of project. Verification env setup by utilizing already existing database, debugging, porting, and modifying the files with latest required information as per the project guidelines. Write test plan, simulation setup and verification of Regscan and CRAM unload features of the FPGA tile. Mentoring an intern and helping him to grow in his career.

**Project 3: DFx verification of vision SOC**

**Duration: Nov’19-Sept’21**

**Description:** Vision based SOC which consists of 4 cores along with vision, media etc blocks along with graphics subsystem, pciess. All blocks/subsytems has multiple interfaces (Jtag, AXI).

**HDL:** Verilog

**Methdology:** UVM

**EDA Tool:** VCS, Verdi, VTPSim

**Responsibilities:** working on HVM reset implementation and validation using JTAG protocol along with scan pattern generation and debug. Code coverage collection and debug to identify the gap and suggest team to cover the missing test scenarios. Providing technical support to young team members in architecture understanding, testplan creation and debug.

Working on post-si test pattern generation of HVM Reset, PLL, BSCAN. Work closely with post-Si test team and provide them debug support on the tester.

**Project 4: DFX verification of server based SOC**

**Duration: Jan’19-Oct’19**

**Description:** Server based SOC which consists of multiple high speed blocks along with graphics subsystem, pciess. All blocks/subsytems has multiple interfaces (Jtag, STF, IOSF-SB).

**HDL:** Verilog

**Methdology:** OVM, ITPP

**EDA Tool:** VCS, Verdi

**Responsibilities:** working on STF (standard test format) and JTAG protocol verification along with mentoring team of 3 engineers. Collect required data from specification and provide debug support to the team.

**Project 5: Verification of DPD (Digital pre-distortion) IP for 5G antenna system**

**Duration: May’18-Dec’18**

**Description:** DPD top-level architecture has TX, FB and memory blocks. TX block uses FIR filters to convert non-linear data into linear data and pass to the capture points, memories stores data from the capture points and provide access to

the DMA to read the data. It has 3 interfaces AXI stream for Data processing, AXI4-Lite for providing register access controls, and DMA interface to read/write the memory. Matlab used as reference model.

**HDL:** VHDL

**Methodology:** UVM

**EDA Tools:** VCS, DVE, Questasim

**Responsibilities:** Responsible to create testcases/sequences and matlab reference model,debug of VHDL RTL and Matlab Model. Read captured result by using DMA. Worked on code coverage setup and analysis for Questa and VCS simulators.

**Project 6: DFX verification of base die for computer system chip**

**Duration: Mar’17-Apr’18**

**Description:** - The SOC has 2 dies, Base and compute. JTAG connects all the IPs by using TAPLink network architecture. All IPs having alternate path to access by using Jtag. IDV (in-die variants) used to maintain the same frequency throughout the SOC which is being generated from ports. Security policies are defined to block/unblock access to the IPs.

**HDL:**Verilog

**Verification Methodology:**OVM

**EDA Tools:** VCS, DVE, Verdi

**Responsibilities:** Creating test plan, write OVM sequences/testcases for TapLink, STF, IDV, IOV, VDM, ODI, DFx\_Aggregator security.

Verification of GPIO in different modes.

Worked on UPF based simulation and toggle coverage setup and analysis as well.

**Project 7: DFX Verification of mobile communication system**

**Duration: Dec’14-Oct’16**

**Description:** The Project involves SoC Verification of Mobile communication system with C/VHDL/verilog environment. The chip Verification includes several IPs like DMAC, USB, PCIe, SDMMC, LTE, 3g, 2g etc along with modules DnT, CGU, SCU etc.

**HDL:** Verilog

**Verification Methodology:** C, UVM

**EDA Tools:** VCS, DVE

**Responsiblities:** Creating verification Objectives for DFx flow. To plan and code the testcases checking the connectivity of GPIO PADs and IPs with JTAG port with different tetsmodes.

Worked on TCL script for automating the testcases.

Worked on unit delay GLS debug for 3 months during the end phase of project