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Preface and specification

In this project, we aimed to design a bandpass filter for a neural measurement system. The neural measurement system is composed of an electrode array for signal recording, multiple low noise amplifiers for signal amplification, multiplexers and A/D converters for digitalization of the incoming data and a digital ASIC for preprocessing and signal processing.

The energy of the system is constrained to a low power design. Due to the limitation of the maximum applied field to the brain the transmitted power cannot be too large. Furthermore the heat dissipation has to be considered, otherwise a small increase in temperature will lead to tissue damage. So here the maximum power of each amplifier is 180 µW.

Another important constraint is the low noise. For signals detected in this system are Local Field Potentials (LEP) and Neural Spikes. The Local Field Potentials record signal of a large number of contributing neurons for each electrode. It represents the activity of a specific observed area. It can be seen as an envelope of spike activity. The amplitude of LEP is usually smaller than 5mV and the bandwidth is from 1Hz to 250Hz. Spikers are recorded from a dedicated neuron. The Amplitude is much higher which is from 50 to 500 µV and bandwidth is from 1Hz to 10kHz. Due to the attributes of these two signals we need to design a bandpass filter with a suitable bandwidth. Here the interesting bandwidth is from 0.1kHz to 1kHz. Since he amplifier is very noise sensitive, the input referred noise is limited to 20 to 30 $nV/\sqrt{Hz}$.

Due to the fact the incoming signals are in the microvolt range, a high amplification is needed. Here a gain of 40 dB is needed in this bandpass filter.

Description of amplifier topology

For the bandpass filter we designed consists three parts. The first part is an Operational Amplifier. The second part is that we add a highpass filter as the feedback to the Opamp. The third part is a voltage buffer. In the project we need to design the first two parts the Opamp and the highpass feedback to achieve its bandpass attribute. The figure 1 Shows the profile of the whole system.

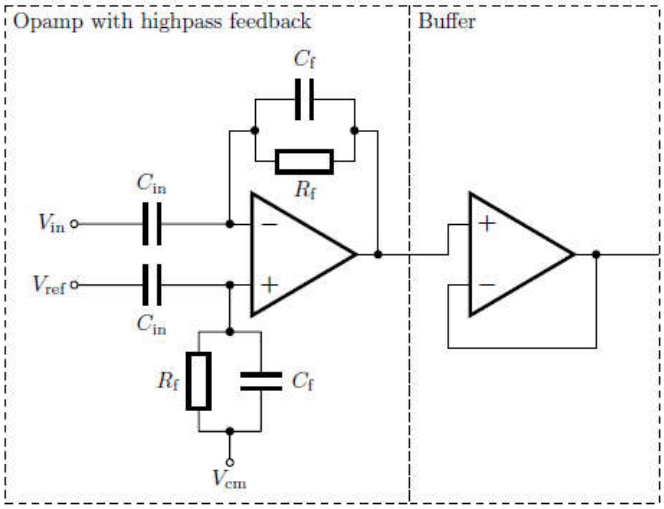

Figure 1: Topology for a low noise amplifier and bandwidth filter

The operational amplifier itself has a low pass characteristic. The Opamp in this project is a two stage amplifier. The first stage amplifier is a differential amplifier with a current mirror. The second stage is common source amplifier with active load. Besides, use current mirror to supply bias current for each MOSFET. In this project, we use 350nm PDK from AMS. The supply voltage for this process is 3.3V.

The first stage differential amplifier is composed of four MOSFETs. M1 and M2 compose the differential amplifier. We can supply two input signals from the gate of each MOSFET. Each MOSFET works as a common source amplifier. M3 and M4 compose the current mirror. The potential of drain is equal to the voltage of gate in M3. So this current mirror can mirror the drain current of M1 to the other side. Finally the output can be seen for one side of differential amplifier. And we need to supply same common mode voltage to the gates of M1 and M2. The common voltage is used to set the operation point. Usually we set common mode voltage to Vdd/2 to have a larger input range which can make sure the MOSFET to work in saturation region. By using differential amplifier as the first stage a lot of environment noise is cancelled. And M8 and M5 compose another current mirror which supplies bias current for differential amplifier. In DC analysis, the bias current in each side of differential amplifier is equal to half of the bias current (Ibias). And difference in two inputs of differential amplifier will be amplified and seen at the output.

The second stage is a common source amplifier with an active load. M8 and M6 compose a current mirror to supply bias current to M7. And also it can make the output resistance larger to get a higher gain. And the output voltage of the first gate is the input of the second stage.

I think one the reason to use two stage amplifier is that it can decrease the gain on each MOSFET. So the drain current will not too large as single stage that may destroy the amplifier.

And about input referred noise of two stage amplifier, the first stage renders the noise second stage negligible. So we choose a high gain low noise first stage amplifier.

After design of the amplifier we have to cheek the phase margin. The larger phase margin is, the smaller overshoot it has and the system is more stable. Usually we want to achieve a phase margin larger than 60 degree. And in this Opamp, we have two poles in the circuit. One dominant pole at the output. One nondominant pole is at the output of first stage. Totally it will have a phase shift about 180 degree. And we use miller capacitor with a resistance to shift these two poles to achieve a reasonable phase margin.

We aimed to get a bandpass filter. A bandpass can be seen as a combination of low pass and a high pass. So we add a feedback with highpass. And from the theory of Opamp with feedback, we know that if the open loop gain is much large than the feedback gain, then the total gain of closed loop is robustly equal to feedback gain. So in this project we actually define the gain by feedback parameter, but we have to make sure the open loop gain of Opamp is high enough. For highpass circuit we use a RC filter to suppress the low frequencies in the ground signal.

Design of the OPAMP

We use the GMID method to design the OPAMP. For GMID method we have to choose an inversion coefficient. From the GMID plot of ams350 we can read Gm/Id, Gds/Id and W/Id after choosing a reasonable IC and length of MOSFET.

For amplifier we usually choose a small IC around 1, because choosing IC around 1, we can get the best transconductance of MOSFET (Gm). We usually choose IC around 10 for the current mirror, because the larger IC will provide larger rds of MOSFET. The rds of current mirror is the output resistance amplifier and also can protect the amplifier better from outside influence.

About length of MOSFET, it is also proportional to the rds of MOSFET. In our project we want to have an open loop gain which is far larger than 40dB, so we should not choose small length.

Furthermore, to achieve lower input referred noise, we need to choose a low noise high gain amplifier. So a longer length for current mirror M3 and M4 is chosen. It will be explained later in noise analysis.

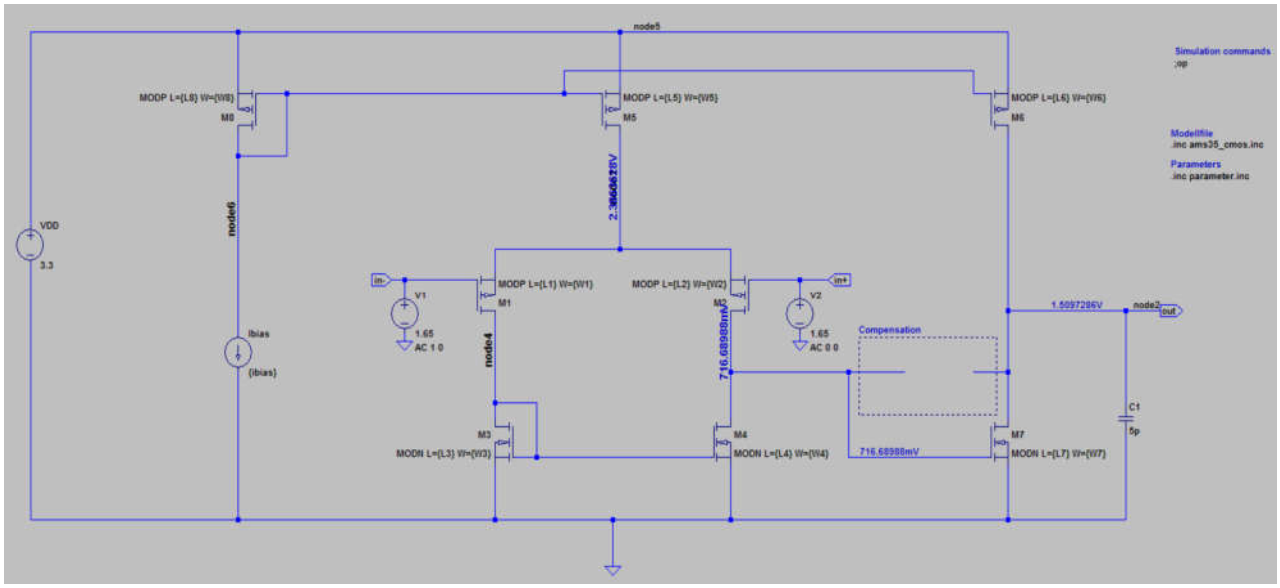

Figure 2: Opamp with compensation of RC circuit

In the project, IC and Length chosen for each MOSFET is shown in Table1.

	M1=M2	M3=M4	M5=M6=M8	M7
Length(µV)	1.05	10.05	1.05	1.05
IC	0.7	10	10	8

Table 1: IC and Length for each MOSFET

$$A_{total} = A_{1st} * A_{2nd} \qquad (3.1)$$

$$A_{1st} = \frac{g_{m2}}{g_{ds2} + g_{ds4}} = \frac{\frac{g_{m2}}{I_{D1}}}{\frac{g_{m2}}{I_{D1}} + \frac{g_{m4}}{I_{D1}}} \quad (3.2)$$

$$A_{2nd} = \frac{g_{m7}}{g_{ds7} + g_{ds6}} = \frac{\frac{g_{m7}}{I_D}}{\frac{g_{m7}}{I_D} + \frac{g_{m6}}{I_D}} \quad (3.3)$$

According to maximum power of each MOSFET is 180nw and the given voltage is 3.3V, we can calculate the maximum bias current should smaller than 54 μA. Here in this project we choose 44 μA. By changing the bias current the parameter of each MOSFET and the noise will be influenced also.

From equation 3.1, the total gain of the open loop OPAMP equal to the product of each stage gain. We have to make sure total gain is much large than 40dB. We choose IC = 0.7 for M1 and M2 and IC =10 for M3 and M4 to make the first gain A larger. According to the length we chosen, we can read parameters from GMID plot to calculate gain based on equation 3.2. Based on the parameters we read roughly, we got the result first gain A1=50.45dB.

The same way to calculate the second gain when we choose IC =10 for M6 and IC= 8 for M7. Usually the first stage gain should be larger than the second stage. And also considering the operating point, we would like to make the output voltage roughly equal to Vdd/2 to have a large output range, so here we choose IC =8 for M7. According to the result we read, A2 is robustly equal to 43dB. And we can do the Dc simulation to see the operating point of the output is 1.5v.

So total gain of the opamp is equal to 93.49dB, which is far larger than 40dB. This result will guarantee that the closed loop gain will roughly equal to the gain of feedback loop.

After we have already design the Opamp, we check the phase margin which is approximately 0. So we need use Miller capacitor to separate both dominant pole and non-dominant pole. By only adding a miller capacitor, it will produce undesired positive zero. The miller capacitor adds another feedforward path between input and output of second stage, which will lead to positive zero.

So what we need is to use Miller capacitor and resistance in series. From small signal model of the circuit, we can get the equation (3.4) to calculate the zero which is induced by miller capacitor. The frequency of zero is calculated from equation (3.5);

$$\frac{1}{Rc+\frac{1}{SCc}}V = gm_7 V \tag{3.4}$$

$$s_{zero} = w_{zero} = -\frac{1}{Cc(Rc - 1/gm_7)} \tag{3.5}$$

From frequency of zero, we have several options. First, to choose a small Rc to make this positive pole to go infinite. However this method limits the phase margin, increasing Cc to shift non-dominant pole to left will stop at some Cc that further increasing will not increase phase margin anymore. So it is not really worked here. The second method is to increase Rc to make it change to a negative zero. And we can see from equation (3.5) that increasing Rc will lead negative pole smaller. Actually we can use negative zero to cancel or compensate the phase shift of non-dominant pole. It will lead to a phase margin larger than 45 degree.

According to method given in tutorial, we choose Cc'= 25pf according to equation (3.6).

(3.6)

And to calculate Rc according to equation (3.7),Rc=6.7kΩ

$$Rc = \frac{1}{1.7\omega_t Cc} \tag{3.7}$$

But the simulation result shows that although the phase margin is about 100 degree, it causes the lead compensation. It means the gain doesn't decrease steadily. So we calculate a several time to set Rc equal to 3.2kΩ and get a phase margin about 87 degree. The result is good enough, but Cc will be changed later during the feedback design to limit the bandwidth from 0.1Hz to 1KHz.

Design of the filter with feedback

After finishing the design of Opamp, we move on to design the highpass filter. The transfer function of highpass circuit given is equation (4.1).

$$H_{Hp} = \frac{sR_fC_{in}}{1+sR_fC_f} \tag{4.1}$$

$$H(jw)|_{\omega\to\infty} = \frac{C_{in}}{C_f} \tag{4.2}$$

$$|H(jw)| = \frac{C_{in}}{C_f} = 40dB = 100 \tag{4.3}$$

Since the open loop gain is much larger than 40dB. So the closed loop gain is limited by feedback. According the equation (4.2) for frequency goes to infinite, the gain is robustly equal to Cin by Cf. From equation (4.3) Cin is about 100 times large than Cf. Based on the range given, we choose Cin =15p and Cf=150f.

And also from the equation (4.1), a high pass filter will induce a negative pole. According to the requirement to let the pole below 1Hz. We choose Rf=8 TΩ.

Next step is to set the bandwidth. The cutoff frequency of the bandpass filter is 1kHz. So the gain at 1KHz should be approximate 37dB. By increasing the Cc, we can move the dominant pole further left. The dominant pole of Opamp is just the cutoff frequency. Finally we choose Cc=620p. And also increasing Cc will only increase the phase margin to make the system more stable.

Finally the parameters we choose for each element are shown in table 2 and 3.

	M1=M2	M3=M4	M5=M6=M8	M7
IC	0.7	10	10	8
Length(μm)	1.05	10.05	1.05	1.05
Width(μm)	275	62.8	37	18.2

Table2. MOSFET parameter choosing by GMID

Rc(Ω)	Cc(F)	Cin(F)	Cf(F)	Rf(Ω)
3.2k	620p	15p	150f	8T

Table3. Compensation and Highpass filter

Result analysis

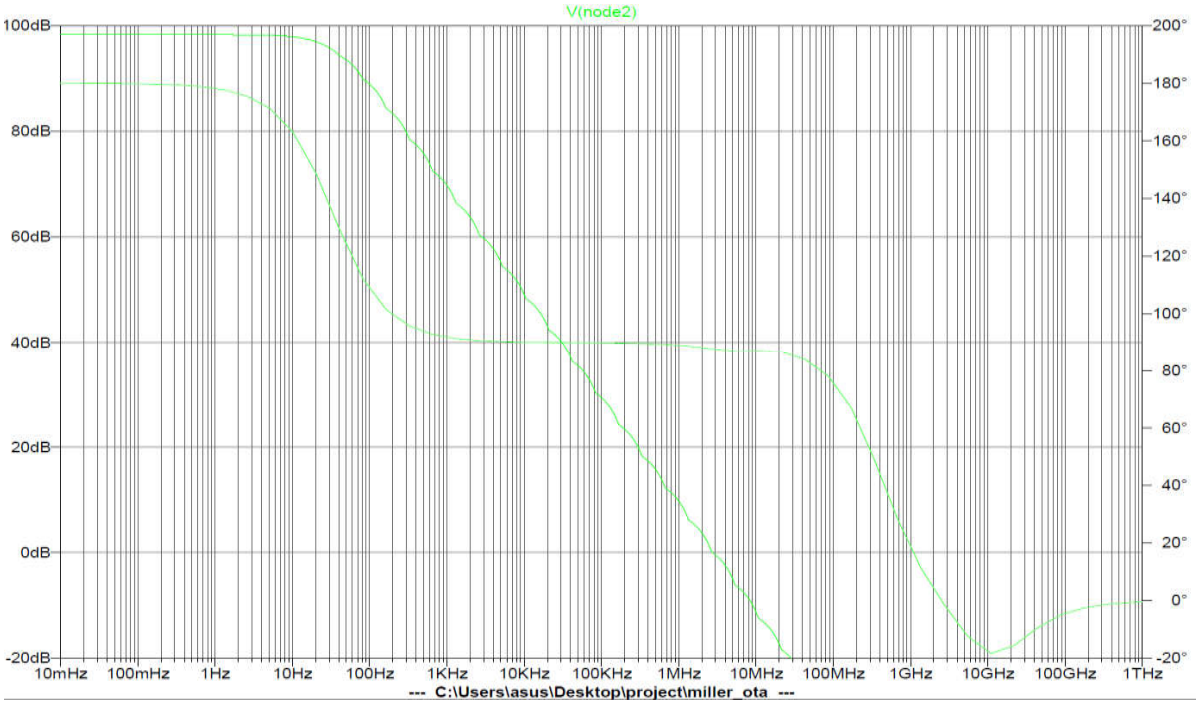

Figure 5.1: Bode plot of Opamp with Rc compensation

The figure 5.1 is the output behavior of Opamp with compensation which Rc=3.2kΩ and Cc=25p. The phase margin is about 87 degree.

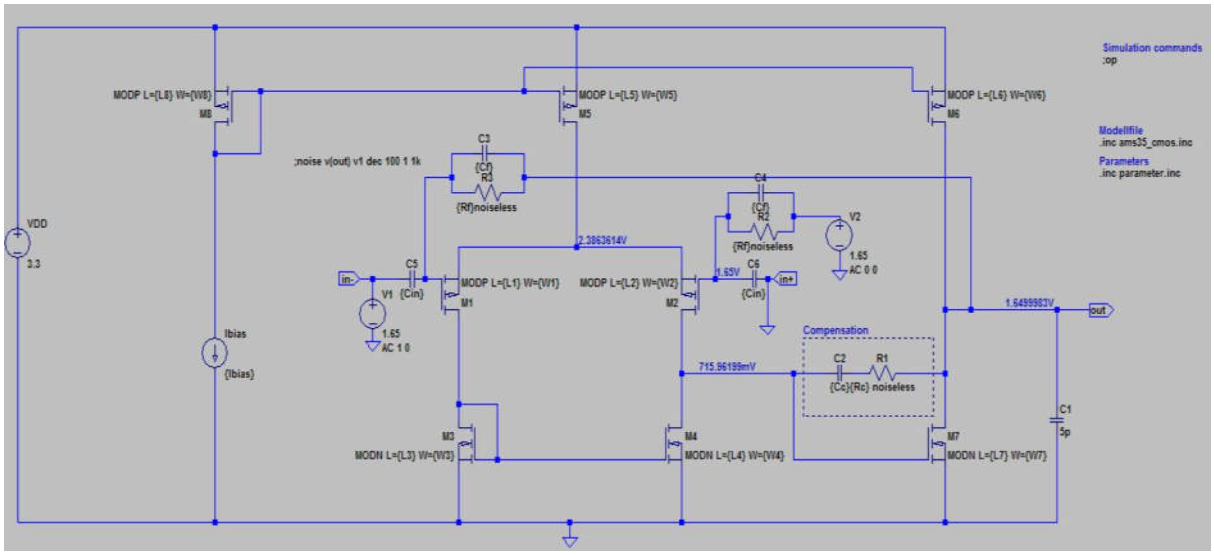

Figure 5.2: Opamp with highpass feedback

Figure 5.2 shows the circuit opamp with the highpass feedback. And the closed output behavior is shown in Figure 5.3. At the 3dB-cutoff (37dB) the frequency is 1.030kHz and0.12Hz. So the bandwidth of this bandpass filter is from 0.12Hz to1.030kHz which meet the requirement precisely. And the gain during the bandpass is exactly 40dB.

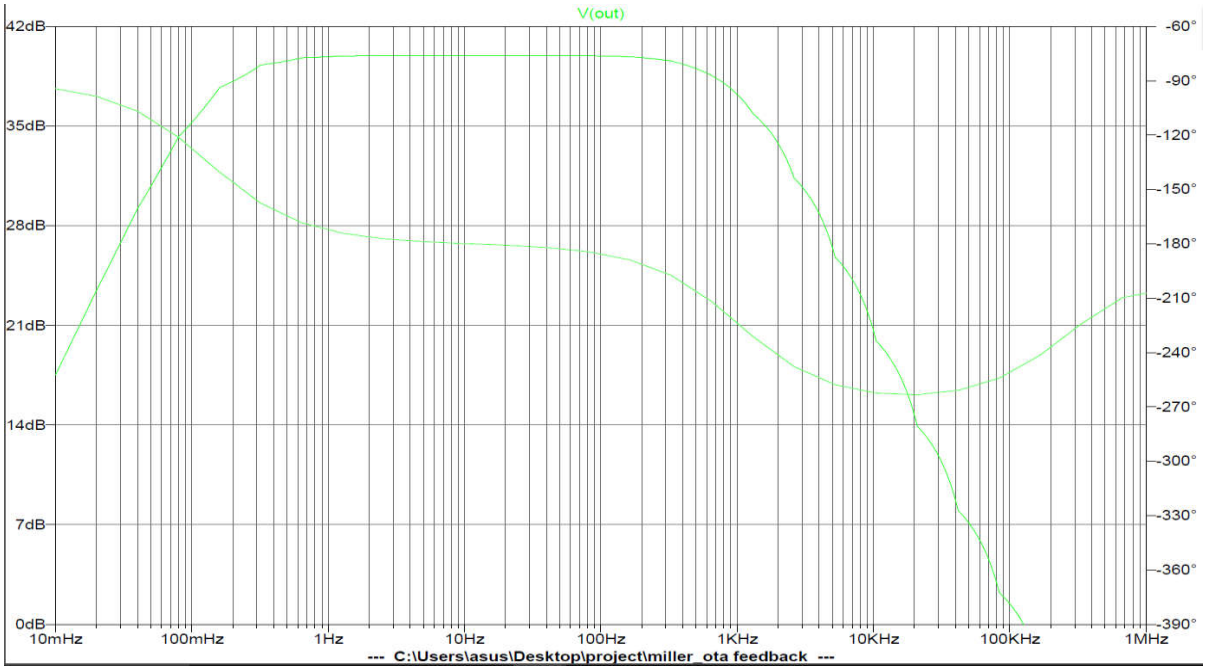

Figure 5.2: The output behavior of closed loop system

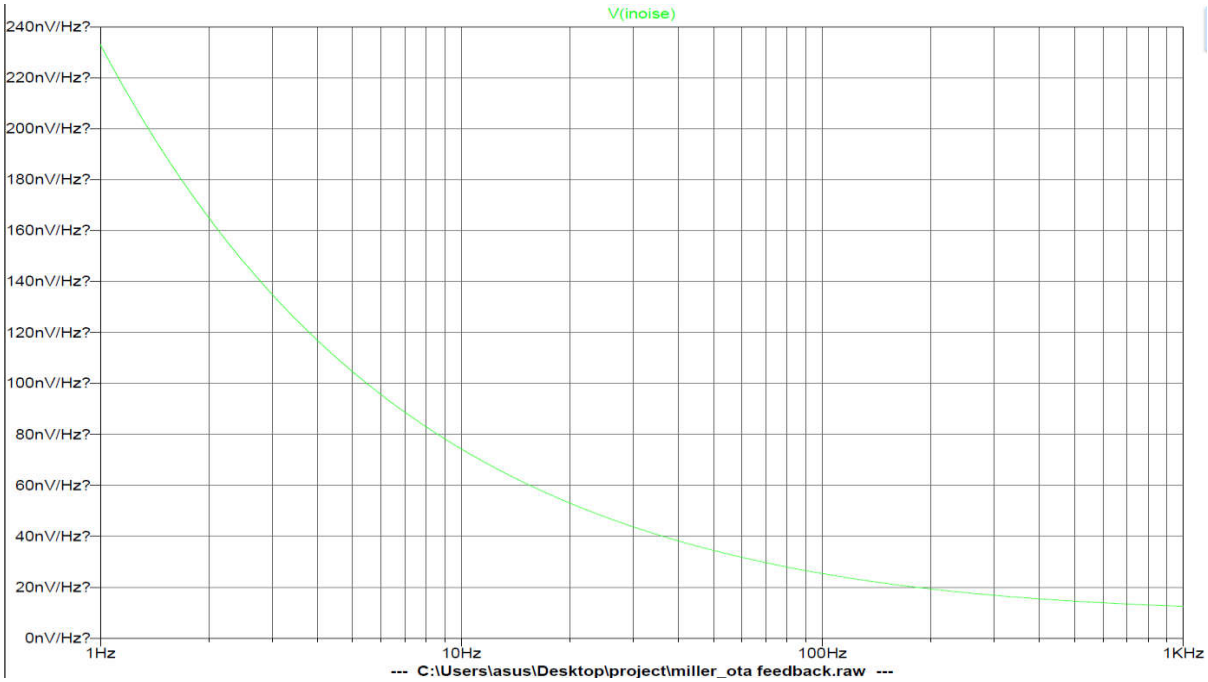

Figure 5.3: Input noise behavior of the closed loop system

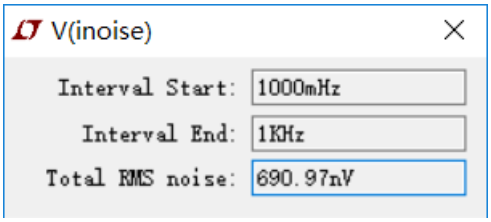

Figure 5.4 total Input referred noise in the bandwidth

The last part of the project result analysis is to check the noise behavior. In the circuit analysis we use the normalized power to represent the noise. In the project, we assume Rc and Rf are ideal resistance which will not produce thermal noise. So the noise of this bandpass filter is only produced from the MOSFET. Equation (5.1) is the input referred noise. From equation (5.1), the noise of MOSFET is composed of thermal noise and the flicker noise, which can be seen from figure 5.3. At low frequency the flicker noise dominates and at high frequency the thermal noise dominates.

$$v_{in}^{2}(f) = 4kT(\frac{2}{3})\frac{1}{gm} + \frac{k}{wLCo'f} \qquad (5.1)$$

Furthermore from equation (5.1), we can see that input referred noise is inversely proportional to transconductance of MOSFET and channel Length. That is why we choose IC=0.7 for M1 and M2 and Channel length 10.05 μm for M3 and M4 to decrease the input referred noise. And the required input referred noise is from $20nv/\sqrt{Hz}$ to $30nv/\sqrt{Hz}$. From equation 5.2, we can calculate the total noise in the bandwidth from 1Hz to 1KHz. The range is from 632.45 to 948.68nV.

$$V_{in} = V_{inrms} \cdot \sqrt{bandwidth} \qquad (5.2)$$

Figure 5.4 shows the total input referred noise in the bandwidth is 690.97nV that is just in the range of the requirement.

From the simulation result, the bandpass filter we designed achieve gain of 40dB, bandwidth is from 0.12Hz to 1.030KHz and a low noise behavior.