# AJAY KRISHNA

ajaykrishna1111@utexas.edu | (512) 299-7378 | linkedin.com/in/ajay-krishna-ananda-kumar

## EDUCATION

**The University of Texas at Austin** **4.0/4.0**
Master of Science: Electrical and Computer Engineering Fall'18 – Spring'20
Coursework: Computer Architecture**,** CompArch: Parallelism and Locality**,** Superscalar Microprocessor Architecture, VLSI, High-Speed Computer Arithmetic

**Anna University, Madras Institute of Technology Campus** **9.52/10.00**
Bachelor of Engineering: Electronics and Communication Engineering (2nd Rank) Fall'11 – Spring'15
Coursework: Digital Electronics and System Design, Electronic Circuits, Advanced DSP, Embedded Systems, Digital VLSI

## EXPERIENCE

**Performance Architecture Intern: Architecture-Level Power Modeling** **Samsung SARC**
AFFILIATED WITH TEAMS: CPU PACT, PERF. MODELING AND CORRELATION, RTL POWER & DESIGN, CAD May'19 – Aug'19

- Proposed detailed hier2powermodel mapping and improved the resolution of the CPU power models in spatial domain for accurate hotspot identification.
- Improved the accuracy of the sub-block level models by time-domain decomposition and various other Machine Learning approaches to guide power-aware microarchitecture design space exploration.

**Machine Learning (ML) based Power Modeling of Processors: Research** **UT Austin**
GRADUATE RESEARCH ASSISTANT AT SYSTEM-LEVEL ARCHITECTURE AND MODELLING GROUP UNDER DR. GERSTLAUER Jan'19 - Present

- Synthesized and simulated RISC-V CPUs for different workload scenarios; analyzed and attributed power consumption of various sub-blocks in the design.
- Identified minimal set of high-level features with high correlation to power; applied different ML models and techniques for accurate power modeling (>95% average accuracy) of sub-blocks.

**SoC Low-Power Design Engineer** **Qualcomm Inc**
AFFILIATED WITH TEAMS: POWER ARCHITECTURE, SOC POWER, SYNTHESIS, PD, RTL DESIGN, DV, CAD Jun'15 – Jun'18

- Developed Power intent [**UPF** 2.0, CPF] for **Snapdragon** SoCs with multiple low power islands (LPI), 100+ power domains - multiple supply rails, power switches & muxes - with diverse isolation and retention requirements.
- Owned **Low Power static verification** [CLP] flow from RTL2GDSII at SoC level. Worked with core power and PD teams to flush out UPF propagation through all phases of the execution cycle: 8+ months, **~90mm2 die area @7nm**.
- Devised a flow to make SoC LP-verification independent of HM synthesis – **Reduced effective time** (1week -> 2days).
- Estimated **dynamic power consumption** [PTPX] for modem and multimedia use cases and for PDN design.
- Improved the accuracy of **memory inrush analysis** flow – reduced number of decaps needed – **area reduction**.
- Worked on setting up the **leakage power budgets** for SoCs - 28LP CMOS to 7FF FinFet; measured and correlated the leakage power estimates against budgets at all netlisting levels.
- Developed/involved with the **PMU** RTL design upgrades for LPI support (+**CDC** +**Lint**), design of **thermal mitigation** logic, closed loop **AVS** digital controller design and integration, and **CAN** based wakeup for automotive market SoC.
- Debugged and root caused corner case design bugs and fixed it as **metal-only ECOs** in short time **avoiding respin.**

**RTL Power Intern: Analysis and Reduction** **Qualcomm Inc**
AFFILIATED WITH TEAMS: RTL POWER & DESIGN May'14 – Jul'14

- Worked on PowerArtist - RTL power analysis; Surveyed various RTL power reduction techniques.

## PROJECTS

- **Efficient Data Partitioning for Deep Neural Networks Training -** Data, model and hybrid parallel partitioning in GPUs.
- **A Programmable Precision Multiplier for Neural Networks** – Analysis of Precision vs Performance-Power trade-off.
- **Assembler and cycle-accurate simulator** for LC-3b RISC ISA – supports virtual addressing, exception handling.
- **Evaluation of SRRIP, DRRIP, LRU** replacement on LLC for five workloads from SPEC CPU2006 suite using ChampSim.
- **Complex Event Processing based Hybrid Intrusion Detection System**, ICSCN - 2015 3rd International Conference.
- **Architecture independent BIST for embedded multipliers** in Cyclone II devices.

## TECHNICAL SKILLS

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|---|---|
| **HDL & PROGRAMMING** | Verilog, System Verilog (basics); C, C++, TCL, Perl, Python, CUDA, Regent, Bash |
| **TOOLS & SIMULATORS** | PTPX, CLP, PowerArtist, VC LP, Questa 0-in, Spyglass(basics), Verdi(debug), Formality(basics); GEM5, ChampSim, perf, PAPI, CACTI, SimPoints, NVProf, PIN |