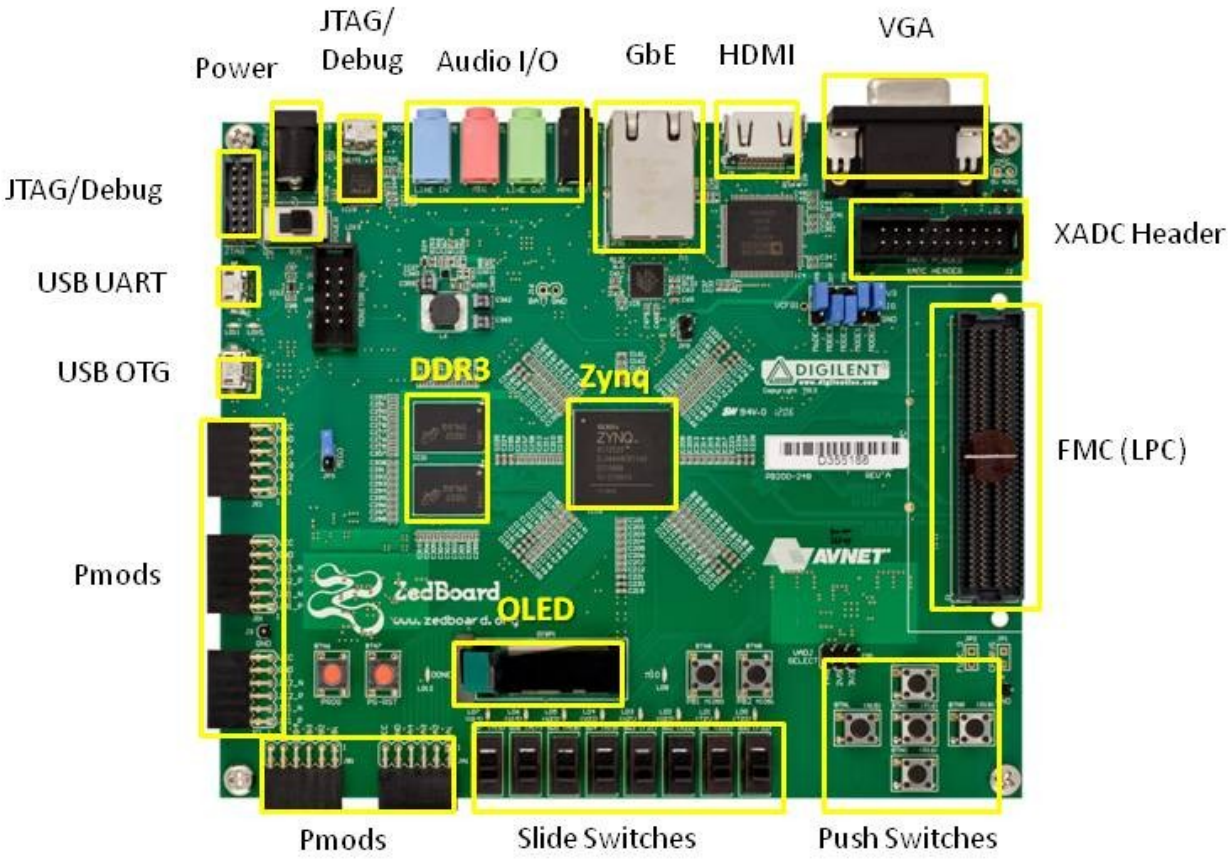
ZedBoard DAQ

Jia Fu Low
James Bueghly
Jovana Andrejevic

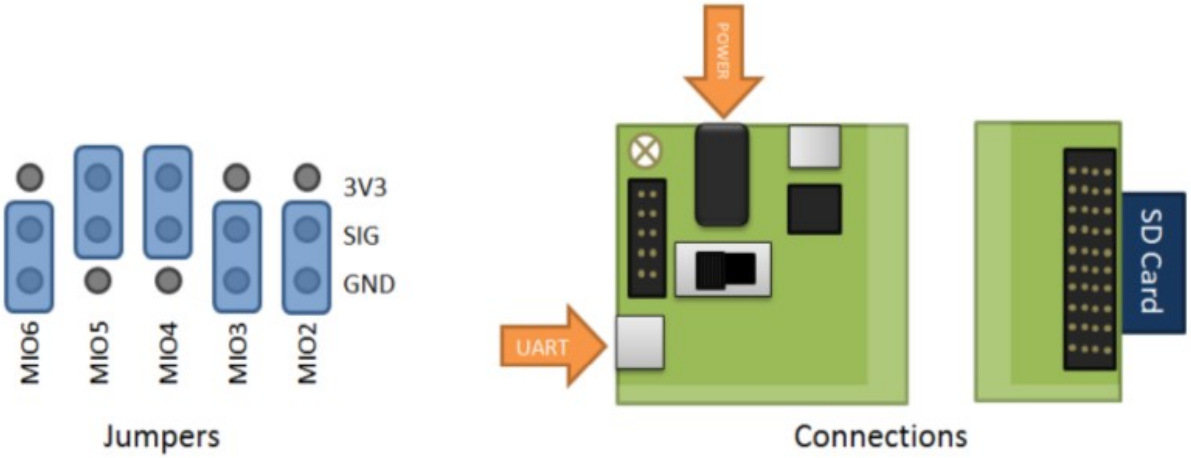
July 27, 2015

ZedBoard Schematic



* SD card cage and QSPI Flash reside on backside of board

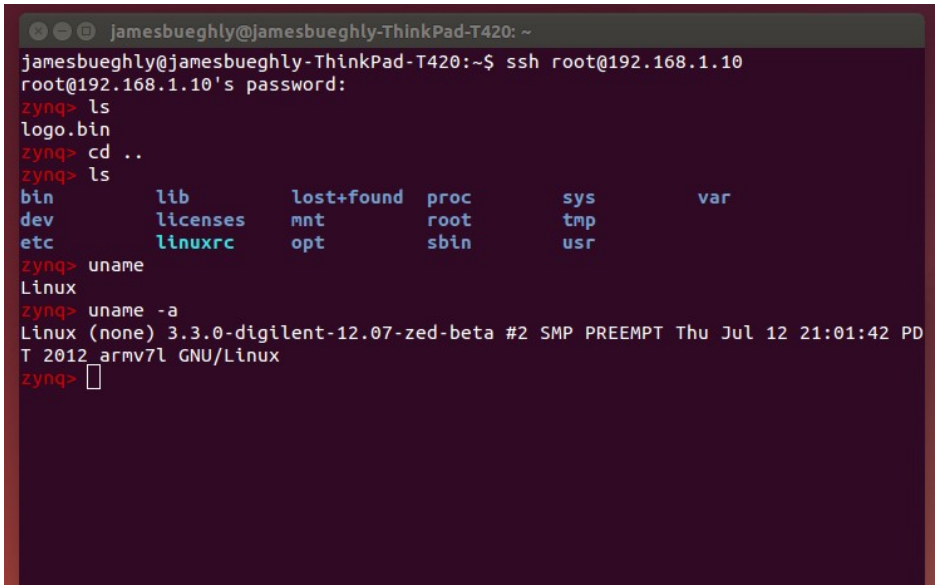
Booting Linux on Zynq



- Boot from SD card using GTKterm terminal emulator
- UART connection settings:
  - Port: /dev/ttyACM0
  - Baud rate: 115200
- Simple built-in commands to access peripherals
  - write_led

Connecting Via Ethernet

- Standard ethernet connection between ZedBoard and PC
- Network properties
  - IP address: 192.168.1.1
  - Subnet mask: 255.255.255.0
  - Gateway: blank
- Connect via SSH → file transfer via SCP

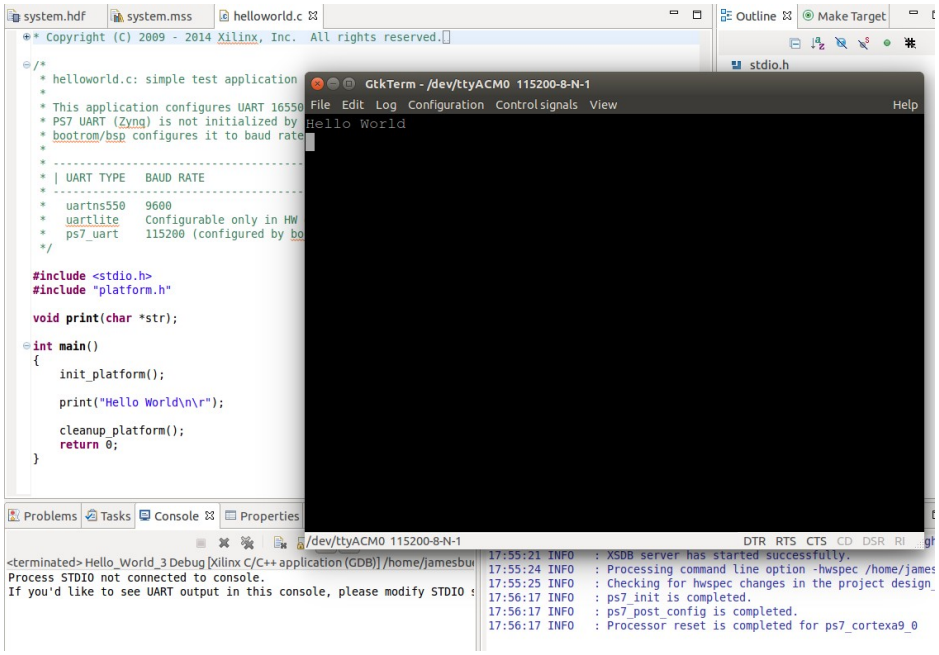


Vivado & SDK Procedure

1) Create Vivado project
2) Develop block design with IP cores
3) Modify connections/settings and validate design
4) Generate an HDL wrapper
5) Synthesis, implementation and bitstream generation
6) Program the ZedBoard hardware
7) Export to SDK and develop board support package
8) Develop software application to execute on the board

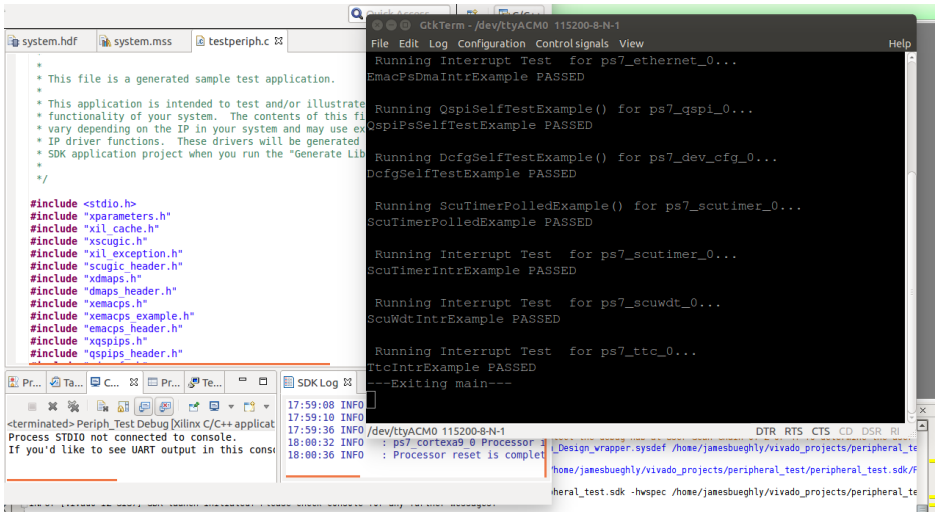
Hello World

- Jumper pins in cascaded JTAG mode
- Basic hardware design in Vivado including only PS
- Write helloworld.c in SDK and run on ZedBoard
- Output displayed in GTKterm window

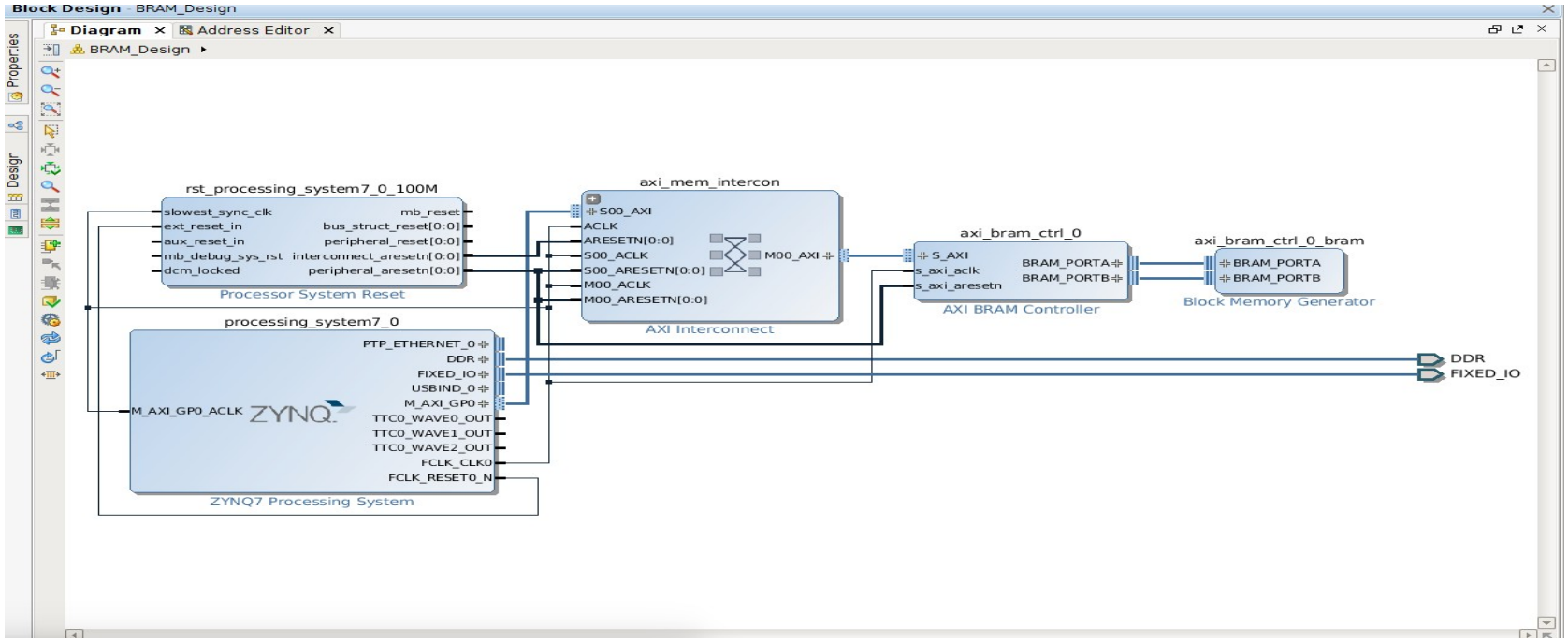


Memory and Peripherals

- Hardware design utilizes only PS
- Use SDK templates to test memory and peripherals
- Relevant information displayed in GTKterm window



Data Transfer Tests



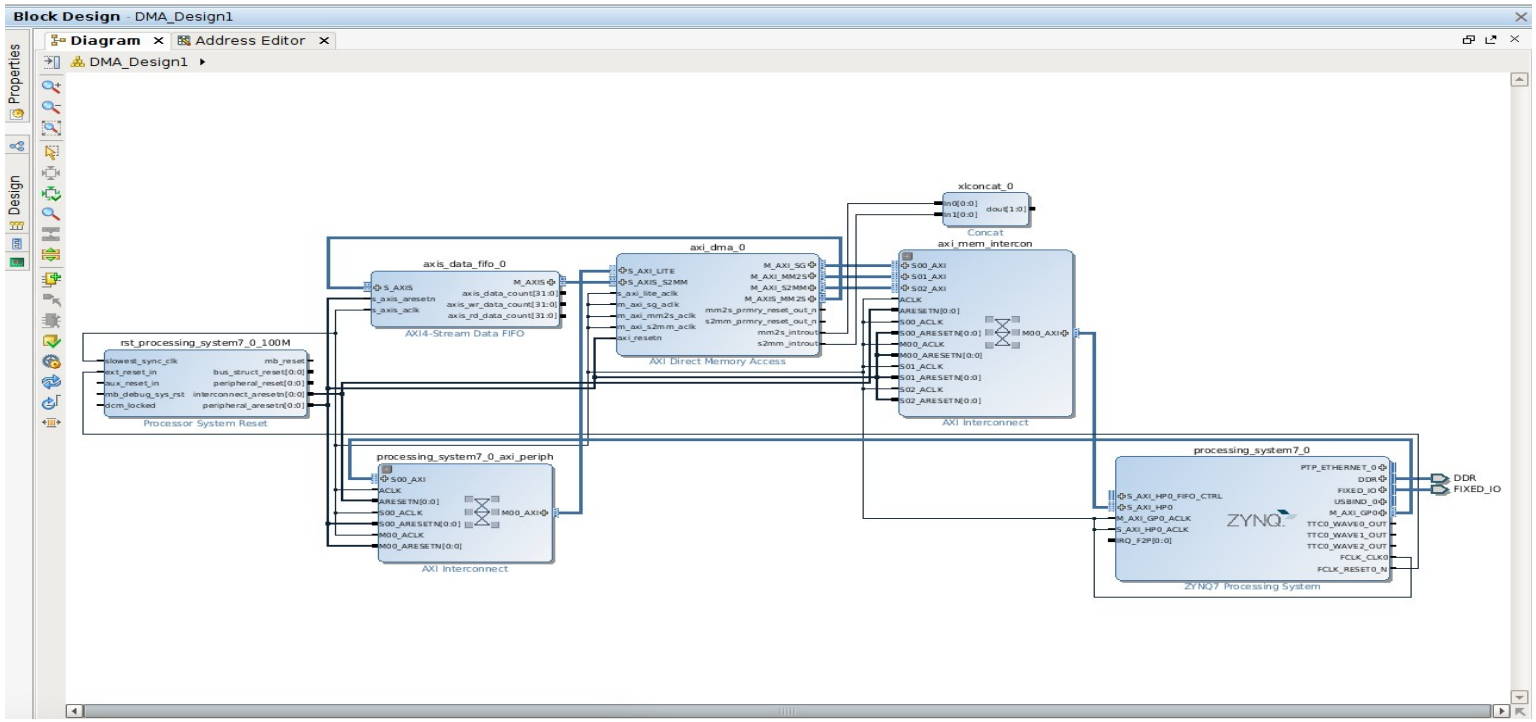
- Add BRAM, BRAM controller, and AXI-interconnect in Vivado block design
- Execute C script to test transfers between memory locations
  - BRAM → BRAM
  - BRAM → DDR3
  - DDR3 → DDR3

Transfer Test Results

Bytes transferred	BRAM/BRAM	BRAM/DDR3	DDR3/DDR3
256	18	10	2
512	20	11	2
1024	20	11	2
2048	21	11	2
4096	21	11	3
8192	21	11	3

Table 1: **Gain in data transfer rate** (ratio of clock cycles elapsed without DMA/clock cycles elapsed with DMA). This table compares data transfer rates with and without the use of a DMA Controller, varying the number of bytes transferred as well as the source and destination pairs (specified by the notation "source/destination"). We can observe that DMA is particularly advantageous for large data transfers involving PL components, such as the BRAM.

Data Transfer with FIFO

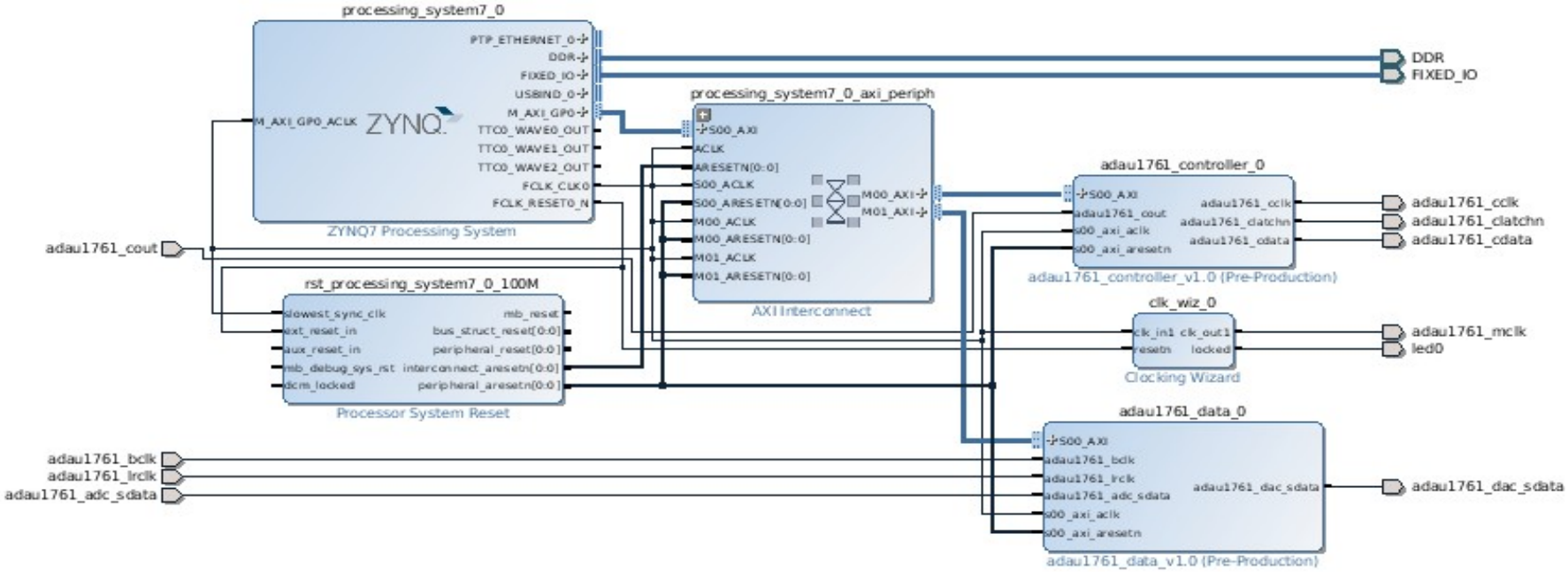


- Add FIFO loopback IP in PL
- Transfer: DDR3 → DDR3 using DMA

Data Transfer from Switch Register

- Input 8-bit data using switches on ZedBoard
- Include GPIO IP core in Vivado block design
  - Make connections external to access switches
- Transfer: Switches → BRAM → DDR3
  - Transfer both with and without DMA
- Read input data out in GTKterm window

Audio with ZedBoard



- Create custom IP: adau1761 controller and data
- Create and add to constraints file to assign external pins
- Audio in from computer → ZedBoard → audio out to headphones