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DAQ for Test beam plans

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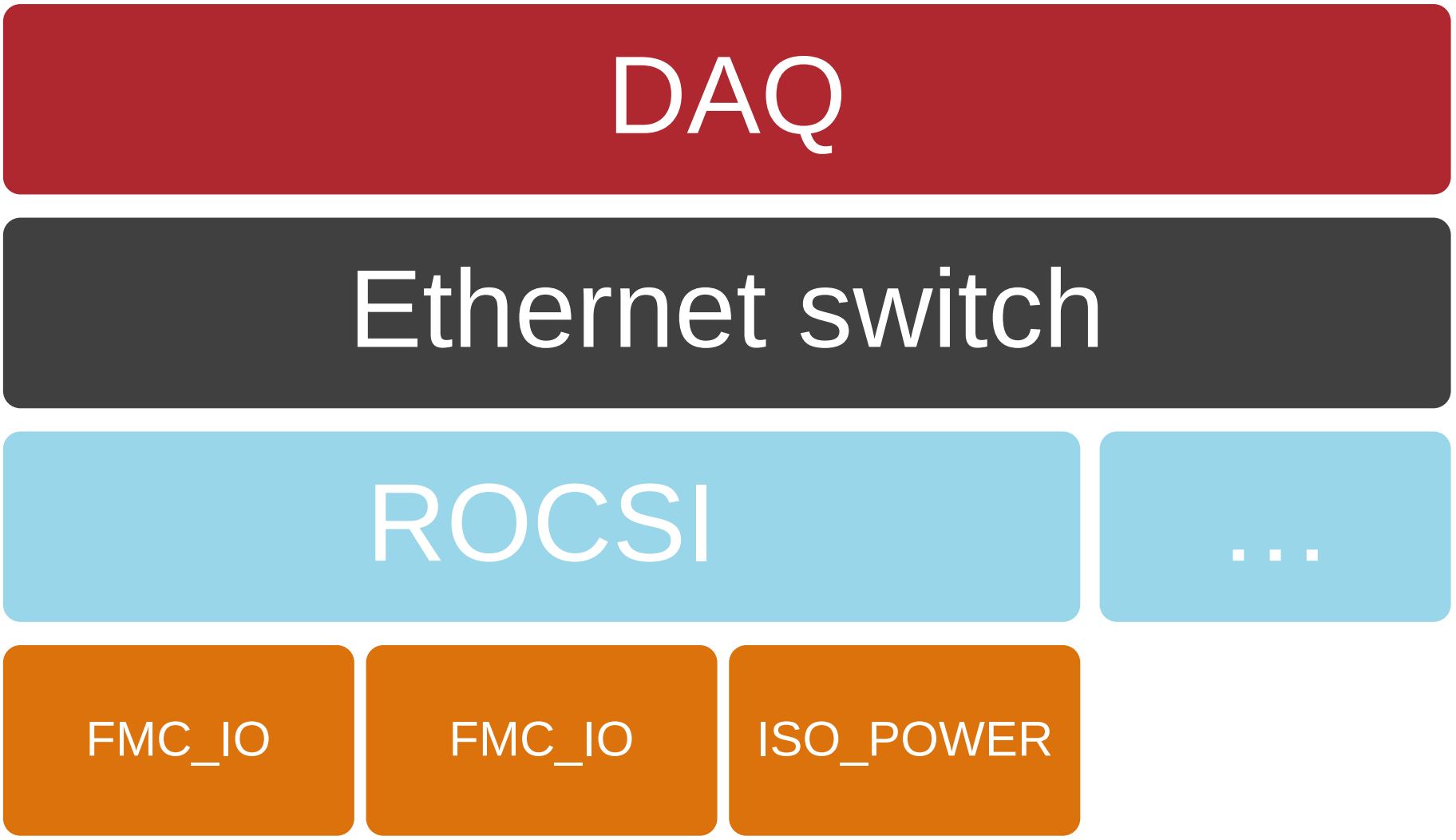
HGC Testbeam

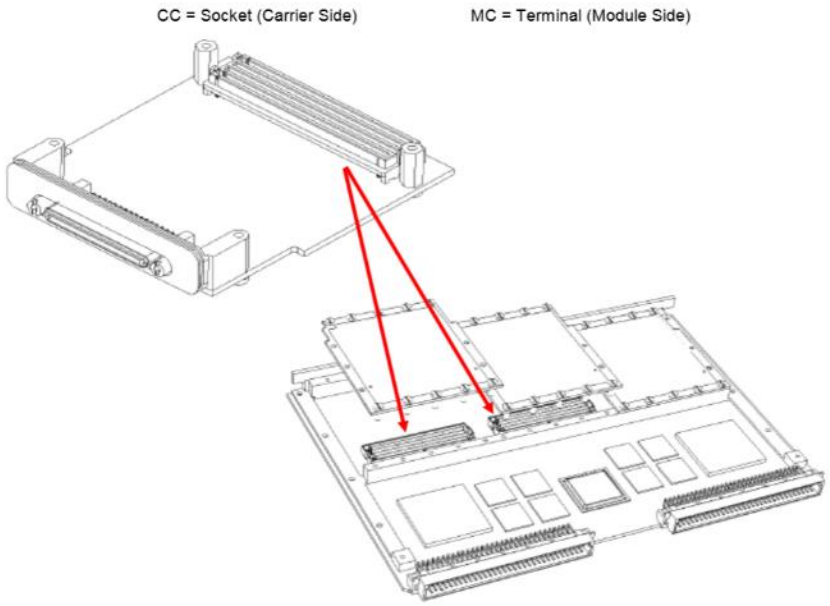
8 Oct 2015

Terminology Refresh



ROCSI

- Read Out Controller with SKIROC Interface
  - Carrier Card
  - Mechanically compatible with inexpensive VME crates (but not a VME card)
  1. Zynq (running Linux)
  2. Gig Ethernet
  3. SFP+ site
  4. Timing and trigger



Current status:

schematics in progress

ROCSI “stand in”

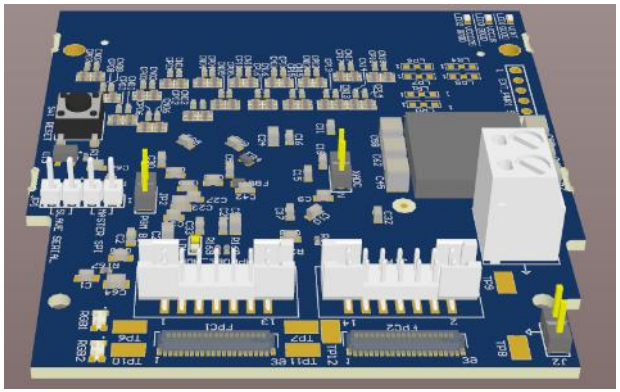
- Viable alternative(s) for ROCSI exist for **EARLY** stages of TB
  - Good: same Zynq, software, GBE, Interface to FMC_IO
  - OK: trigger can be kludged
  - BAD: no way to provide isolation

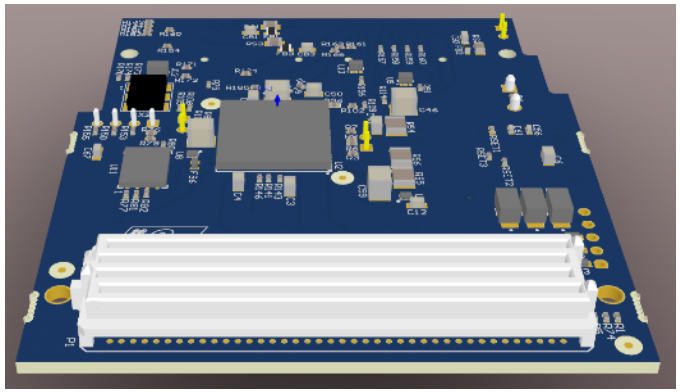
I think: ok for getting started, can be used for “couple” HGC modules

FMC_IO

Main interface to SKIROC

- Artix XC7A100T CSG324 (~6MB mem, 3.3V IO, no GTP)
- Can use isolated power supplied via FMC connector or externally supplied
- Designed to allow “kludged” clock/trigger
- If you had nothing else….





Current status:

all done, waiting for manufacturing

ISO Power

- Awaiting final review
  - Layout 100% done…. But I can't show it to you right now for technical reasons
    - this board is done in Mentor Expedition flow, not Altium like FMC_IO

Current status:

coming soon to screen near you!

Other stuff… Simulator board

- Debugging the SKIROC interface is key
- Optimizing SKIROC analog performance is key
  - Help this along by making a board that
    - Utilizes existing packaged SKIROCs
    - Simulates sensors
      - "what happens if the pixel capacitance is increased by x?"

This is a small board design to "simulate the sensor"

Key features:

daisy chain for SKIROC readout connectors

two SKIROC on board- can test differences of decoupling, etc

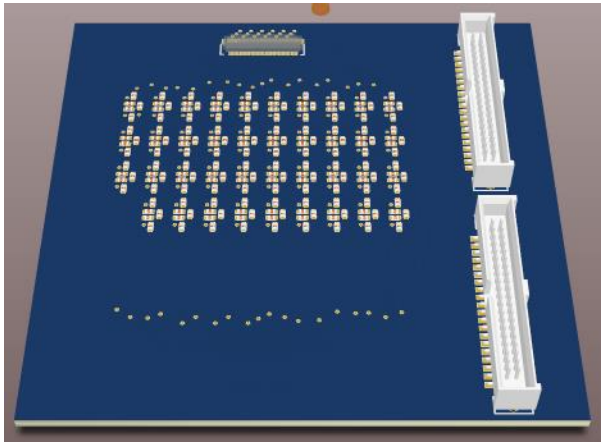
simulated inputs (multiplexed)

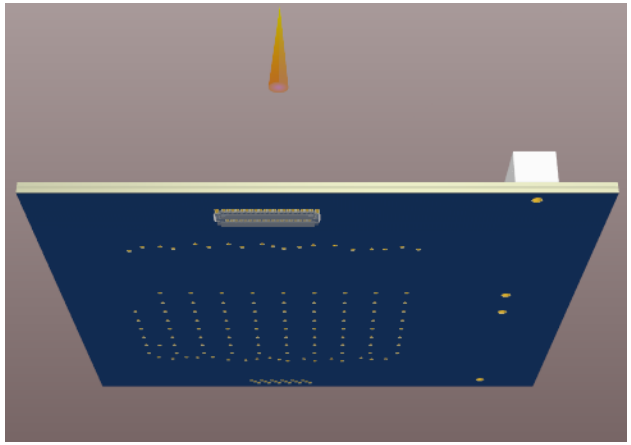
Current status:

Going into layout any day….

Other stuff… Breakout board

- Debugging the SKIROC interface is key
- Optimizing SKIROC analog performance is key
  - Help this along by making a board that
    - Breaks out the lines on the flex cable
    - Allows addition of filters, terminators, pull ups, pull downs
    - Allows fixing interface errors (what?!)





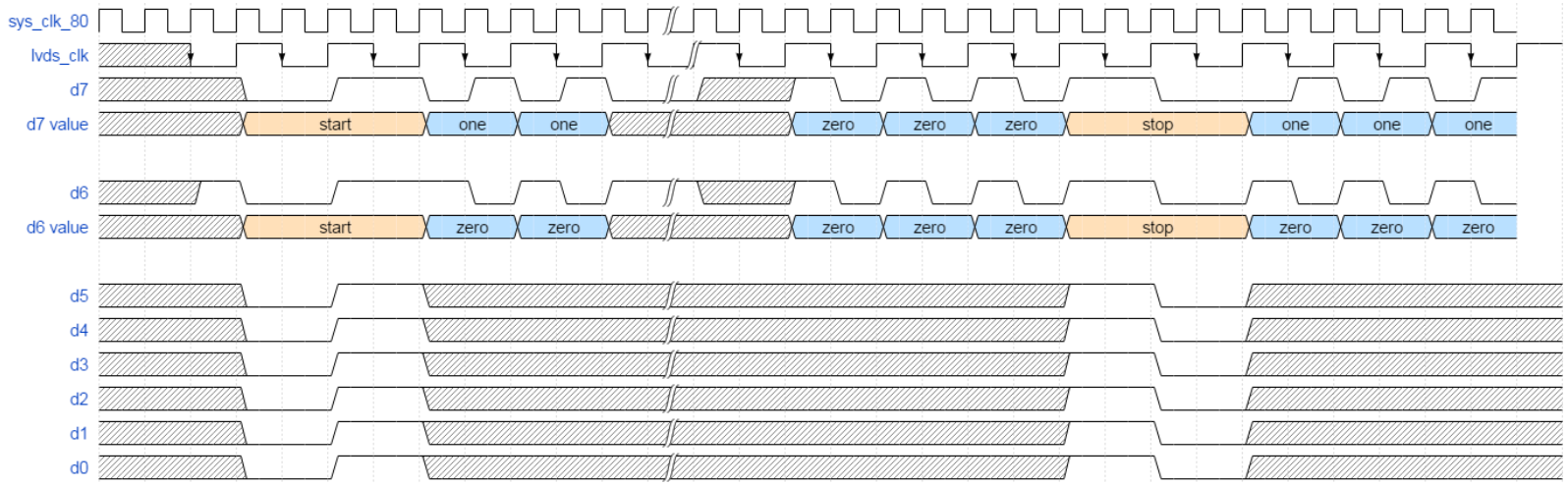
Current status:

Just about ready to go

Next steps

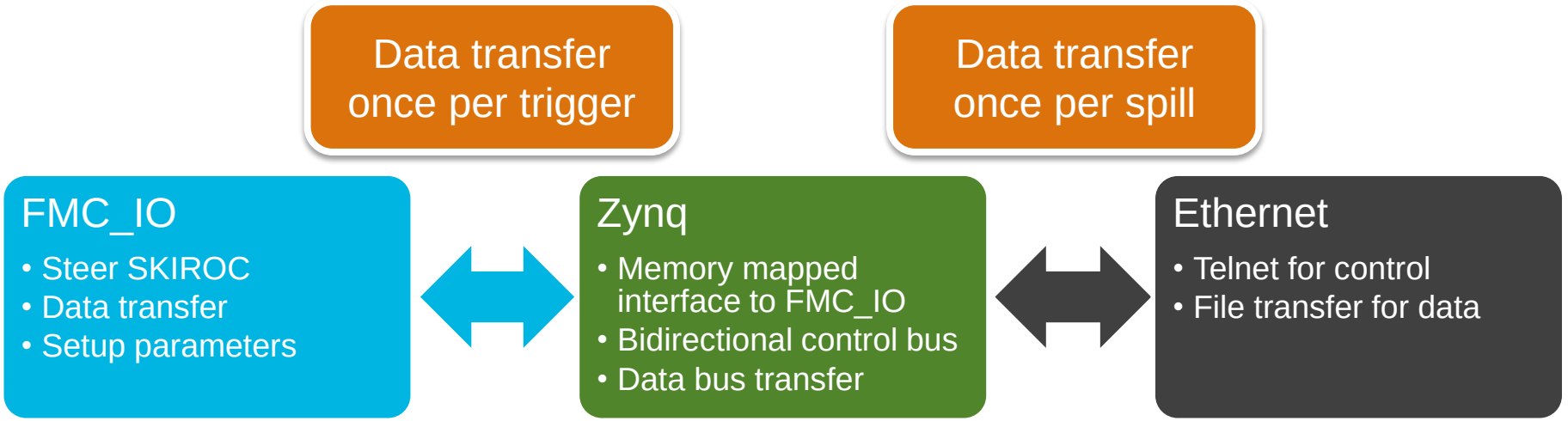
- Software & Firmware (& PCB design/debug)

- Define transfer protocol Zynq ←→ FMC_IO



IPbus simplified protocol subset… doc in preparation

Outline of data flow architecture



Summary

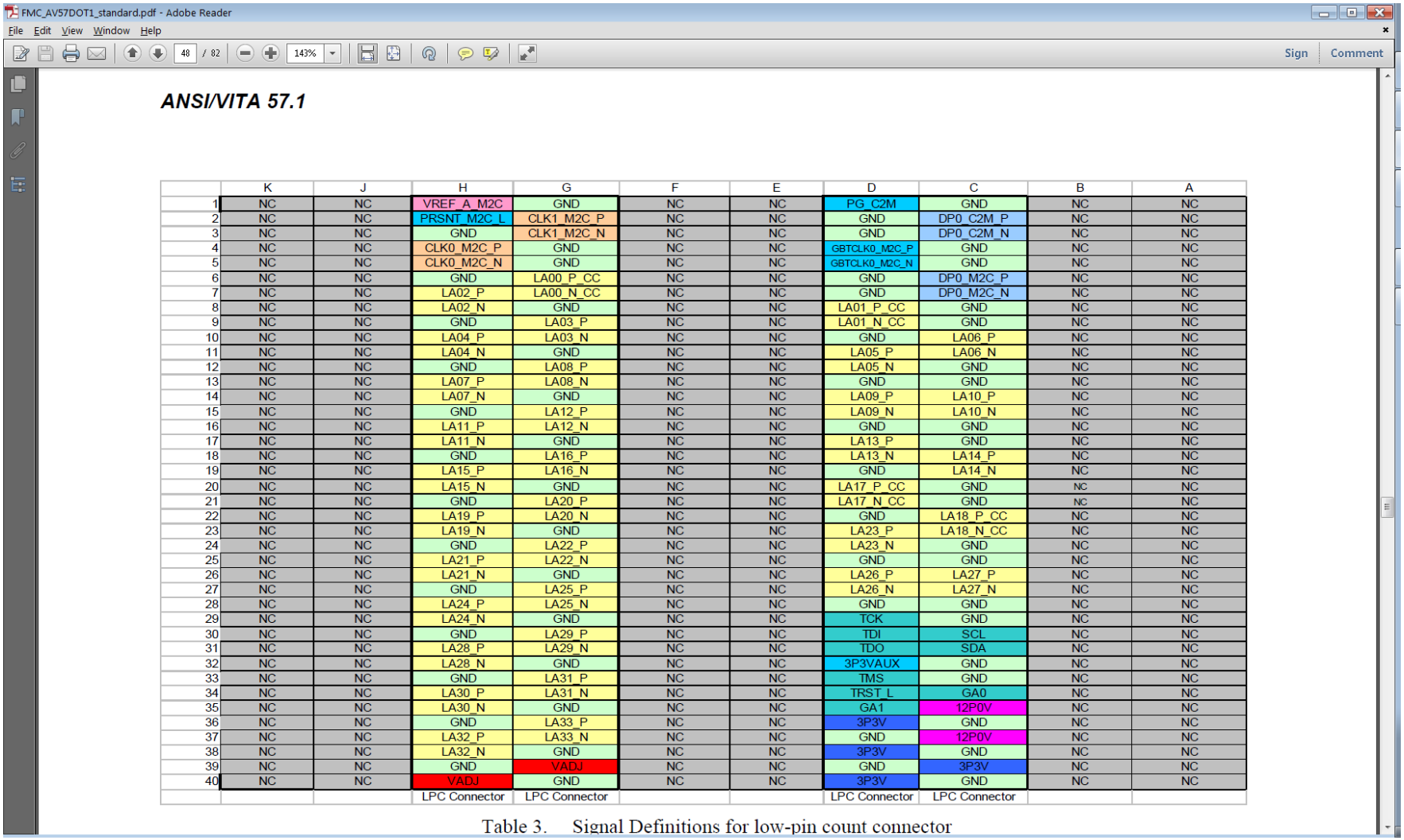
I think we have the start of a great team to work on DAQ

- Fermilab (Zoltan Gecse, Paul Rubinov, Cristian Gingu)
- Northwestern (Jia Fu Low, James Buehly)
- Univ of Mn (Erich Frahm)

- Things I think:
  - Will need to divide and conquer (define clear interfaces and responsibility)
  - Don’t forget beam instrumentation (wire chambers, other?)
  - Many new things, be realistic about debug/revisions

BACKUPS

Backup


FMC_AV57DOT1_standard.pdf - Adobe Reader

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48 / 82 143% Sign Comment

ANSI/VITA 57.1

	K	J	H	G	F	E	D	C	B	A
1	NC	NC	VREF_A_M2C	GND	NC	NC	PG_C2M	GND	NC	NC
2	NC	NC	PRSNT_M2C_L	CLK1_M2C_P	NC	NC	GND	DP0_C2M_P	NC	NC
3	NC	NC	GND	CLK1_M2C_N	NC	NC	GND	DP0_C2M_N	NC	NC
4	NC	NC	CLK0_M2C_P	GND	NC	NC	GBTCLK0_M2C_P	GND	NC	NC
5	NC	NC	CLK0_M2C_N	GND	NC	NC	GBTCLK0_M2C_N	GND	NC	NC
6	NC	NC	GND	LA00_P_CC	NC	NC	GND	DP0_M2C_P	NC	NC
7	NC	NC	LA02_P	LA00_N_CC	NC	NC	GND	DP0_M2C_N	NC	NC
8	NC	NC	LA02_N	GND	NC	NC	LA01_P_CC	GND	NC	NC
9	NC	NC	GND	LA03_P	NC	NC	LA01_N_CC	GND	NC	NC
10	NC	NC	LA04_P	LA03_N	NC	NC	GND	LA06_P	NC	NC
11	NC	NC	LA04_N	GND	NC	NC	LA05_P	LA06_N	NC	NC
12	NC	NC	GND	LA08_P	NC	NC	LA05_N	GND	NC	NC
13	NC	NC	LA07_P	LA08_N	NC	NC	GND	GND	NC	NC
14	NC	NC	LA07_N	GND	NC	NC	LA09_P	LA10_P	NC	NC
15	NC	NC	GND	LA12_P	NC	NC	LA09_N	LA10_N	NC	NC
16	NC	NC	LA11_P	LA12_N	NC	NC	GND	GND	NC	NC
17	NC	NC	LA11_N	GND	NC	NC	LA13_P	GND	NC	NC
18	NC	NC	GND	LA16_P	NC	NC	LA13_N	LA14_P	NC	NC
19	NC	NC	LA15_P	LA16_N	NC	NC	GND	LA14_N	NC	NC
20	NC	NC	LA15_N	GND	NC	NC	LA17_P_CC	GND	NC	NC
21	NC	NC	GND	LA20_P	NC	NC	LA17_N_CC	GND	NC	NC
22	NC	NC	LA19_P	LA20_N	NC	NC	GND	LA18_P_CC	NC	NC
23	NC	NC	LA19_N	GND	NC	NC	LA23_P	LA18_N_CC	NC	NC
24	NC	NC	GND	LA22_P	NC	NC	LA23_N	GND	NC	NC
25	NC	NC	LA21_P	LA22_N	NC	NC	GND	GND	NC	NC
26	NC	NC	LA21_N	GND	NC	NC	LA26_P	LA27_P	NC	NC
27	NC	NC	GND	LA25_P	NC	NC	LA26_N	LA27_N	NC	NC
28	NC	NC	LA24_P	LA25_N	NC	NC	GND	GND	NC	NC
29	NC	NC	LA24_N	GND	NC	NC	TCK	GND	NC	NC
30	NC	NC	GND	LA29_P	NC	NC	TDI	SCL	NC	NC
31	NC	NC	LA28_P	LA29_N	NC	NC	TDO	SDA	NC	NC
32	NC	NC	LA28_N	GND	NC	NC	3P3VAUX	GND	NC	NC
33	NC	NC	GND	LA31_P	NC	NC	TMS	GND	NC	NC
34	NC	NC	LA30_P	LA31_N	NC	NC	TRST_L	GA0	NC	NC
35	NC	NC	LA30_N	GND	NC	NC	GA1	12P0V	NC	NC
36	NC	NC	GND	LA33_P	NC	NC	3P3V	GND	NC	NC
37	NC	NC	LA32_P	LA33_N	NC	NC	GND	12P0V	NC	NC
38	NC	NC	LA32_N	GND	NC	NC	3P3V	GND	NC	NC
39	NC	NC	GND	VADJ	NC	NC	GND	3P3V	NC	NC
40	NC	NC	VADJ	GND	NC	NC	3P3V	GND	NC	NC
			LPC Connector	LPC Connector			LPC Connector	LPC Connector		

Table 3. Signal Definitions for low-pin count connector

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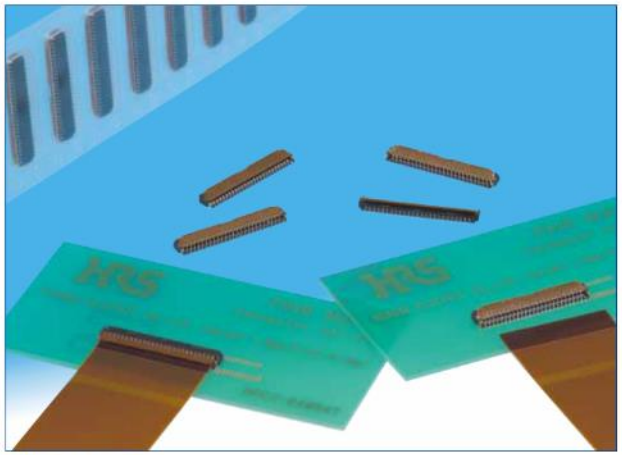
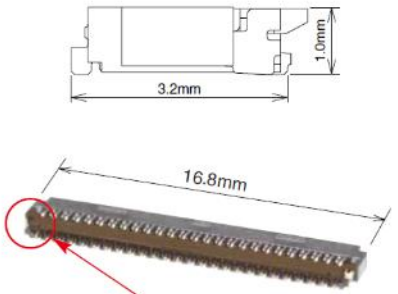
FPC

0.3 mm Pitch, 1.0 mm Height FPC Connector

FH26 Series



●Space saving(51 pos. shown)



■Features

1. Low-profile 0.3 mm pitch FPC connector

Ultra-thin design, 1.0 mm height, 3.2 mm width all add up to a compact, space saving form factor.

∗30% reduction in PCB footprint

∗40% reduction in weight

(Compared to our 0.3 mm pitch FH23 Series 51 position connector.)

2. Easy PCB Mounting

●Can be mounted over conductive traces.

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Might look a little like this