CSE530: Assignment#2 Report

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Introduction

In this report, we will be discussing and highlighting the results of ablation studies to understand the effect of changing cache parameters (cache size, associativity) on *Area* of data array, Total dynamic read *Energy* of data array and *Access time* of a cache. We will be using Cacti tool [1] to generate the values for each configuration change. Kindly refer to this GitHub project (https://github.com/ajaynarayanan/cse_530) for python jupyter notebook for automation code and generation of graphs. For glossary/detailed explanation of terms, please refer to [2].

Experiments and Discussions

1. Impact on Cache area

In this study, we vary cache size and associativity to understand the effect on the data array area of the cache.

a. Cache size

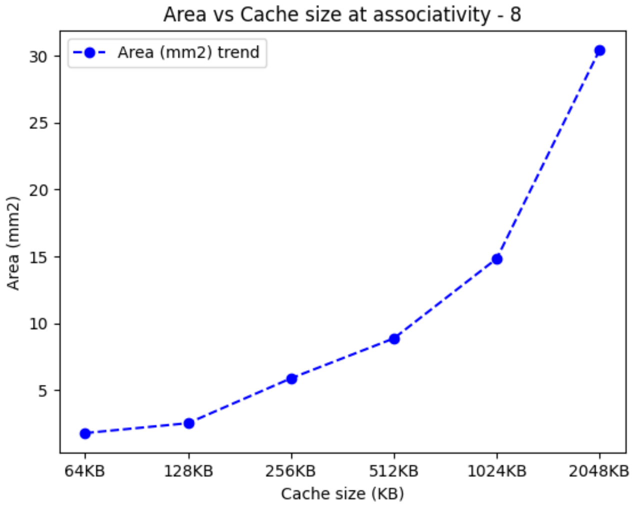

Fig. 1a: Effect of cache size on area of cache at constant associativity value of 8

In this experiment, we vary cache size from 64KB to 2MB in powers of 2 at a constant associativity value of 8 and observe the effect on the area (mm2) of the cache. From Fig 1a, we observe that the area (mm2) increases with increasing cache size. Recall that area = width of the data array * height of the data array. Increasing cache size will increase width and height to accommodate the extra bytes in SRAM of the cache. Also, there will be an increase in the area due to wiring costs. The results from the above graph align with the above statements.

b. Associativity

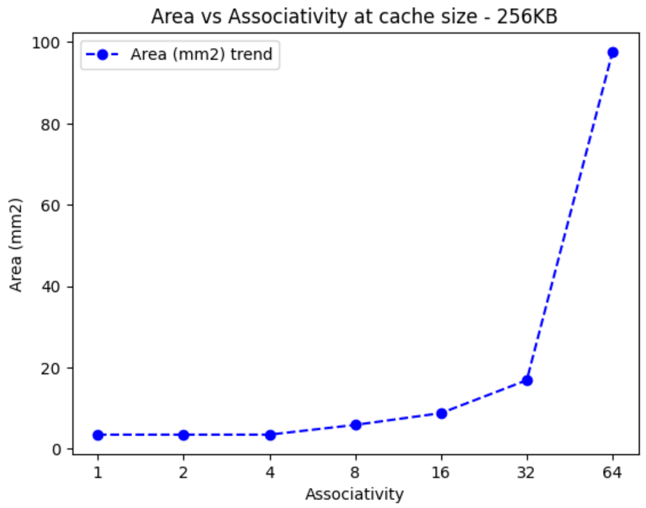

Fig. 1b: Effect of associativity on area of cache at constant cache size of 256KB

In this experiment, we vary associativity from 1 to 64 in powers of 2 at constant cache size of 256KB and observe the effect on the data array *area* of the cache. From Fig 2b, we observe that the *area* (mm2) increases significantly with increasing associativity size after associativity value of 16. We believe that this is due to the increased wires/lines and area cost of implementing tag comparator (more bits to compare). We theorize that after a point the area cost of tag comparator increases significantly which results in huge jump in area.

2. Impact on Cache Energy consumption

In this study, we vary cache size and associativity to understand the effect on the total dynamic read energy consumption of the data array of the cache.

a. Cache size

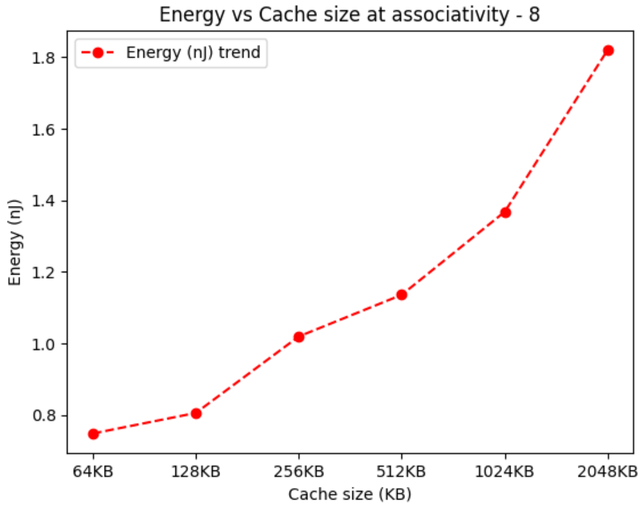

Fig. 2a: Effect of cache size on total dynamic read energy of data array of cache at constant associativity of 8

In this experiment, we vary cache size from 64KB to 2MB in powers of 2 at constant associativity of 8 and observe the effect on the total dynamic read energy of the data array. From Fig 2a, we observe that the energy (nJ) increases with increasing cache size. Recall dynamic energy is directly proportional to capacitance of the line ($C_L V^2 P_{0->1}$) and probability of transitioning from 0 to 1 [2]. We justify the above graph observation by the fact that increasing cache size increases the energy consumed to drive each transistor (increases all components in the energy equation).

b. Associativity

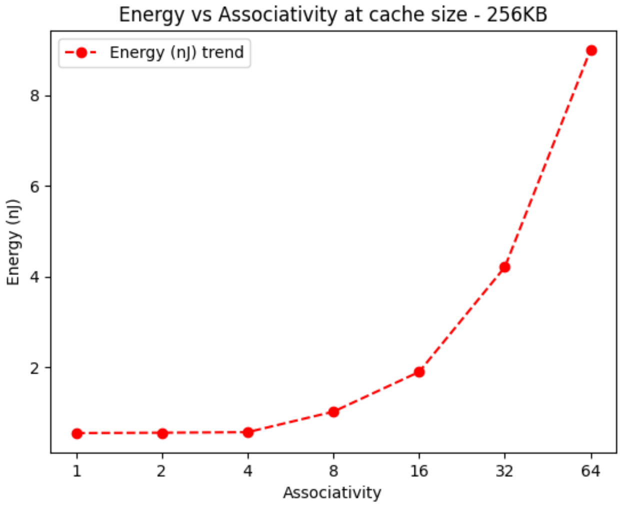

Fig. 2b: Effect of associativity on total dynamic read energy of data array of cache at constant cache size of 256KB

In this experiment, we vary associativity from 1 to 64 in powers of 2 at constant cache size of 256KB and observe the effect on the total dynamic read *e*nergy of the cache. From Fig 2b, we observe that the *energy* (nJ) increases significantly with increasing associativity size after associativity value of 16. Recall dynamic energy is directly proportional to capacitance of the line ($C_L V^2 P_{0->1}$) and probability of transitioning from 0 to 1 [2]. We believe that the above trend is due to the increased wires/lines which result in increased capacitance. Additionally, the tag comparator will increase the circuit depth and $P_{0->1}$ and thereby increasing energy consumption.

3. Impact on Access time

a. Cache size

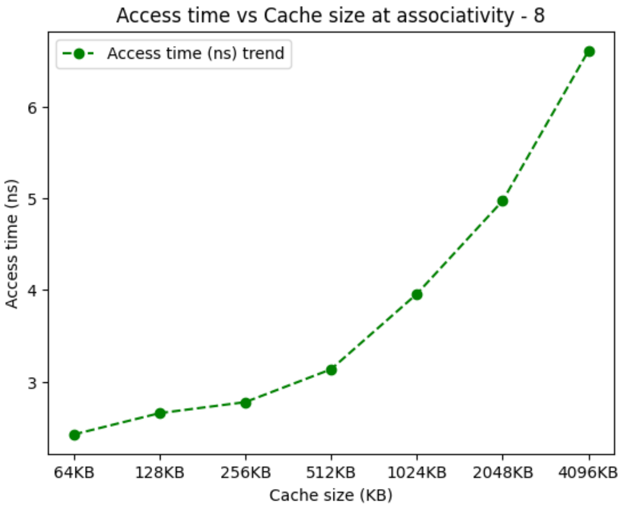

Fig. 3a: Effect of cache size on access time of cache at constant associativity of 8

In this experiment, we vary cache size from 64KB to 4MB in powers of 2 at constant associativity of 8 and observe the effect on the *access time* of the cache*.* From Fig 3a, we observe that the access (ns) time increases with increasing cache size. Note that the data array access time increases due to long wires in the cache circuit to accommodate the extra bytes in SRAM.

b. Associativity

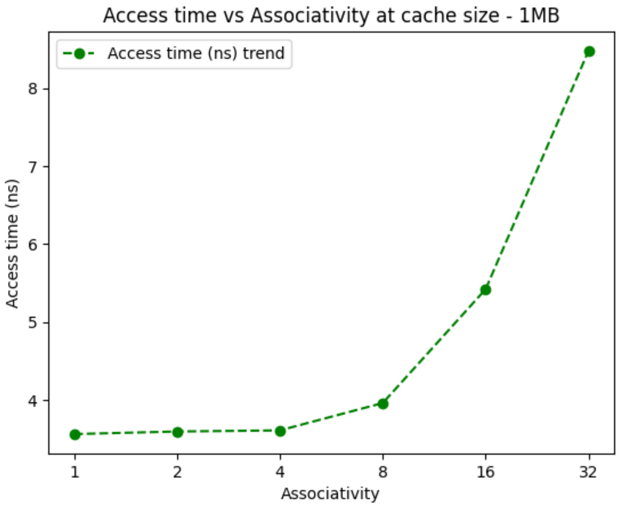

Fig. 3b: Effect of associativity on access time of cache at constant cache size of 1MB

In this experiment, we vary associativity from 1 to 32 in powers of 2 at a constant cache size of 1MB and observe the effect on the access time of the cache. From Fig 2b, we observe that the access time (ns) increases with increasing associativity size. We recall associativity reduces cache conflict compared to direct mapped cache [2]. Hence, there is no significant impact on access time for small associativity values. However, due to the circuit complexity (more bits to compare in tag, more lines) of implementing higher order set associative cache, the access time increases after associativity of 8.

Conclusions

Based on the discussion and graphs, we understand that increasing cache size and associativity of the cache increases the Area of the data array, Total dynamic read Energy of the data array and Access time of a cache on average.

- Increasing cache size: We reason that the increased data array area results from the increase in breath and width of the cache. Further, the rise in energy is due to the higher bytes to read to drive the circuit and the higher capacitance of the wires. Finally, the access time increases due to the increased width and height of the cache with larger cache sizes.
- Increasing associativity: The increased area is because of the increase in wires and bit to compare in tag component of the cache. Additionally, the rise in energy is due to the same reason mentioned in increasing the cache size subsection. Finally, the access time increases due to the circuit depth and complexity of implementing set associativity.

References

[1.] Balasubramonian, Rajeev, et al. "CACTI 7: New tools for interconnect exploration in innovative off-chip memories." ACM Transactions on Architecture and Code Optimization (TACO) 14.2 (2017): 1-25.

[2] Vijaykrishnan Narayanan. “Lecture slides from Fall 2022 CSE530: Computer Architecture course at PSU”