CSE530: Assignment#3 Milestone Report

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Introduction

In this milestone report, we will be simulating the quicksort benchmark from Stanford LLVM[1] with the following parameters (cpu-type= DerivO3CPU, l2cache enabled, cpu-clock="1GHz", memtype=DDR3_2133_8x8) on gem5[2] to make sure our setup is working as expected. We will capture key statistics from the run, such as execution time, CPU ops distribution, cache accesses/miss rates and memory accesses.

Results

Here, we show a few key statistics from the output of the gem5 simulation on the quicksort benchmark.

Metric Name	parameter	Value
Simulation execution time	simSeconds	0.190031
#(instructions simulated)	simInsts	169069275
#(CPU ALU instructions committed)	system.cpu.commit.committedInstType_0::IntAlu	157399295
#(CPU Int Mult instructions committed)	system.cpu.commit.committedInstType_0::IntMult	1500500
#(CPU Int Div instructions committed)	system.cpu.commit.committedInstType_0::IntDiv	734
#(MemRead instructions committed)	system.cpu.commit.committedInstType_0::MemRead	79725811
#(MemWrite instructions committed)	system.cpu.commit.committedInstType_0::MemWrite	19325867
Instruction Cache (L1) misses	system.cpu.icache.overallMisses::total	483
Instruction Cache (L1) total accesses	system.cpu.icache.overallAccesses::total	43599098
Instruction Cache (L1) miss rate	system.cpu.icache.overallMissRate::total	0.000011
Data Cache (L1) misses	system.cpu.dcache.overallMisses::total	406
Data Cache (L1) total accesses	system.cpu.dcache.overallAccesses::total	109751022
Data Cache (L1) miss rate	system.cpu.dcache.overallMissRate::total	0.000004
L2 cache misses	system.l2.overallMisses::total	480
L2 total accesses	system.l2.overallAccesses::total	791
L2 cache miss rate	system.l2.overallMissRate::total	0.606827
#(bytes read from memory)	system.mem_ctrls.dram.bytesRead::total	30720
#(reads from memory)	system.mem_ctrls.dram.numReads::total	480

Note: since the quicksort benchmark is based on integer arrays, most CPU ops are ALU/mem operations.

References

[1.] https://github.com/llvm/llvm-test-suite/blob/main/SingleSource/Benchmarks/Stanford

[2.] https://www.gem5.org/documentation/