

Toward Printed Integrated Circuits based on Unipolar or Ambipolar Polymer Semiconductors

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For at least the past ten years printed electronics has promised to revolutionize our daily life by making cost-effective electronic circuits and sensors available through mass production techniques, for their ubiquitous applications in wearable components, rollable and conformable devices, and point-of-care applications. While passive components, such as conductors, resistors and capacitors, had already been fabricated by printing techniques at industrial scale, printing processes have been struggling to meet the requirements for mass-produced electronics and optoelectronics applications despite their great potential. In the case of logic integrated circuits (ICs), which constitute the focus of this Progress Report, the main limitations have been represented by the need of suitable functional inks, mainly high-mobility printable semiconductors and low sintering temperature conducting inks, and evolved printing tools capable of higher resolution, registration and uniformity than needed in the conventional graphic arts printing sector.

Solution-processable polymeric semiconductors are the best candidates to fulfill the requirements for printed logic ICs on flexible substrates, due to their superior processability, ease of tuning of their rheology parameters, and mechanical properties. One of the strongest limitations has been mainly represented by the low charge carrier mobility (μ) achievable with polymeric, organic field-effect transistors (OFETs). However, recently unprecedented values of $\mu \sim 10 \text{ cm}^2/\text{Vs}$ have been achieved with solution-processed polymer based OFETs, a value competing with mobilities reported in organic single-crystals and exceeding the performances enabled by amorphous silicon (a-Si). Interestingly these values were achieved thanks to the design and synthesis of donor-acceptor copolymers, showing limited degree of order when processed in thin films and therefore fostering further studies on the reason leading to such improved charge transport properties. Among this class of materials, various polymers can show well balanced electrons and holes mobility, therefore being indicated as ambipolar semiconductors, good environmental stability, and a small band-gap, which simplifies the tuning of charge injection. This opened up the possibility of taking advantage of the superior performances offered by complementary "CMOS-like" logic for the design of digital ICs, easing the scaling down of critical geometrical features, and achieving higher complexity from robust single gates (e.g., inverters) and test circuits (e.g., ring oscillators) to more complete circuits.

Here, we review the recent progress in the development of printed ICs based on polymeric semiconductors suitable for large-volume micro- and nano-electronics applications. Particular attention is paid to the strategies proposed in the literature to design and synthesize high mobility polymers and to develop suitable printing tools and techniques to allow for improved patterning capability required for the down-scaling of devices in order to achieve the operation frequencies needed for applications, such as flexible radio-frequency identification (RFID) tags, near-field communication (NFC) devices, ambient electronics, and portable flexible displays.

1. Introduction

In 1958, the first integrated circuit (IC) was developed by Jack Kilby at Texas Instruments, and this fuelled tremendous growth in silicon (Si)-based electronics.^[1] Advances in the IC technology have made ICs more powerful in terms of computational capabilities, faster, smaller, and less expensive in each generation. Now electronics, from personal computers to smart phones, govern our daily lives and it is expected that this trend toward ubiquitous electronics will continue. For such future applications, electronics should be cost-effective, environmentally friendly, disposable/recyclable, light-weight, unbreakable, and easy to carry: printed and flexible (or stretchable) devices can satisfy these requirements. Flexible radio-frequency identification (RFID) tags, near-field communication (NFC) devices, ambient electronics, and portable flexible displays are some examples of such ubiquitous electronic applications that can be realized within the near future.^[2] Recently, a few pioneering companies have successfully demonstrated the first example of these flexible RFID tags and active matrix flexible displays.^[3–6]

From a manufacturing perspective, the biggest difference between flexible and conventional rigid electronics is the handling of non-self-standing substrates such as plastics, thin metal foils, and ultrathin glass during the manufacturing processes.^[7] These flexible substrates cannot perfectly retain their shape during processing, which is one main reason for the relatively low production yield. To

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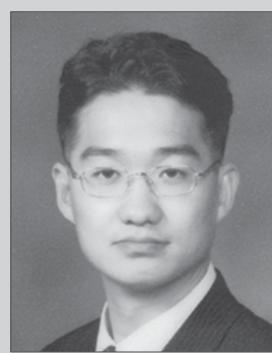


DOI: 10.1002/adma.201205361

overcome this problem, lamination of the flexible substrate on a rigid carrier, such as a glass or silicon wafer, is commonly adopted to provide self-standing properties to the flexible substrate.^[8] After the overall manufacturing process, the flexible devices are subsequently delaminated from the rigid substrate using various methods, such as laser irradiation.^[7] Electronics on Plastic by Laser Release (EPLaR), which was invented by Philips, is one typical example of a method utilizing laminating-delaminating techniques to manufacture flexible e-paper or organic light-emitting diodes (OLEDs) displays.^[9] However, the method can raise the costs and increase process defectivity, mainly due to the critical laminating-delaminating step.^[10] Roll-to-roll (R2R) manufacturing, where a suitable mechanical tension applied on the continuous flexible substrate replaces the need for a carrier, is instead considered to be the ideal method for producing flexible devices. Moreover, the R2R process can effectively reduce the manufacturing cost when it is combined with various graphic arts printing (GAP) methods for the deposition and patterning of functional films.

Printed electronics is an emerging industry in which conventional printing technologies are utilized to manufacture a variety of electronic devices with various form factors and applications, including devices with flexible and/or stretchable substrates.^[11] This industry has been enabled by the development of a wide range of functional materials, including metals, insulators, and semiconductors, that can be formulated into inks or pastes and that therefore lend themselves to be adopted for the realization of electrical components and devices by printing techniques. This industry mostly aims to achieve low-cost, large-area, and flexible electronics by eliminating some of the cost drivers in conventional Si-based electronics, such as the high-vacuum deposition equipment, subtractive processes, and photolithography. Although printed devices still show poorer performance than their vacuum-deposited or crystalline inorganic counterparts, they could provide good electronic functionalities in a completely new family of products including flexible displays, RFID tags, smart cards, disposable point-of-care applications, electronic labels, and memory.

During the early development of printed electronics, the printing technology was mainly used for manufacturing 'low-end' devices requiring larger printed feature sizes, such as printed antennas in Si-based RFID tags and various wiring patterns.^[12] However, as forecasted in a printed electronics technology roadmap produced by Nikkei Electronics in 2007, the technology is expected to progress to 'high-end' products requiring sophisticated alignment, complicated patterning, and extremely small feature sizes, such as those needed for high density printed memory and highly integrated printed microprocessors (see **Figure 1**). It should be noted that state-of-the-art microprocessors based on vacuum-deposited organic semiconductors^[13] now exhibit performance levels very similar to those of early-stage Si circuits, such as the Intel 4004, the first commercial microprocessor.^[14] Released by the Intel corporation in 1971 and manufactured using a ~10 µm scale photolithography process, Intel 4004 was a 4-bit central processing unit (CPU) consisting of ~2300 transistors and carrying out *p*-only operation at ~108 kHz.^[14] The first 8-bit organic microprocessor was instead reported in 2011: mainly based on a vacuum process, it was composed of ~4000 *p*-type pentacene transistors (average μ



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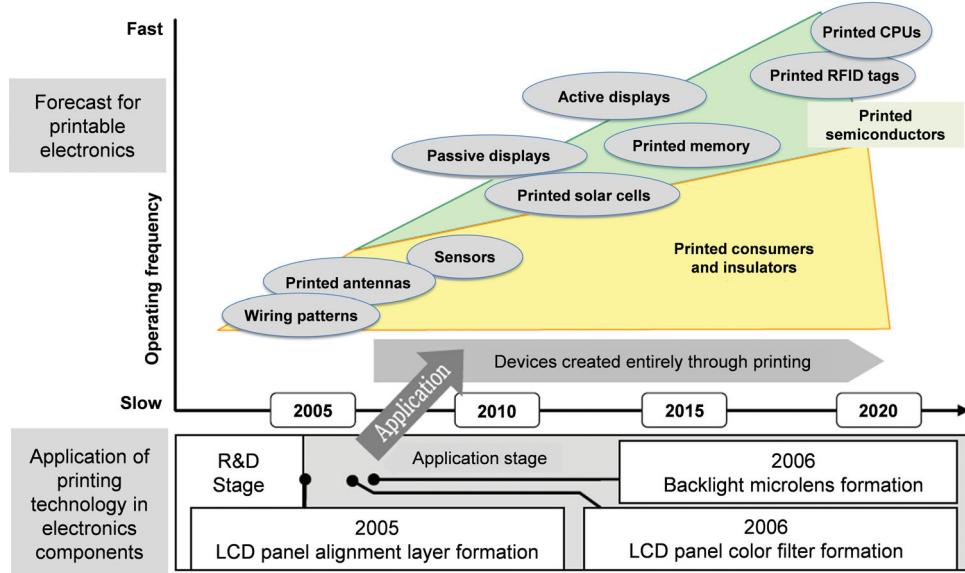


Figure 1. Printed electronics technology roadmap produced by Nikkei Electronics, March 2007. Reproduced with permission. Copyright 2007, Nikkei Electronics.

of $\sim 0.19 \text{ cm}^2/\text{Vs}$) fabricated on a flexible plastic foil and it could operate at 6 Hz thanks to dual-gate logic architecture.^[13] Despite this remarkable achievement, organic and printed electronics technology is still immature, because of its recent development mainly concentrated in the last two decades, and devices look crude compared to Si transistors. However, it is expected that printed electronic circuits will be significantly improved and will be used in real applications in the near future.

According to a technical report produced in 2011 by IDTechEx,^[15] the market for printed and thin film electronics, including organics, inorganics, and composites, will increase remarkably from US\$ 2.2 billion in 2011 to US\$ 46.94 billion in 2021 (see Figure 2a). There are already a number of applications of the printed and potentially printed electronics, such as conductive inks (for membrane keyboards, printed circuit boards, and flex connectors), sensors (e.g. disposable glucose sensors for diabetes), and OLEDs on glass substrates, which are not printed as yet. Although these more mature applications make a relevant market size in 2011, only 37% employ predominantly printing. However, these products will be rapidly overtaken in terms of the market value as hundreds of companies are developing, for example, printed OLED displays on flexible substrates as well as printed thin-film transistor (TFT) backplanes. The evolution of these technologies has been relatively slow for many reasons, such as not enough opto/electronic performance, uniformity, reliability and stability issues; however, as mentioned before, their markets are expected to grow rapidly, with a projected US\$ 301 billion market in 2028.^[15] Importantly, printed logic and memory applications are also expected to be a major market share (US\$ 4.0 in 2021), as shown in Figure 2b.

The most significant advantage of printable organic and inorganic electronic materials is that it can be extremely inexpensive to form them into components and circuits. This is because only small quantities of these materials will be needed

per device (when direct printing methods are used), and they show potentiality for being directly printed onto low-grade packaging materials, thus strongly simplifying the integration of electronic functionalities into other products. This technology

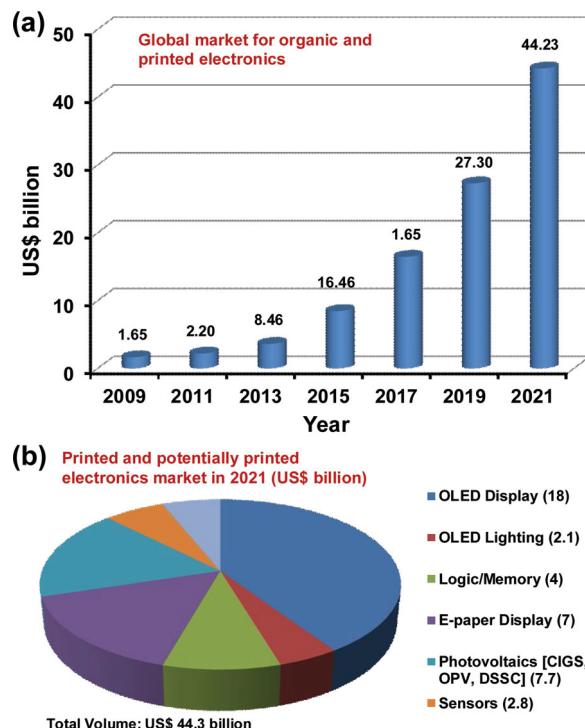


Figure 2. (a) Market forecast for organic and printed electronics (US\$ billion), and (b) split of printed and potentially printed electronics market in 2021 (US\$ billion) by component type. Reproduced with permission from Ref. [15].

also provides new paradigms for manufacturing truly new products, such as bendable, rollable, foldable, edible, stretchable, or biodegradable ones. In some cases, there is room also for improved performances with respect to present technologies on the market, e.g. the power conversion efficiency (η) of polymer solar cells ($\eta \sim 9.2$ to 11%),^[16] which however are not fully printed yet, is approaching the one achievable with cells based on a-Si:H ($\eta \sim 12.5\%$).^[17] These technologies will thus create completely new industrial markets, which are already present in some areas, such as smart packaging, architectural features, skin patches, and new toys. It is obvious that printed electronics technology may be a leading market driver within ten years.

In this progress report, we present a broad overview of recent advances in and perspectives for printed organic electronic devices and circuits, mainly focusing on those based on polymer semiconductors. This report is organized into the following parts. Section 2 is an introduction to π -conjugated polymer semiconductors, where a variety of the best performing materials and their charge carrier mobilities in OFET devices are presented. Section 3 provides then a brief review of printing techniques, developed for graphical arts that can be adapted to the additive processing of polymer circuits. Section 4 introduces fundamentals of electronic circuits relevant for understanding the recent progress in the development of printed ICs based on organic semiconductors, which is the focus of this section. In Sections 5 and 6, we discuss the most promising strategies for realizing high-performance complementary and ambipolar ICs and we review recent progresses toward these approaches. Finally, concise summaries of and perspectives for printed electronics and ICs are presented in conclusions.

2. Polymer Semiconductors and Manufacturing Processes

2.1. π -Conjugated Polymer Semiconductors

Compared to small-molecule organic semiconductors, π -conjugated polymers generally have excellent large-area film uniformity with isotropic charge transport and low device-to-device performance variation, easy control of the rheological properties of the solutions (very important for printing processes), relatively easy multilayer stacking through the proper choice of orthogonal solvents for the underlying films, and very good mechanical properties. All these features make polymer semiconductors suitable for R2R printed and flexible electronics. As shown in **Figure 3**, polymer semiconductors for OFETs and ICs applications must have two essential structural features:^[18] (i) a π -conjugated backbone composed of linked, unsaturated units, that results in extended π -orbitals along the polymer chain^[19] and (ii) functionalization of the polymer core with solubilizing substituents, which enables solution processing through a variety of printing techniques and enhances the interactions between the polymer cores.^[19–21] Notably, the extent of the π -conjugation and the interactions between these units determine the electronic and optoelectronic properties of the polymers, such as their optical absorption/emission, redox

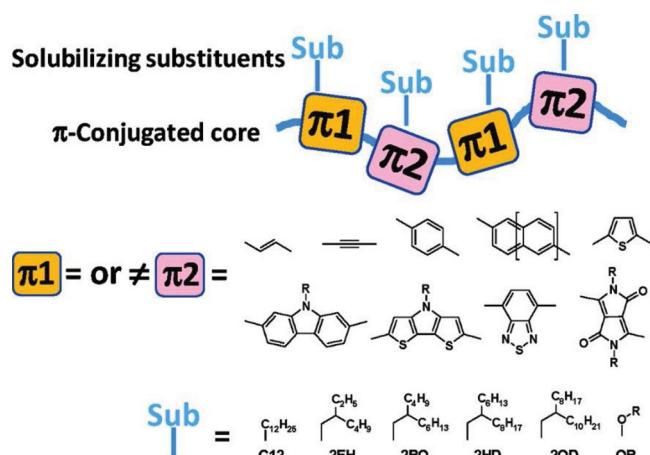


Figure 3. Schematic representation of a polymer chain with just a few examples of unsaturated (π) and solubilising (sub) units. Reproduced with permission from Ref. [19]. Copyright 2011, American Chemical Society.

characteristics, frontier molecular orbital energy levels (the highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO)), and transport of charge carriers.^[19] In addition, the parameters for polymeric materials in particular, such as the molecular weight and the polydispersity index (PDI), are also important and have to be controlled and designed to achieve proper solubility, ink formulation (rheological properties), thin-film formation, and morphology.^[19]

2.2. *p*-type Polymer Semiconductors

To date, a variety of *p*-type polymer semiconductors for use in OFETs and ICs have been reported. **Figure 4** presents the chemical structures of the state-of-the-art *p*-type polymer semiconductors and their corresponding charge carrier (hole) mobilities. Regioregular poly(3-hexylthiophene) (rr-P3HT) is a very well-known, representative material that has been widely studied, allowing to achieve a substantial understanding of general optical and electrical properties of π -conjugated polymer semiconductors as well as for their applications in opto-electronic devices, such as OFETs,^[20] organic photovoltaics (OPVs),^[22] and sensors.^[23,24] The presence of the 3-substituent alkyl-chain in the polythiophene core leads to good solubility and processability. The hole mobility of rr-P3HT OFETs typically ranges from 10^{-3} to $10^{-1} \text{ cm}^2/\text{Vs}$ and has been extensively investigated by various research groups considering the effects of molecular weight,^[25–27] control of regioregularity,^[28] film deposition solvents,^[29] thin-film morphology,^[30,31] film thickness,^[32] fabrication process,^[33] humidity,^[34] and core substituent (alkyl chain) length.^[35] These fundamental studies have contributed to the early development of relatively high-mobility polymer semiconductors by deepening our understanding of the charge transport mechanism and inspired the further development of π -conjugated polymer semiconductors with improved charge carriers mobility, in the range from 1 to $10 \text{ cm}^2/\text{Vs}$, excellent bias and good environmental stability.^[36,37]

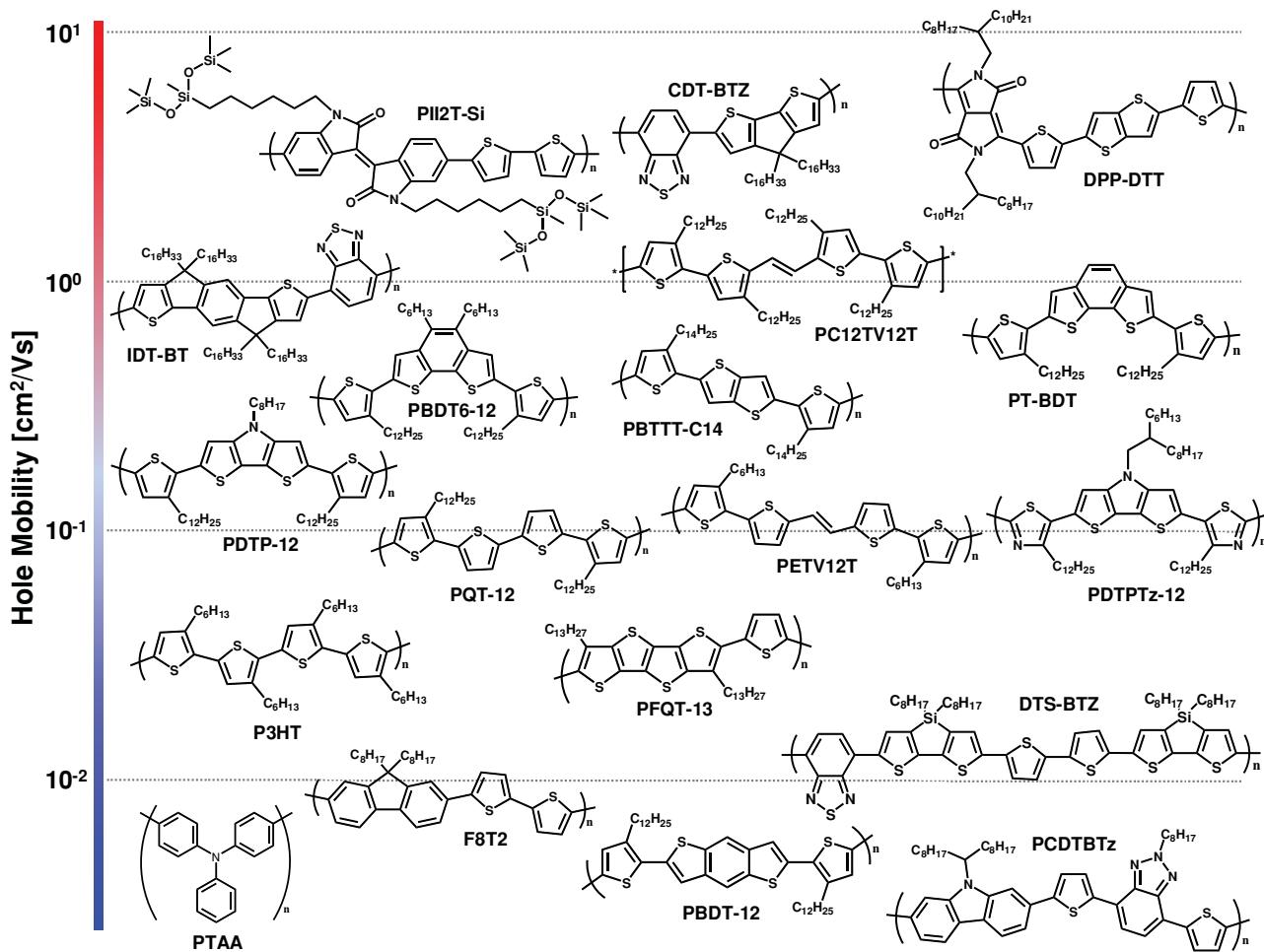


Figure 4. Chemical structures and corresponding charge carrier mobilities of representative *p*-type polymer semiconductors.

To address some of the problems of P3HT, such as its insufficient mobility and stability upon exposure to ambient air, new polythiophenes were developed by Ong et al. (regioregular poly-quaterthiophenes, PQTs)^[38] and McCulloch et al. (Poly[2,5-bis(3-tetradecylthiophen-2-yl)thieno[3,2-b]thiophene], PBTTT-C14),^[39] who increased the oxidative doping stability (i.e. increased the oxidation potential by slightly twisting the repeating units in the backbone) and enhanced the intermolecular ordering (i.e. induced molecular self-assembly and interdigitated long alkyl chains). The PQT- and PBTTT-based OFETs showed quite high saturation mobilities of ~0.14 cm²/Vs and 0.2–0.7 cm²/Vs, respectively.^[38,39] These results also triggered a number of studies aimed at understanding their morphological and optoelectronic properties, which highlighted the relevance of structural order for charge transport properties within this class of materials.^[40,41]

This is one of the most notable examples within the remarkable progress that has recently led to the development of improved *p*-type polymers and of high-performance polymer OFETs. A brief historical summary of key *p*-channel polymers can be found in Ref. [19]. As it can be seen in Figure 4, beyond the first-generation polymer semiconductors (e.g. polytriarylamine (PTAA), poly(9,9-diocetylfluorenyl-2,7-diyl-co-bithiophene) (F8T2),

and polycarbazole), recently a variety of important new structures for building high performance opto-electronic polymer semiconductors have been developed, such as condensed-ring thiophenes (PFQT),^[42] N-alkyldithieno[3,2-b;2',3'-d]pyrrole (DTP),^[43] benzo[2,1-b;3,4-b']dithiophene (BDT),^[44] thienylenevinylene (TV) derivatives,^[45] cyclopentadithiophene (CDT),^[46] benzothiadiazole (BTZ),^[46] isoindigo,^[47] and indacenodithiophene (IDT)^[48] containing homo- and copolymers.

Notably, Mei et al. demonstrated a novel siloxane-terminated solubilizing group as side chains in an isoindigo-containing polymer, PII2T-Si in Figure 4.^[47] This showed high hole mobility, up to 2.48 cm²/Vs, thanks to an enhanced charge transport due to a shorter π–π stacking distance of 3.58 Å compared to the reference alkyl-chain terminated polymer (π–π stacking distance of 3.76 Å) and a larger crystalline coherence length.^[47] Moreover, Li et al. reported OFETs with a very high charge carrier mobility of ~10 cm²/Vs,^[37] which is the present record for polymer semiconductors. To achieve such a remarkable field-effect mobility, which approaches values that were so far thought to be accessible only with very highly ordered small molecule organic semiconductors, they used a conjugated alternating electron donor-acceptor (D-A) copolymer with dithienylthieno[3,2-b]thiophene (DTT) as the donor and

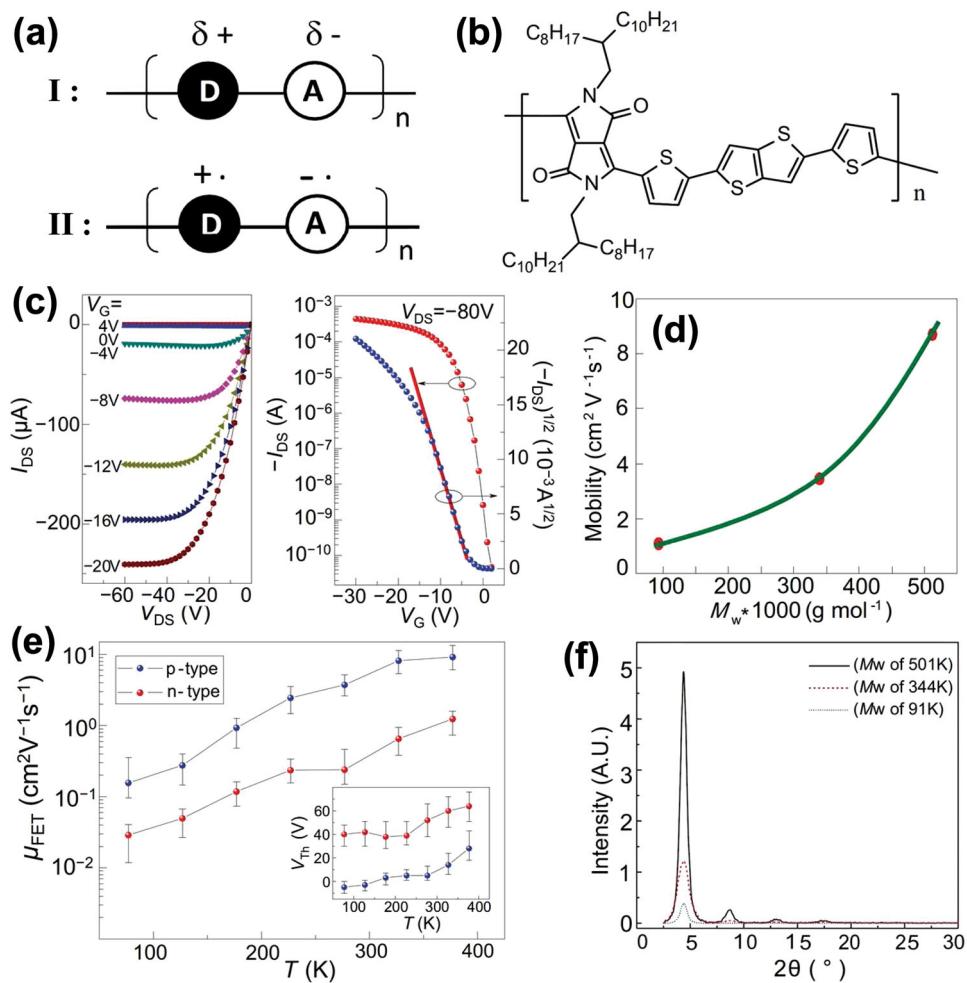


Figure 5. (a) Schematic partial charge-transfer ground state I and biradical anion-cation state II and (b) chemical structure of DPP-DTT-based conjugated polymer. (c) Output and transfer characteristics of Si/SiO₂ with alkyl-silyl SAMs bottom-gate and Au bottom-contact structure OFET, (d) The dependence of the average saturated mobility of five representative devices on the semiconductor weight-average molecular weight (M_w). (e) Temperature dependence of electron and hole mobilities in vacuum (the inset reports the temperature dependence of threshold voltage, V_{Th}). (f) X-ray diffraction peaks for verifying the increased crystallinity of a thin film (100 nm) of DPP-DTT-based polymer semiconductor as a function of increasing M_w .^[37] Reproduced with permission from Ref. [37]. Copyright 2011, Nature publishing group.

a comparatively weaker acceptor moiety, 1,4-diketopyrrolo[3,4-c]pyrrole (DPP) (Figure 5b). This type of D-A copolymer has been considered an extremely important building block in the development of high-mobility polymer semiconductors, and although there is no general consensus on the fundamental reasons leading to enhanced charge transport properties,^[49] it is a fact that more and more research groups converged in synthesizing semiconductors based on this kind of basic architecture.^[50] One proposed reason for the achievement of high charge carrier mobility is that the conjugated alternating D-A polymer makes it feasible to create a ground state that is a partial charge-transfer state, as schematically described as state I in Figure 5a: the weakly polarized state I is believed to have a beneficial effect both on charge injection and transport by promoting a very small π - π stacking distance and thus greatly boosting the effective charge transport efficiency.^[37] The extent of ground-state charge transfer in a conjugated alternating D-A copolymer can be modulated by changing the relative donor

and acceptor strengths and the nature of the π -conjugation within the polymer framework,^[37] with the limit of maintaining the semiconducting properties and avoiding a formal charge separation as in state II. This state, corresponding to a biradical anion-cation, would be a conducting state much like the intermolecular charge-transfer complexes in tetrathiafulvalene-tetracyanoquinodimethane (TTF-TCNQ)^[51] and poly(3,4-ethylenedioxythiophene):poly(styrene sulfonate) (PEDOT: PSS).^[52]

In fact, there has been a variety of reports on DPP-based D-A copolymer semiconductors with a wide range of mobilities from $\sim 0.1 \text{ cm}^2/\text{Vs}$ to $\sim 2 \text{ cm}^2/\text{Vs}$, with most being around $1 \text{ cm}^2/\text{Vs}$.^[53–63] Synthesis of high-molecular-weight polymers (number average/weight average molecular weight, $M_n/M_w = 320 \text{ k} / 840 \text{ k}$) and optimization of the fabrication processes can yield simple DPP-DTT-based conjugated polymers with extremely high hole mobilities of over $10 \text{ cm}^2/\text{Vs}$ [see Figure 5d], high ON- to OFF-current ratio (I_{on}/I_{off}) of $\sim 10^6$, exceptional device shelf-lives, and exceptional operational

stabilities. In such devices, as shown in Figure 5e, a temperature activated transport was found, where the activation energies for hole and electron conduction were estimated to be ~60 meV and ~49 meV, respectively. This is indicative of a hopping transport mechanism instead of the, still largely debated, band-like transport reported for highly ordered small molecule semiconductors. It is quite interesting that such high charge carrier mobility is achievable via a hopping mechanism in a solution-processed, inherently more disordered, polymer semiconductor. Finally, researchers have shown a high inverter gain of 92 and a five-stage ring oscillator with a ~1.2 kHz operating frequency based on the *p*-only device configuration. The relatively low operation frequency obtained can mainly be attributed to the wide channel length and large parasitic capacitance of the printed ring oscillator.^[37]

2.3. *n*-type Polymer Semiconductors

In comparison to *p*-type materials, *n*-type organic semiconductors have been less developed. Recently, however, a number of π -conjugated organic molecules for *n*-type OFETs have been demonstrated based on the understanding of the intrinsic and extrinsic factors that determine the electron injection and transport properties in OFETs.^[64] As for the intrinsic factors, the electron-transport materials should have a proper electronic structure that yields the desired electron deficiency and strong π -stacking between adjacent molecules.^[64] Notably, many experimental and theoretical studies have suggested that organic π -conjugated semiconductors can transport electrons as efficiently as or even more efficiently than holes.^[19] However, electron-deficient materials have small reduction potentials and thus relatively low-energy LUMOs, which typically leads to larger electron injection barriers for injection from the commonly used high-work-function (W_f) metal electrodes (e.g. Au) as well as weak processing and operating stabilities in air. Energetically favourable low- W_f metal electrodes, such as Ca and Sm electrodes, have problems attributed to easy air-induced oxidation. Besides the intrinsic semiconductor electronic structure, there are several other key factors affecting the *n*-type OFET characteristics, such as the semiconductor-dielectric interface chemistry, metal electrode contact, and ambient conditions. In a pioneering study, Chua et al. reported the general electron transport behaviour in various π -conjugated organic semiconductors that were previously believed to be *p*-type only semiconductors. These results were obtained by effectively passivating the electron-trapping hydroxyl groups on the SiO_x gate dielectric surface.^[65] Hydroxyl-free polymer gate dielectrics can also effectively remove the electron traps and thus typically show better *n*-type transistor properties.

Fortunately, most of these concerns can be effectively addressed either by designing and synthesizing a chemical structure that will provide high electron mobility and high stability under air and under the device operating conditions, or by optimizing the fabrication process and device architecture. It should be noted that top-gate/bottom-contacts (TG/BC) OFETs using *n*-type polymer semiconductors and hydroxyl-free polymer gate dielectrics generally

show higher electron mobilities, better air-stability attributed to the auto-encapsulation effect of the overlaid gate electrode and dielectric layers, and smaller contact resistance (R_c) resulting from the large charge injection area from the BC electrode to the top semiconductor-dielectric interface.^[66,67] From an energetic perspective, it is now believed that there is a quite narrow energetic window for the LUMO level, located approximately between -4.0 and -4.3 eV, in which good electron transport behaviour is possible in organic semiconductors under ambient conditions.^[19] For *n*-type organic semiconductors with higher LUMO energies (i.e. low electron affinities) than the above values, the *n*-channel OFET performance rapidly degrades after exposure to air, including when electron-trap-free dielectrics are used.^[19]

Figure 6 shows the chemical structures of representative *n*-type polymer semiconductors. A brief historical summary of the *n*-channel polymers can be found in a few references.^[19,64] In this section, we briefly describe the most remarkable progress recently achieved in the *n*-type polymer semiconductor field. Yan et al. developed the high mobility *n*-type polymer semiconductor poly([*N,N'*-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,5'-(2,2'-bithiophene)) (P(NDI2OD-T2)) which shows an electron mobility as high as 0.85 cm²/Vs and low threshold voltages.^[68] The electron-deficient *N,N'*-dialkynaphthalenedicarboximide (NDIR) comonomer was used for the development of P(NDI2OD-T2), because it has a large electron affinity that is comparable to that of the far more π -extended *N,N'*-dialkylperylene dicarboximide (PDIR) systems and because the NDIR-Br₂ can be easily isolated as pure 2,6-diastereoisomers, enabling the synthesis of a regioregular polymeric backbone.^[19] Therefore, the NDIR can lead to a structure that is more π -conjugated than that of PDIR, in turn leading to better charge transport efficiency. Proper alkyl (R) functionalization at the rylene nitrogen atoms, with 2-octyldodecyl (2OD) in the previous study, resulted in polymers that were highly soluble in common organic solvents, and processable with various printing techniques.^[19] Finally, the dithiophene (T2) unit was also utilized because of its commercial availability, stability, and known electronic structure and because of the geometric characteristics of the core, which provide highly π -conjugated, planar, rod-like polymers.^[19,68] Notably, the P(NDI2OD-T2) has a very low R_c with a BC Au electrode,^[69] which makes it possible to build complementary circuitry by combining it with *p*-type OFETs based on the same device structure.^[70] Thanks to this, printed inverters with high gains of 25–60 were demonstrated using P(NDI2OD-T2) (*n*-type), P3HT (*p*-type), and ActivInkTM D2200 (gate dielectric) (see **Figure 7**).^[68]

2.4. Ambipolar Polymer Semiconductors

A polymer semiconductor is considered unipolar if it shows measurable currents for only one type of carrier or if it is characterized by a strong unbalance between holes and electrons mobility. In contrast, in an ambipolar polymer both electrons and holes can be transported with comparable mobilities. As previously discussed, the general observation of the *n*-channel

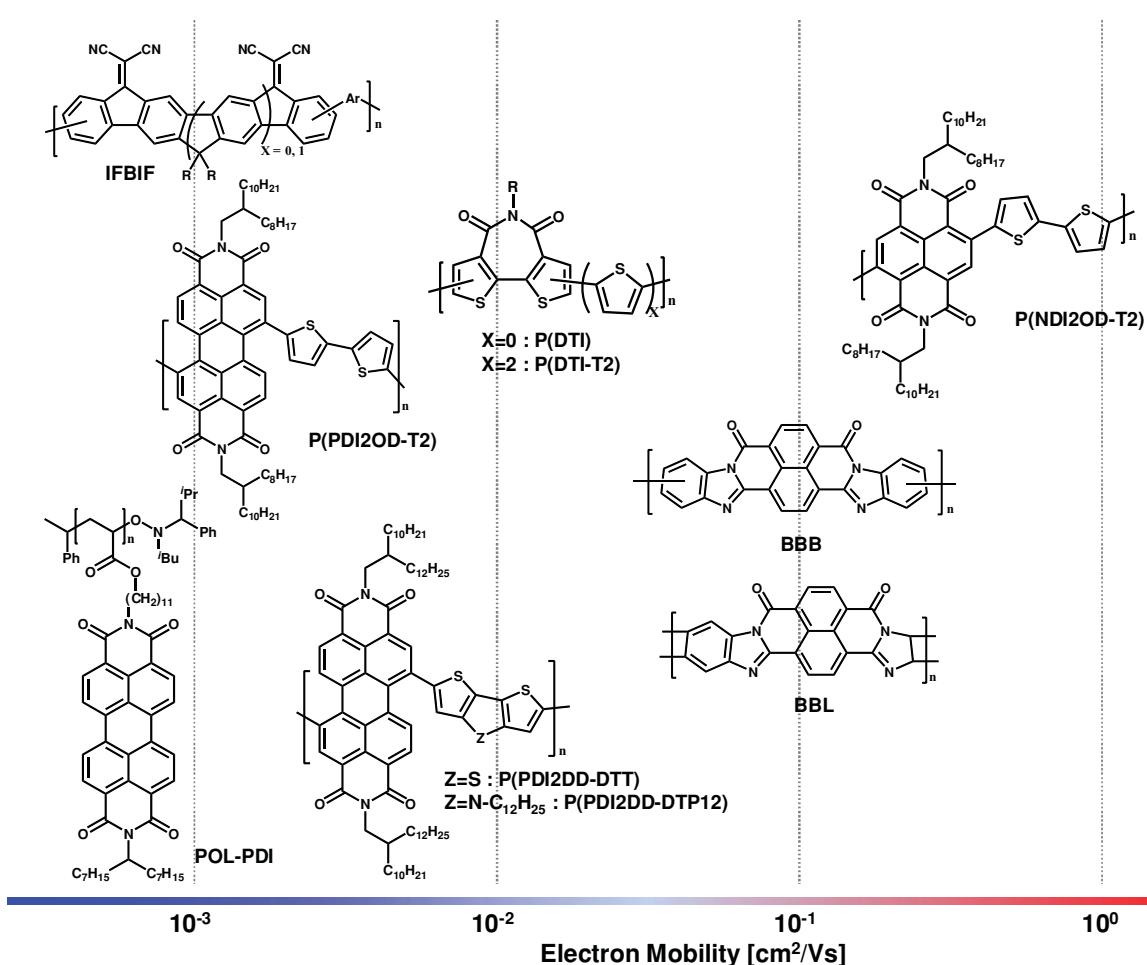


Figure 6. Chemical structures and corresponding charge carrier mobilities of representative *n*-type polymer semiconductors.

behaviour in organic semiconductors, when electron traps due to hydroxyl, silanol, and carbonyl groups are excluded, provided an important understanding both for developing high performance *n*-type and ambipolar organic semiconductors.^[65] Importantly, for efficient charge injections of both carriers into the same active channel from the common source/drain electrodes, the ambipolar semiconductors should have a small bandgap (below 2 eV) compared to unipolar semiconductors. Typically, but not necessarily, this has been achieved by the same D-A copolymer-like chemical structure, characterized by the copolymerization of electron-rich and electron-deficient heteroaromatic units, described in the previous section.^[19] These so-called push-pull copolymers (Figure 8) are strongly coupled and the reduced bond length alternation effectively reduces band-gap.^[71] Notably, the copolymer reported by Reynolds et al., obtained by coupling the strong donor DTP with the strong acceptor (4,8-dithien-2-yl-2λ⁴δ²-benzo[1,2-*c*;4,5-*c'*]bis[1,2,5]thiadiazole) BThBBT (P(DTP-BThBBT)), shows one of the lowest optical bandgap value obtained so far, which is as low as ~0.5–0.6 eV.^[72] Figure 8 shows the chemical structures and the corresponding charge carrier mobilities of representative ambipolar polymer semiconductors. The properties of OFETs based

on recently developed ambipolar polymer semiconductors are reported in Table 1.^[19]

DPP-based copolymers are representative materials with a strong ambipolarity. Impressive carrier mobilities for both electrons and holes, that are close to or even higher than those of the state-of-the-art unipolar conjugated polymers, have been recently reported for this class of copolymers. Based on the siloxane-terminated solubilizing group previously introduced by Mei et al.,^[47] very recently Lee et al. reported the solution-processable donor-acceptor type copolymer consisting of the DPP unit and hybrid siloxane substituents at the nitrogen atoms of this unit (abbreviated PTDPSe-Si, in Figure 9). Figure 9 shows the design motif for the PTDPSe-Si polymer semiconductor and its fabrication technique for achieving hole and electron mobilities of 3.97 and 2.20 cm^2/Vs , respectively.^[36]

3. Graphic Arts Printing Technology

The attractiveness of printed electronics technology mainly resides in the possibility of preparing stacks of micro-structured layers, and thereby thin-film devices, in a much simpler

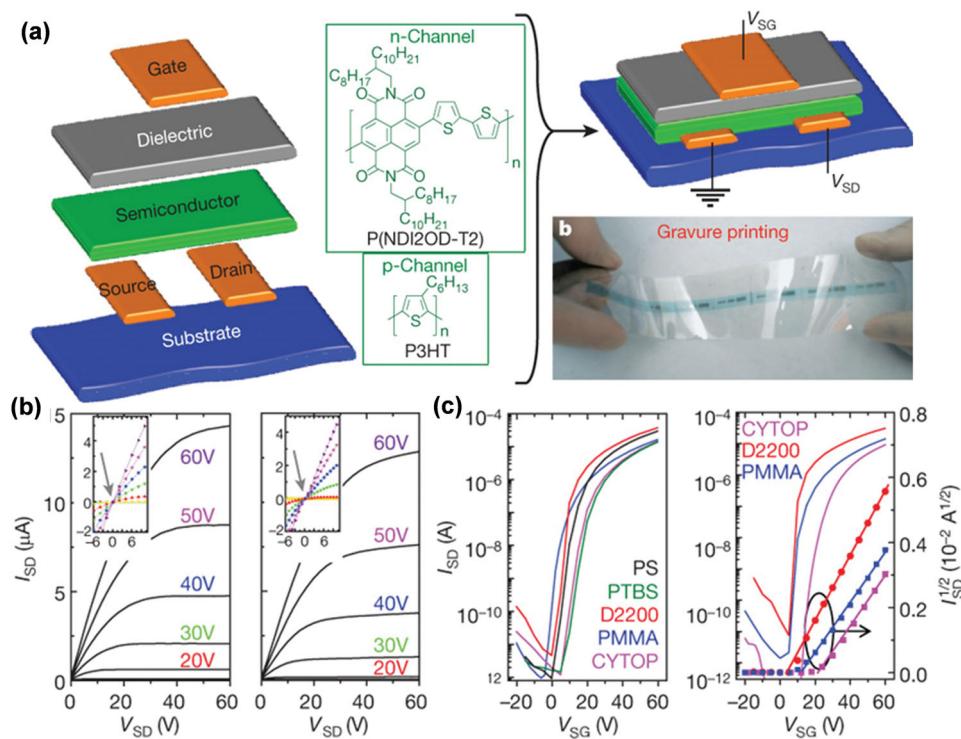


Figure 7. (a) Illustration of TFT material components (left), chemical structures of P(NDI2OD-T2) and P3HT semiconducting polymers, and illustration of the TG/BC TFT architecture (right). (b) TFT output plot for a PMMA-based (left) and a poly(4-tert-butyl styrene) (PTBS)-based (right) device on glass. Inset: low-voltage scan (axes same as main plot). (c) TFT transfer plots for representative TG/BC devices on glass using the indicated polymeric dielectrics (left) and TFT transfer plot for representative devices on PET using the indicated polymeric dielectrics (right). Reproduced with permission from Ref. [68]. Copyright 2009, Nature publishing group.

and cost-effective process flow than in the case of photolithography used for conventional electronics. In addition to this advantage, printing of functional inks allows to implement opto-electronic functionalities on a large variety of non-rigid media, from plastics to paper, paving the way for novel applications. Various techniques, traditionally developed for the graphic arts printing (GAP) sector, have been used for printed electronics: inkjet, spray, and screen printing, and the so-called mass-printing methods, such as gravure, reverse-offset, and flexographic printing (Figure 10).^[85] Mass-printing methods are commonly employed in web-based R2R fabrication, whereas inkjet printing and screen printing are mostly used as sheet-fed methods, though being compatible with R2R processes as well and already adopted in the GAP in such way. The selection of the most suitable printing method used for fabricating opto-electronics products is mostly determined by the requirements for the printed layers, the rheological properties of the materials, and economical and technical considerations. Typical features and characteristics of the various printing technologies are listed in Table 2.

The mass-printing methods, such as gravure, reverse-offset, and flexographic printing are much more productive than other printing techniques, with a high throughput of 10–60 m²/s. Therefore, they are especially suitable for achieving a dramatic reduction in fabrication costs when they are used in electronics applications.^[85] Usually standard tools show a quite limited lateral resolution and registration in the context of microelectronic devices, and they are better suited for the fabrication of large

area applications with limited need for fine patterning, such as polymer solar cells, fuel cells, and loudspeakers.^[86,87] Apart from the solar cells case, there are limited examples in the literature reporting the use of these tools to develop other opto-electronic organic devices. In the case of OFETs, both gravure^[88] and reverse-offset^[89] were adopted to define different parts of the transistor stack. In particular, reverse-offset printing achieves the highest resolution among these techniques down to ~5 μm.^[89]

The inkjet printing process is a flexible and versatile digital printing method. Because it can be set up with relatively little effort at laboratory scales, it is presumably the most commonly used printing method for printed electronics.^[90] Inkjet printing is well suited for low-viscosity, highly soluble materials, such as organic semiconductors and conducting polymers. With high-viscosity materials, such as dielectrics, dispersed nano particles, and inorganic metal inks, difficulties due to clogging of the nozzles often occur. Notably, inkjet printing has a disadvantage compared to mass-printing technology in terms of throughput (0.01–0.5 m²/s); moreover, while the resolution achievable with conventional inkjet is better or at worst comparable with that offered by the other printing methods (20–50 μm), film uniformity and homogeneity is also limited because of the drop-wise deposition of layers. Although these problems have been addressed using parallelization (usage of multi-nozzle print heads) and pre-structuring of the substrate to contain the jetted inks with suitable banks, inkjet printing has mainly been employed for rough patterning of the active semiconductor and electrodes.

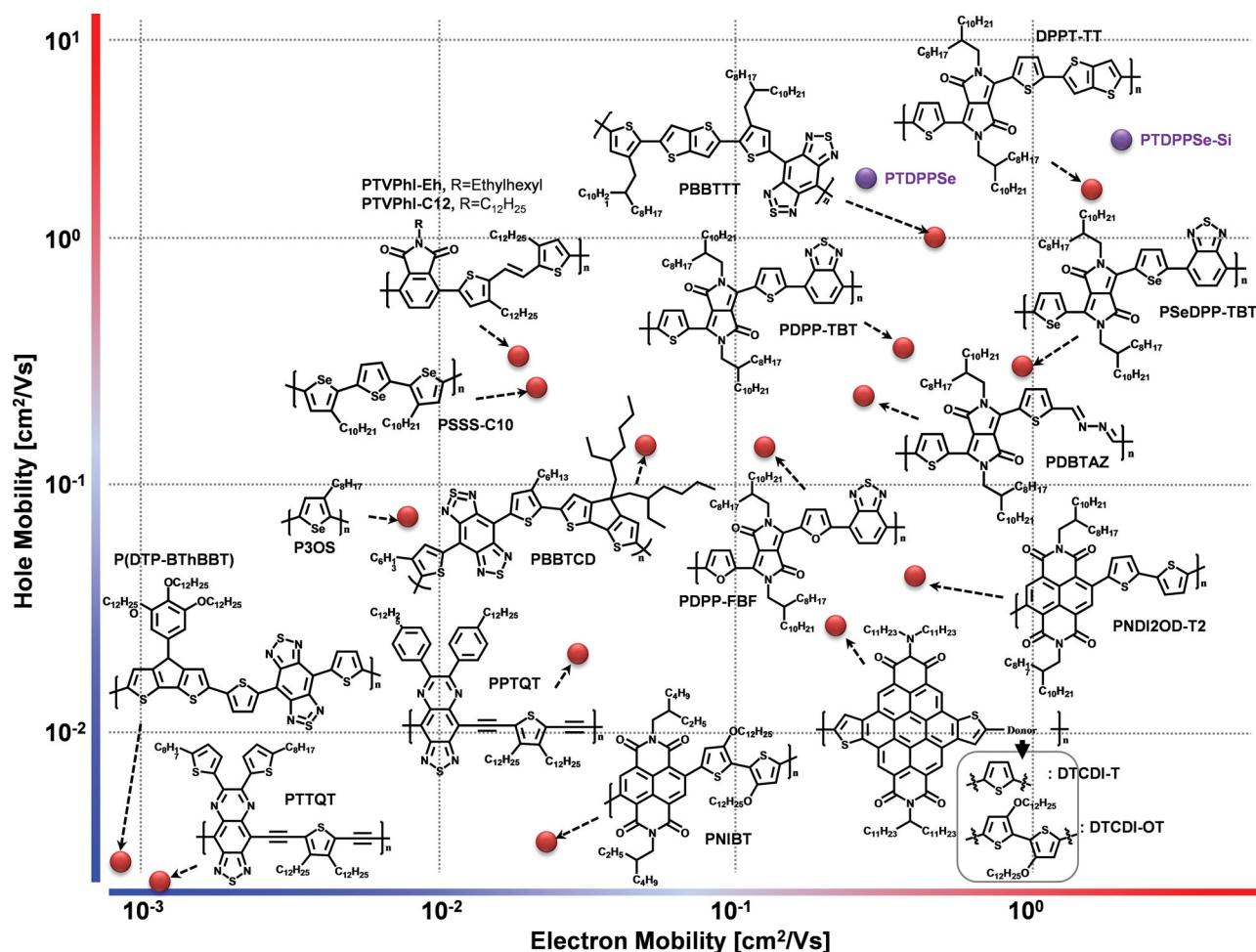


Figure 8. Chemical structures and charge carrier mobilities of representative ambipolar polymer semiconductors. Chemical structures of the PTDPPSe and PTDPPSe-Si are shown in Figure 9.

Screen printing, which allows preparing thick layers (from 1 to several microns) from paste-like functional inks, has been used in a broad range of applications for the fabrication of electric and electronic components on industrial scales. This method is mainly used to prepare conducting lines from inorganic conductors, such as those on printed circuit boards (PCB) and RFID tag antennas, and insulating/passivation layers, for which a relatively high layer thickness is necessary but a high resolution is not important, have also been prepared using this method. The printing speed (2–3 m²/s) and resolution (20–100 μm) are also limited, as with inkjet printing.

Comprehensive description of these printing techniques can be found in a few references.^[85,91] Besides these conventional printing methods, new but similar techniques have also been employed, among them, electrohydrodynamic (EHD) jet printing,^[92] micro-contact printing,^[90] and nanoimprint lithography (NIL).^[93]

Note that a number of technological issues (summarized in Table 3), in terms of materials, devices, printing process, and transfer of this technology from lab to fab manufacturing scale, have still to be overcome. Moreover, the different

printing techniques have specific difficulties associated with them. Although it is very hard to address all these difficulties, the most important parameter determining the printability of materials is the viscosity and surface tension of functional inks. Notably, these parameters are strongly depending on solvent, concentration, solubility of the materials, etc. In the case of polymer semiconductors, the printability of inks that should be optimized to each printing tools can be tuned by changing the functional groups in the polymer backbone and/or side groups to induce different solubility in various solvents, and changing the molecular weight and interactions between the molecules. In addition, the other important issue for printed and organic electronics is a flexible (or stretchable if required) substrate affordable for web-based R2R processes. For most applications in printed electronics, the engineered substrates should overtake a variety of key technical challenges, such as low shrinkage, low coefficient of thermal expansion, upper temperature limit for processing, low surface roughness, high solvent and moisture resistance, environmental compatibility, transparency and rigidity. Moreover, all these characteristics should be found in a substrate which is commercially available at a reasonably low price.

Table 1. OFET characteristics of representative ambipolar polymer semiconductors.

Semiconductor	Structure	Dielectric	Contact (Treatment)	$\mu_{FET,h}$ [cm ² /Vs] ($V_{Th,h}$)	$\mu_{FET,e}$ [cm ² /Vs] ($V_{Th,e}$)	Ref.
PDPP-TBT	TG/BC	D139	Au/Cr (PFBT)	0.53 (-17.1 V)	0.58 (15.8 V)	[73]
		SiO ₂ /OTS	Au	0.35	0.40	[60]
		PMMA	Au	0.33	0.57	[74]
PSeDPP-TBT	TG/BC	PMMA	Au	0.46	0.97	[74]
PSSS-10	TG/BC	PMMA	Au	0.30	0.030	[75]
P3OS	TG/BC	PMMA	Au	9.0×10^{-2}	9.0×10^{-3}	[75]
PNIBT	BG/BC	SiO ₂	Au	2.4×10^{-3} (-42.9 V)	3.8×10^{-2} (19.9 V)	[76]
PBBTCD	BG/BC	SiO ₂	Au	0.11	0.074	[77]
PBBTPD	BG/BC	SiO ₂	Au	9.6×10^{-3}	8.2×10^{-3}	[77]
PBBTFL	BG/BC	SiO ₂	Au	5.6×10^{-3}	7.0×10^{-4}	[77]
PBPTSID	BG/BC	SiO ₂	Au	1.9×10^{-3}	1.1×10^{-2}	[77]
DPPT-TT	TG/BC	PMMA	Au	1.36	1.56	[78]
PTVPhI-Eh	TG/BC	PMMA	Au	0.54 (-42.9 V)	0.022 (61.1 V)	[79]
			Au/Cs ₂ CO ₃	0.03 (-56.8 V)	0.089 (56.3 V)	
			Au/CsF	0.04 (-63.0 V)	0.26 (44.3 V)	
PTVPhI-C12	TG/BC	PMMA	Au	0.07 (-46.9 V)	0.010 (52.3 V)	[79]
			Au/Cs ₂ CO ₃	0.01 (-66.1 V)	0.068 (49.7 V)	
			Au/CsF	0.03 (-61.3 V)	0.10 (49.9 V)	
P(NDI2OD-T2)	TG/BC	PMMA	Au	5.0×10^{-3} (-34.5 V)	0.26 (7.5 V)	[80]
		P(VDF-TrFE)	Au	0.11 (-20.4 V)	0.093 (12.3 V)	
PPTQT	BG/BC	SiO ₂ /HMDS	Au	0.028	0.042	[81]
PTTQT	BC/BC	SiO ₂ /HMDS	Au	1.3×10^{-3}	1.1×10^{-3}	[81]
PDPP-FBF	BG/TC	SiO ₂ /OTS	Au	0.18	0.16	[57,58]
DTCDI-T	TG/BC	PMMA	Au	0.04 (-41 V)	0.30 (34 V)	[56]
DTCDI-OT	TG/BC	PMMA	Au	3.0×10^{-3} (-65 V)	3.0×10^{-2} (47 V)	[56]
P(BtimR-T)	BG/TC	SiO ₂	Au	3.6×10^{-4} (-95 V)	4.6×10^{-4} (100 V)	[82]
PBBTTT	BG/BC	SiO ₂ /DTS	Au	1.0	0.7	[83]
P(DTP-BThBBT)	BG/BC	SiO ₂ /OTS	Au	1.2×10^{-3}	5.8×10^{-4}	[72]
PDBTAZ	TG/BC	CYTOP	Au	0.36	0.41	[84]
PTDPPSe	BG/TC	SiO ₂ /OTS	Au	2.53	0.43	[36]
PTDPPSe-Si	BG/TC	SiO ₂ /OTS	Au	3.97	2.20	[36]

4. Printed Integrated Circuits

4.1. Basic Aspects of Complementary Inverters and Ring Oscillators

Complementary metal–oxide–semiconductor (CMOS) technology is used for making ICs that consist of complementary and symmetrical pairs of *p*-type and *n*-type metal–oxide–semiconductor field-effect transistors (MOSFETs) for logic functions.^[94] This CMOS technology has been widely used in most microprocessors, microcontrollers, static random access memory (SRAM) modules, and other digital logic circuits as well as for a wide variety of analogue circuits, such as image sensors, data converters, and highly integrated transceivers for many types of communication.^[95] The most

basic and fundamental element in ICs is the CMOS inverter, which carries out the ‘NOT’ logic function. Note that the electrical behaviours of the above complex electronic circuitry can be derived almost completely by extrapolating the results obtained for inverters. The analysis of inverters can be extended to explain the behaviour of more complex logic gates, such as NAND, OR, NOR, or XOR gates. Therefore, once the operation and characteristics of the CMOS inverter are clearly understood, designing more complex structures, such as logic gates, adders, and multipliers, becomes greatly simplified.

As shown in Figure 11, an inverter can be built using either a unipolar or an ambipolar logic. Unipolar circuits are typically designed when the *p*-type and *n*-type semiconductors do not have equivalent transistor characteristics, such as when *n*-type

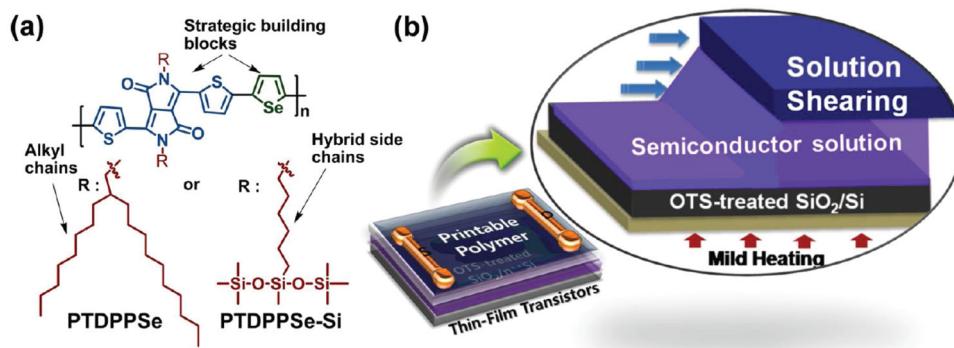


Figure 9. Design motif and solution-shearing schematic. (a) Molecular structures of the PTDPPSe and PTDPPSe-Si and (b) schematic illustration of TFT structure and solution-shearing technique. Hybrid side chains include a siloxane substituent combined with alkyl chain. Reproduced with permission from Ref. [36]. Copyright 2012, American Chemical Society.

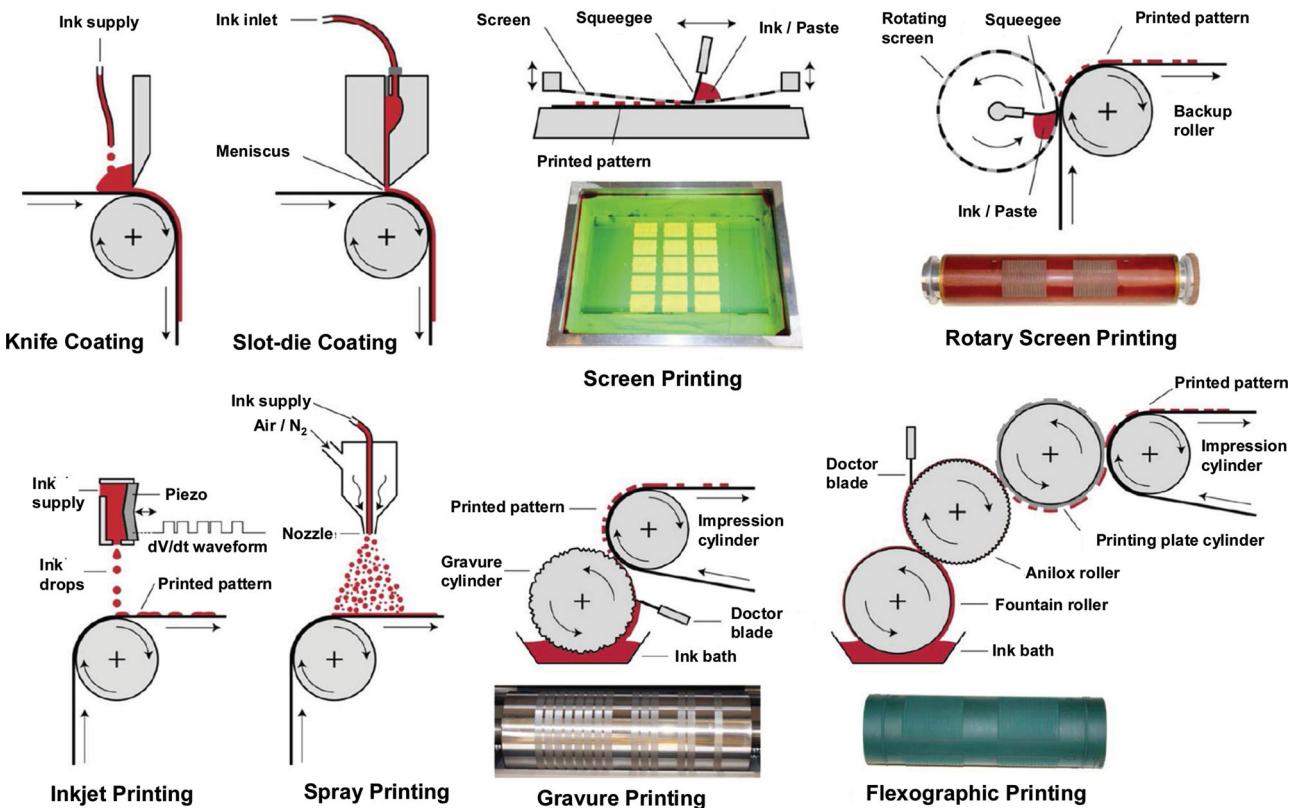


Figure 10. Schematic illustration of printing techniques: knife coating, slot-die coating, screen printing, rotary screen printing, inkjet printing, spray printing, gravure printing, and flexographic printing. Reproduced with permission from Ref. [85]. Copyright 2012, John Wiley & Sons, Inc.

Table 2. Characteristics of the various printing techniques.

Printing Techniques	Viscosity [Pas]	Thickness [μm]	Feature Size [μm]	Throughput [m^2/s]	Registration [μm]	Features
Flexography	0.05–0.5	0.04–2.5	80	3–30	<200	Inexpensive plate pattern, high throughput, thick layer/ low viscosity ink
Gravure	0.01–0.2	< 0.1–8	75	3–60	>20	Fast printing, high resolution, relatively high plate cost, low dot gain
Offset	5–100	0.5–2	10–50	3–30	>10	High quality, high throughput, need for ink additives
Screen	0.5–50	0.015–100	20–100	2–3	>25	Robust, simple, thick layer, large feature size, high ink viscosity, slow speed
Inkjet	0.001–0.04	0.01–20	20–50	0.01–0.5	5–20	Non-contact, small ink quantities, digital printing, low viscosity ink, slow speed

Table 3. Technological issues in printed electronics.

Technology	Challenges
Materials	<ul style="list-style-type: none"> • Ink formulation and viscosity required to each printing process • Printability to under-laid layer • Ink stability (particle agglomeration, settling, etc.) • Material lifetime after exposure to moisture, oxygen, and ozone, etc. • Cost (e.g. expensive Au and Ag vs Cu) • Reliability (organic/inorganic semiconductors, nanowires, nano carbon materials, etc.) • Film thickness uniformity • Performance (charge carrier mobility, photo conversion efficiency, etc.) • Process and solvent compatibility • Wetting properties (surface tension, surface energy)
Devices	<ul style="list-style-type: none"> • Parasitic capacitance (e.g. overlap capacitance between S/D and gate electrodes) • Feature size (affecting device area and operating speed) • Device-to-device uniformity • Reliability and yield (due to pinholes, rough surface roughness, etc.) • Encapsulation (for longer lifetime) • Process compatibility of sequential device layers • Device architecture (top-gate or bottom-gate, bottom-contact or top-contact)
Printing process	<ul style="list-style-type: none"> • Registration, deposition accuracy • Throughput and printing speed • Chemical compatibility of materials (orthogonal solvents) • Physical compatibility (step coverage, work function, etc.) • Curing/drying of inks within thermal tolerances and time • Online quality control to optimize process yield • Controlled atmosphere for sensitive materials
Manufacturing (from lab to fab)	<ul style="list-style-type: none"> • Environmental impact, disposability • Benign solvents for health and safety • Process time and print speed • Photonic (UV curing or laser sintering) and thermal curing • Thermal budget • Substrate tension, layer thickness • Yield, uniformity, process monitoring, • Packaging • Operation in air and at elevated temperatures for commercial products

or *p*-type behaviour is dominant for amorphous oxide semiconductors or organic semiconductors, respectively. A complementary design, which offers low power consumption, higher switching speed and stronger robustness to noise, is possible when both *n*-type and *p*-type transistors are available and show reasonably balanced field-effect mobilities (μ_{FET}) and threshold

voltages (V_{Th}). “CMOS-like” logic can be implemented both with the close patterning of two different unipolar *n*-type and *p*-type semiconductors, and with a single ambipolar semiconductor. **Figure 12** shows an example of a generic CMOS inverter and its basic operation mechanism, which is in general applicable to any of the “CMOS-like” schemes described above, provided that the two transistors in the logic gate behaves as perfect unipolar devices; this is not usually the case when adopting an ambipolar polymer and a suitable unipolarization of devices has to be implemented, as it is discussed in Section 6. An input voltage (V_{IN} ; logic ‘1’) at the input would make the *p*-type transistor turn OFF and the *n*-type transistor turn ON, pulling the output voltage (V_{OUT}) close to the low supply voltage (ground, GND; logic ‘0’). A logic ‘0’ V_{IN} voltage, on the other hand, will make the *p*-type transistor turn ON and the *n*-type transistor turn OFF, pulling V_{OUT} close to high supply voltage (V_{DD}), i.e. logic ‘1’. At the various switching points from A to E in Figure 12, the *p*-type and *n*-type transistors are operating in different regimes, specified in the panel (b).

By considering the voltage transfer characteristics (VTCs) of the basic inverter, as shown in **Figure 13a**, the switching threshold (V_{inv}) corresponds to the point on the curve where V_{IN} is equal to the V_{OUT} . At this point, both the *p*-channel and *n*-channel OFETs are operating in the saturation region. Since the drain current (I_d) in each OFETs must be equal, it follows that in the saturation region:^[96]

$$\frac{\beta_n}{2}(V_{inv} - V_{Th,n})^2 = \frac{\beta_p}{2}(V_{DD} - V_{inv} - V_{Th,p})^2 \quad (1)$$

where V_{Th} is the threshold voltage, $\beta = (W/L)\mu C_i$, in which W indicates the FET channel width, L the channel length, μ the field-effect mobility and C_i the dielectric specific capacitance, is a design factor for adjusting the OFET *p*- and *n*-channel saturation currents, and the subscripts *p* and *n* denote the semiconductor type. Therefore, V_{inv} can be expressed by the following equation^[96]:

$$V_{inv} = \frac{\sqrt{\frac{\beta_n}{\beta_p}} \cdot V_{Th,n} + (V_{DD} - V_{Th,p})}{1 + \sqrt{\frac{\beta_n}{\beta_p}}} \quad (2)$$

where β_p and β_n are the design factor, and $V_{Th,p}$ and $V_{Th,n}$ the threshold voltages for *p*- and *n*-channel OFETs, respectively. It is noted that if V_{inv} is shifted from $\frac{1}{2}V_{DD}$ (the ideal switching point for a CMOS inverter with equivalent *p*- and *n*-type transistors) because of the μ and V_{Th} differences between the *p*- and *n*-channel OFETs, the design factor (β) must be properly adjusted, mainly by changing W/L , to obtain equivalent saturation currents for the *p*-type and *n*-type OFETs. Whether an inverter works properly or not is determined by a set of functional criteria. The first criterion is that the inverter gain (g_{inv}), which is obtained by calculating the absolute value of dV_{OUT}/dV_{IN} in the inverting region, must be > 1 ; in reality, to work in a complex circuit, this should be as high as possible, with different authors indicating a value between 4 and 10 as the minimum required value.^[97] Two important characteristics of CMOS circuits are their high noise immunity and very low static power consumption. The noise margin (NM) is the maximum noise signal that

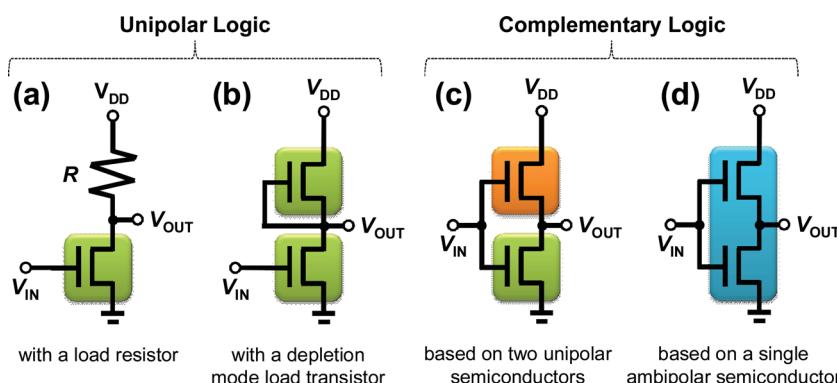


Figure 11. Various circuit configurations for the organic inverters: (a) and (b) are unipolar architectures, while (c) and (d) represent complementary “CMOS-like” configurations. *p*-type only or *n*-type only semiconductor based unipolar inverter with a load resistor (a) or (b) a depletion mode load transistor. (c) Complementary inverter consisting of two different *p*-type and *n*-type unipolar semiconductors. (d) Complementary inverter based on a single ambipolar semiconductor.

can be superimposed on a digital signal without causing a malfunction of the circuit. Figures 13a and 13b show the VTC curve of an inverter and the definition of the noise margin. NMs have been defined in the literature in several different ways, following different criteria.^[98] The maximum equal criterion is probably the

most adopted one in the literature on organic electronics.^[99] In this case, the NM is simply defined as the side of the largest square that can be inscribed within the loop formed by the VTC curves of an inverter pair. However, most of the digital circuits textbooks report a different criterion, usually indicated as the “-1” slope criterion, likely due to the fact that it is easy to find an analytical expression for each quantity involved. In the following we describe this criterion. The maximum/minimum input and output voltages (V_{IH}/V_{IL} and V_{OH}/V_{OL}) are defined by the critical points where $g_{inv} = 1$ (Figure 13a and b). The noise margins at the high (NM_H) and low levels (NM_L) are described in the following Equations:

$$NM_H = V_{OH} - V_{IH} \quad (3)$$

$$NM_L = V_{IL} - V_{OL} \quad (4)$$

Note that the minimum required value for the noise margin is typically 10% of $\frac{1}{2}V_{DD}$.^[97]

As a way to test the operation of inverters in a logic circuit and to extract useful information about the achievable switching frequency of a given logic technology, usually a ring

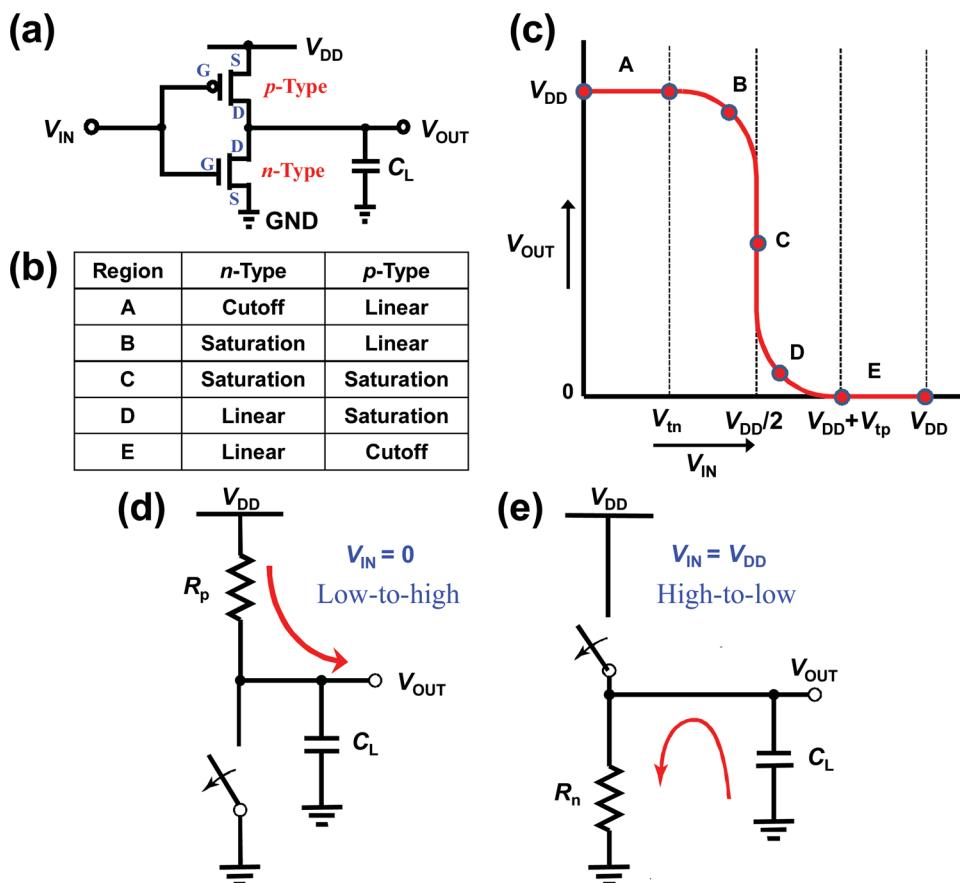


Figure 12. CMOS inverter characteristics. (a) Circuit configuration, (b) characteristic operation regions, and (c) corresponding voltage transfer characteristics for a CMOS inverter. Schematic descriptions during the operation of CMOS inverter (d) at $V_{IN} = 0$ V and (e) $V_{IN} = V_{DD}$.

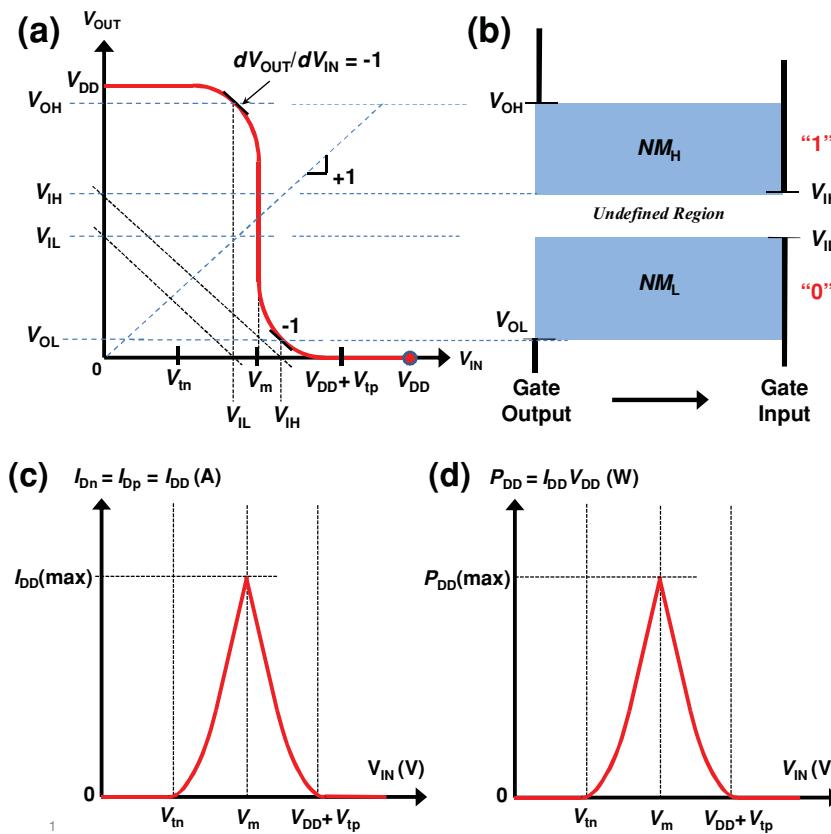


Figure 13. CMOS inverter characteristics. (a) VTC and (b) corresponding noise margins. (c) I_{DD} and (d) its power consumption during the operation of CMOS inverter. V_m in the figure is same definition with V_{inv} .

oscillator is realized (Figure 14c). A ring oscillator is a simple circuit composed of an odd number of inverters, connected in a chain, where the output of the last inverter is fed back into the first one. Each gate inverts the logic value at its input, so that given the odd number of gates, the last inverter will negate the input of the first one, imposing an oscillation to the circuit limited by the time needed by the signal to propagate through the inverting chain.

In fact, in a physical device, no gate can switch instantaneously. Thus, in a device fabricated with FETs, for example, the gate input capacitance must be charged by the preceding gate output current in order to alter its voltage level. This delay adds up at each gate, so that adding more inverters to the chain increases the total circuit delay, reducing the oscillation frequency (f_{osc}). The propagation delay (τ_p) of the single inverter stage has a relationship with the circuit f_{osc} given by the following Equation^[96]:

$$f_{osc} = \frac{1}{T} = \frac{1}{2n\tau_p} \quad (5)$$

where n is the number of inverter stages and T is the total delay time in Figure 14d. It should be noted that in general the measured delay time depends on the shape of the input signal and on the load at the output of each inverter stage in a digital circuit. Typically, two main conditions have to be satisfied

to measure the exact circuit speed: (i) the inverter should only delay the signal without distorting it and (ii) the load at the output should be equal to the input impedance of the inverter. These conditions are well met by a ring oscillator and therefore this basic circuit is frequently used to measure the delay time of digital circuits.

The propagation delays of the complementary inverter (Figures 14a and 14b) for the high-to-low (τ_{pHL}) and low-to-high (τ_{pLH}) transitions can be derived using first-order linear RC-network analysis,^[95] as follows:

$$\tau_{pHL} \approx \ln(0.5) R_n C_L \approx 0.69 R_n C_L \quad (6)$$

$$\tau_{pLH} \approx \ln(0.5) R_p C_L \approx 0.69 R_p C_L \quad (7)$$

where R_n and R_p are the simplified equivalent ON-resistances of the n -type and p -type transistors, assumed, with a strong approximation, to operate in the linear regime. It should be noted that this analysis also assumes that the equivalent load capacitance (C_L) is identical for both the high-to-low and low-to-high transitions. The overall propagation delay (τ_p) of the inverter is defined as the average of the two values, that is:

$$\tau_p = \frac{\tau_{pHL} + \tau_{pLH}}{2} \approx 0.69 C_L \left(\frac{R_n + R_p}{2} \right) \quad (8)$$

From the above simplified equations it is possible to easily deduce ways to minimize the propagation delay of a gate:^[94] (i) by limiting the load capacitance C_L , which depends on the input capacitance of a similar gate, on the fan-out and on the interconnections capacitance, and (ii) by reducing the FET ON-resistance, which depends on the charge carriers mobility, on the geometrical factors W/L , on the specific capacitance (C_i) and on V_{DD} . Increasing μ is still a clear issue in printed electronics, along with the reduction of L , due to the resolution limitations of common printing techniques. A longer W induces a higher gate capacitance, so that this cannot be considered a parameter for boosting the logic speed, at least as long as the gate capacitance prevails on extrinsic contributions, such as capacitance of interconnections. V_{DD} should be limited to reduce power consumption, leaving to the increase of C_i the possibility to improve the currents at the same V_{DD} .^[94]

4.2. Organic Complementary Inverters and Ring Oscillators

Over the last few decades, a variety of organic inverters and ring oscillators have been reported. However, many of these works were carried out either by employing small molecular p - and n -type semiconductors deposited in high vacuum with a thermal evaporation process, or with a unipolar architecture, which shows strong limitations compared

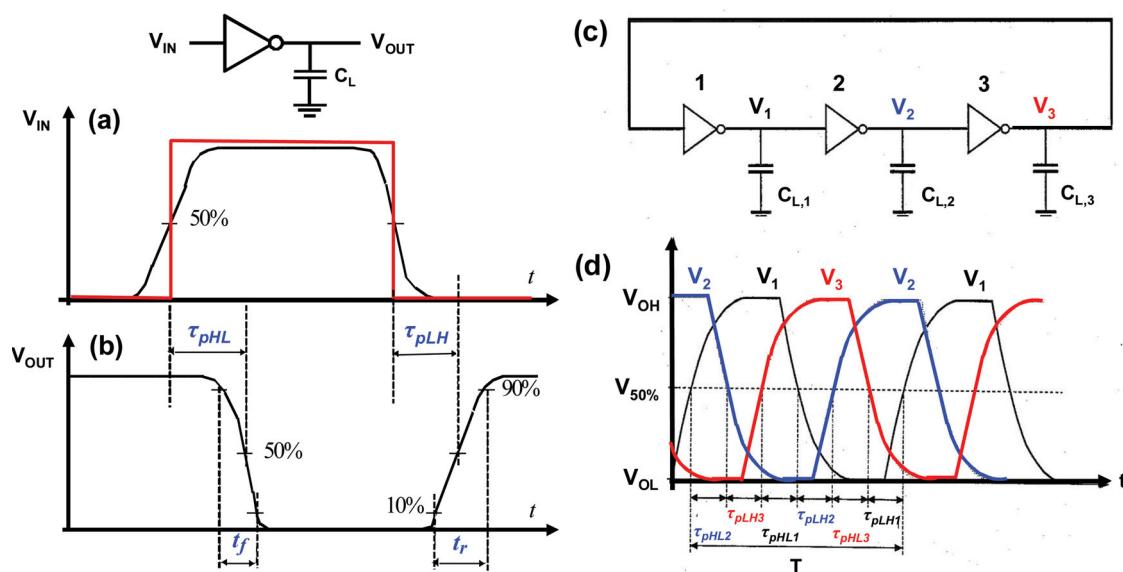


Figure 14. Circuit configuration of a complementary inverter and inverter dynamic characteristics of (b) V_{OUT} versus (a) V_{IN} , (c) circuit configuration of a multistage (here, 3-stage) ring oscillator, and (d) dynamic characteristics of the ring oscillators.

to complementary logic, as reported in the previous section. The organic ring oscillators fabricated using either vapour deposition or solution processes are listed in **Table 4** along with the corresponding circuit f_{osc} . The typical organic ICs showed relatively low f_{osc} that ranged from a few hundred Hz to a few hundred kHz. These relatively slow circuit speeds can be attributed to the low charge carrier mobility of the organic semiconductors, unipolar circuit architecture, long channel distance, and large parasitic capacitance due to the large overlap area between the gate and source/drain electrodes, as clarified in the next Section. Therefore, most importantly, both the electron and hole mobilities of the individual OFET devices have to be further increased and the IC architectures should also be optimized in order to realize high-speed printed circuitry needed for applications, such as printed RFID tags operating at 125–134 kHz or 13.56 MHz. Furthermore, such organic ICs should also be fabricated using printing techniques. A few pioneering studies on the development of complementary inverters were recently undertaken using printing methods, such as gravure and inkjet printing.^[68,100] Very recently, a few promising results with much higher operation speeds of more than a few MHz have been reported.^[101]

5. Strategies for High-Speed Complementary Circuits Using Polymer Semiconductors

The transition frequency (f_T) is the common figure of merit adopted to indicate the maximum operative frequency for a transistor and is defined as the frequency where the AC input-output current gain is reduced to unity.^[135] In the unrealistic case of a transistor with no overlap between the gate and the source/drain electrodes ($L_{ov} = 0$), f_T in the saturation regime can be expressed as:

$$f_T \approx \frac{1.5}{2\pi} \frac{\mu V_{od}}{L^2} \quad (9)$$

where $V_{od} = (V_g - V_{Th})$. In an ideal case therefore f_T should scale with L^{-2} . This scaling is not achieved in actual devices because of the presence of the parasitic overlap capacitance. If an equal gate-source and gate-drain overlap L_{ov} is taken into account, Equation (9) can be modified as follows:^[136]

$$f_T \approx \frac{\mu_{app} V_{od}}{2\pi L (L + 2L_{ov})} \quad (10)$$

where μ_{app} , the apparent device mobility, is also introduced to take into account the effect of extrinsic factors, such as the contact resistances (R_c), in reducing the effective device mobility with respect to the intrinsic charges mobility in the semiconductor. The latter expression allows to immediately point out the main parameters affecting the operation speed of a device. The development of solution-processable semiconductors with higher *p*- and *n*-type mobility directly results in an improved f_T , as this scale with μ_{app} . To boost the switching speed achievable with a given semiconductor, advanced printing processes capable of high lateral resolution should be developed to reduce L , in parallel to suitable methods to reduce R_c effects that are more severe in down-scaled devices and can limit f_T .^[137] However, if no attention is paid in reducing L_{ov} and this is larger than L , f_T would tend to scale only as $\sim L^{-1}$. Therefore, suitable technique to limit L_{ov} should be implemented as well. On top of these requirements, in order to reduce the operating voltages of logic circuits, suitable high-capacitance gate dielectrics should be adopted.^[94,100,138]

Although the performance of state-of-the-art printed organic electronic devices and circuits is still limited by their operational speeds far below a few MHz,^[79,101,113,116,125,132,139] there has been remarkable progress in the last decade. In

Table 4. Representative results for the organic ring oscillators.

Process	Device Configuration (S/D, Dielectrics, thickness)	Semiconductors		L [μm]	V _{DD} [V]	μ _{FET} [cm ² /Vs]	f _{osc} [Hz]	Ref	
		P-Type	N-Type						
Vapour Deposit	BG/BC, P-only (Au/Cr, Ta ₂ O ₅ , 200 nm)	Pentacene	-	9	-5	μ _h = ~ 0.06	2.9k	[102]	
	BG/BC, P-only (Au/Cr, cPVP, 450 nm)	Pentacene	-	5	20	μ _h = ~ 0.6	3k	[103]	
	BG/TC, P-only (Au, P _x MS/SiO ₂ , 100 nm)	Pentacene	-	10	-22	μ _h = ~ 1.35	31.4k	[104]	
	BG/BC, P-only (Au, Al ₂ O ₃ /P-Acid SAM)	Pentacene	-	10	-5	μ _h = ~ 0.4	5k	[105]	
	BG/TC, P-only (Au, Polymer/Al ₂ O ₃)	Pentacene	-	20	-73	μ _h = ~ 1.5	100	[106]	
	BG/BC, P-only (Au, cPVP, 270 nm)	Pentacene	-	5	-50	μ _h = ~ 0.3	6.7k	[107]	
	BG/BC, P-only (Au, cPVP, 230 nm)	Pentacene	-	5	-45	μ _h = ~ 0.06	6k	[108]	
	BG/BC, P-only (Au, cPVP, 270 nm)	Pentacene	-	5	-50	μ _h = ~ 0.2	4.5k	[109]	
	BG/BC, P-only (Au, cPVP, 270 nm)	Dec-2TP2T-Dec	-	20	~ -50	μ _h = ~ 0.3	667	[110]	
	BG/TC, N-only (LiF/Al, BCB or PVP)	-	C ₆₀	2.5	80	μ _e = ~ 6.0	30.5k	[111]	
	BG/BC, CMOS (Au, cPVP, 50 nm)	Pentacene	F ₁₆ CuPC	2	40	μ _h = ~ 0.1	12.5k	[112]	
						μ _e = ~ 0.002			
	BG/BC, CMOS (Au, Al ₂ O ₃ /P-Acid SAM, 3.6/2.1 nm)	Pentacene	F ₁₆ CuPC	20	3.5	μ _h = ~ 0.41	100	[113]	
						μ _e = ~ 0.02			
Spin-Coating	BG/BC, CMOS (LiF/Al & Au, SiO ₂ /TiSiO ₂ /SiO ₂ , 152 nm)	Pentacene	C ₆₀	50	10	μ _h = ~ 0.44	80	[114]	
						μ _e = ~ 0.61			
	BG/BC, CMOS (Au/Ti, SiO ₂ , 100 nm)	Pentacene	PDI-8CN ₂	7.5	100	μ _e = ~ 0.14	34k	[115]	
	BG/BC, CMOS (Au/Ni)	α-6T	F ₁₆ CuPC	7.5	80	μ _h = ~ 0.01	10k	[116]	
						μ _e = ~ 0.01			
	BG/BC CMOS, (Au/Ni, SiO ₂ , 68 nm)	Pentacene	C ₆₀	1000/2	25	μ _h = ~ 1.1	200k	[117]	
						μ _e = ~ 0.73			
	BG/TC P-only (Pseudo-CMOS), (Au, Al ₂ O ₃ /P-Acid SAM, 4/2 nm)	DNTT			7/7	2		4.27k	[118]
	BG/BC, P-only (Au/Pt, cPVP, 300 nm)	diF-TESADT: PTAA	-	1.5	-120	μ _h = ~ 0.1	100k	[119]	
	BG/BC, P-only (Au/Ni, SiO ₂)	diF-TESADT	-	2	-80	μ _h = 0.1 – 0.2	22k	[120]	
	BG/BC, P-only (Au/Ni, SiO ₂)	Tips-Pentacene	-	2	-80	μ _h = 1.2	10.2k	[121]	
	BG/BC, P-only (PANI, SC100, 300 nm)	P3HT	-	1	5	μ _h = 0.003	2k	[122]	
TG/BC	BG/BC, N-only (Au, cPVP, 300 nm)	-	F-C ₆₀ derivative	1.5	150	μ _e = 0.15	10.4k	[123]	
	TG/BC, P-only (Au, Copolymer Blend, 200 nm)	F8T2	-	2	-25	μ _h = 0.015	10.4k	[124]	
	TG/BC, P-only (Au, Copolymer Blend, 250 nm)	P3HT	-	2	-80	μ _h = 0.02	106k	[125]	
	TG/BC, P-only, Polyelectrolyte (Au/Cr, P(VPA-AA), 70 nm)	P(T ₀ T ₀ TT ₁₆)	-	2.5	1.5	μ _h = ~ 0.02	250	[126]	
	TG/BC, P-only, Polyelectrolyte (PEDOT, low-k/high-k polymer)	F8T2	-	100	-80	μ _h = ~ 0.0013	3.9	[127]	
	TG/BC, CMOS (Au, Polymeric Blend, 300 nm)	P3HT	PDI-8CN ₂	~ 5	-12	μ _h = ~ 0.01	75	[128]	
						μ _e = ~ 0.001			
	TG/BC, CMOS, Polyelectrolyte, (Au, P(VPA-AA), P(VP-EDMAEMAES))	P(T ₀ T ₀ TT ₁₆)	P(NDI2OD-T2)	2 ~ 3	1.5	μ _h = ~ 0.03	0.5ms at 7stages	[129]	
						μ _e = ~ 0.007			
	BG/BC, Ambipolar (Au/Ti, SiO ₂ , 206 nm)	PDPP3T		5	130	μ _h = ~ 0.02	42k	[130]	
						μ _e = ~ 0.02			
TG/BC	TG/BC, Ambipolar (Au/Ni & Cs/Au/Ni, PMMA, 520 nm)	PTVPhi-Eh		20	160	μ _h = ~ 0.54	12k	[79]	
						μ _e = ~ 0.26			
BG/BC	BG/BC, N-only (Ag ink, PAN/PMSQ/OTS)	NDI2OD-DTYM2		30		μ _e = ~ 1.2	1.2k	[131]	

Continued

Table 4 Continued.

Process	Device Configuration (S/D, Dielectrics, thickness)	Semiconductors	L [μm]	V _{DD} [V]	μ _{FET} [cm ² /Vs]	f _{osc} [Hz]	Ref	
	TG/BC, Ambipolar (Au, PMMA 70nm, Self-aligned gate)	PSeDPPBT	5	50	μ _h = ~ 0.6 μ _e = ~ 1.1	182k	[74]	
	TG/BC, Ambipolar inverters (Au, P(VDF-TrFE))	P(NDI2OD-T2)	5	-35	μ _h = ~ 0.1 μ _e = ~ 0.1	3.5k	[80]	
Inkjet	TG/BC, CMOS (Au, PMMA 500nm)	P2100	P(NDI2OD-T2)	10	-100	μ _h = ~ 0.5 μ _e = ~ 0.2	50k	[100]
	BG/BC, CMOS (Au, Al ₂ O ₃)	Tips-Pentacene		N3300	5	20	μ _h = ~ 0.53 μ _e = ~ 0.25	[8]
Gravure	TG/BC, p-only (PEDOT:PSS,low-k/high-k)	F8T2	100	-40	μ _h = 0.0013	3.9	[127]	
Doctor-Blade	TG/BC, P-only (PANI or, PEDOT, PMMA or PVP, 1 μm)	P3HT	-	50	-90	μ _h = ~ 0.006	0.85	[132]
Solution-Casting	BG/BC, P-only (Au, cPVP, 350 nm)	Rubrene-based	-	4	-20	μ _h = 0.1–0.7	2 k	[133]
Micro-injector	BG/BC, N-only (Au/Ti, SiO ₂ , 100 nm)	-	PDI-8CN ₂	3.2	100	μ _e = 0.024	3.2 k	[134]

this section, we introduce the recent progress, mostly based on polymer semiconductors, and some of the most effective strategies reported in the literature for developing high-speed printed electronic devices and ICs by addressing one by one the critical points reported before, and summarized in **Figure 15**.

5.1. Development of High-Mobility, Printable Semiconductors

As described in **Section 2**, in the last 30 years the charge carrier mobilities of polymer semiconductors have been greatly improved from $\sim 10^{-5}$ to ~ 10 cm²/Vs. These remarkable improvements have been achieved mostly through a better understanding of the charge carrier transport mechanism in π -conjugated organic molecules, although well-designed synthetic strategies and optimization of the device fabrication process have also contributed. There have been various reports on the development of complementary electronic circuits based on the new high-mobility *p*-type and *n*-type polymer semiconductors. The π -conjugated polymer semiconductors are mainly described in **Section 2**, and their operating speeds are summarized in Table 4. In fact, there has been a remarkable increase in the f_{osc} of such devices from a few Hz to a few hundreds of kHz. Baeg et al. reported high-speed-operating (~50 kHz), all-polymeric complementary circuits based on *p*-type (Polyera ActivInk™ P2100) and *n*-type P(NDI2OD-T2) polymer semiconductors.^[100] The inkjet-printed P2100 and P(NDI2OD-T2) OFETs showed equivalent and high hole and electron mobilities of 0.2–0.5 cm²/Vs, which were mainly enabled by the optimization of the inkjet-printed active features, the small R_c of both electron and hole injection from the Au bottom electrodes, and effective control over the gate dielectrics and the orthogonal solvent effect.^[100]

We think it is worth opening a parenthesis at this point, to discuss different approaches for the development of high-mobility printable semiconductors, because, although the charge carrier mobilities of organic semiconductors have been

significantly improved, these are still quite limited compared to inorganic semiconductors. As an alternative and with the goal to enhance the overall performance of printed device, other kinds of printable active materials have been developed and tested, including carbon nanomaterials (single-walled carbon nanotubes^[143,144] and nanoribbon graphene^[145]), amorphous oxide semiconductors,^[146–148] and printable silicon.^[149] All these materials have much higher charge carrier mobilities than those of organic semiconductors, from a few tens of cm²/Vs with amorphous oxide semiconductors, to ~ 100 cm²/Vs for transistors employing printed graphene inks,^[150] to ~ 1000 cm²/Vs for chemical vapour deposition grown graphene transistors (with a theoretical maximum value of $\sim 10^6$ cm²/Vs).^[151] Thus, a tremendous amount of research has focused on developing the new-generation of printable active materials and their applications. However, there also remain many hurdles to be overcome before this technology is adapted to commercialized products, especially the sorting of semiconducting and metallic carbon nanotubes, the low ON/OFF current ratio attributed to the zero-bandgap properties of graphene, the rare *p*-channel properties and the bias instabilities of the oxide semiconductors. Compared to these counterparts, the polymer semiconductors have many combinational advantages in addition to their moderately high and balanced hole and electron mobilities, such as mechanical flexibility (even stretchability), easy processing with R2R printing methods for high-throughput mass production at low temperatures (even at room temperature), and stability under ambient conditions and air. Notably, the mobility of ~ 10 cm²/Vs recently achieved by using a high-molecular-weight *p*-type polymer semiconductor is quite impressive and was unimaginable a decade ago. This is for example a high enough value to allow the adoption of polymer OFETs as driver transistors in active matrix OLED displays, printed RFID tags operating at 13.56 MHz for item-level tagging, and many flexible and stretchable electronic devices, such as sensors and memory.

From the point of view of the active material, it can therefore be said that if printable semiconductors with high enough

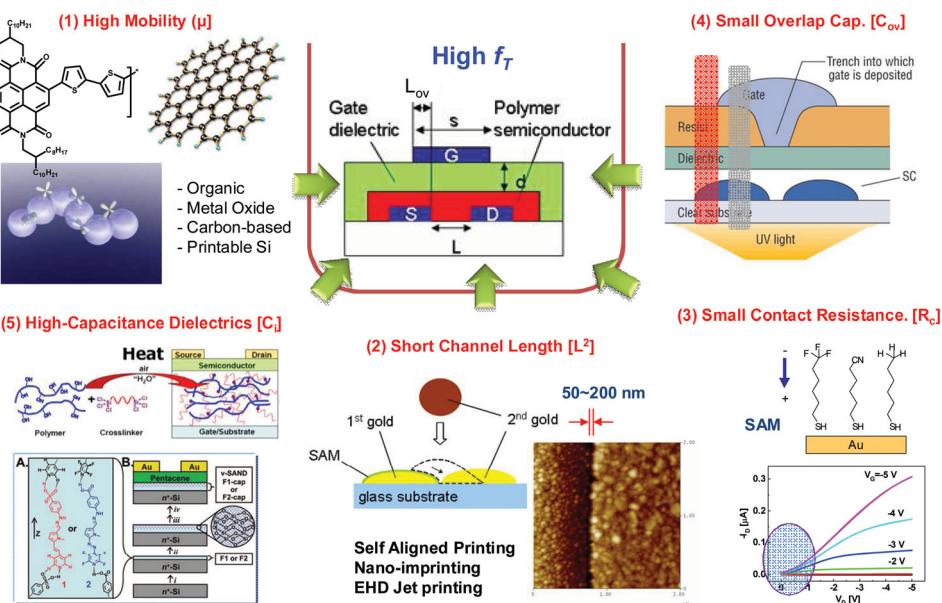


Figure 15. Strategies for developing high-performance organic electronic circuits via (1) high charge carrier mobility active channel materials, (2) short channel length S/D electrodes, (3) reduced contact resistance for charge carrier injection, (4) small parasitic overlap capacitance, and (5) high capacitance gate dielectrics for low voltage operation. Reproduced with permission from Refs. [140-142]. Copyright,

mobilities have only recently appeared, the increasing trend showed by polymer semiconductor performances and the parallel development of alternative technologies based on other solution-processable carbon nanomaterials and inorganic semiconductors allow us to foresee in the short-term a scenario where more and more applications fall within the reach of printed electronics and different technologies are made available to satisfy specific needs in terms of overall performances, process integration, costs, stability or mechanical properties.

5.2. Downscaling of Channel Length

The channel length (L) is a critical feature for obtaining high-speed printed ICs. However, it is quite challenging to obtain channels with micron size or even submicron lengths using the well-developed, standard GAP methods, because the printed feature sizes are typically very large, frequently more than a few tens of micrometres. There have been several approaches to realize printed organic transistors with active channels of submicron lengths. Sirringhaus et al. demonstrated submicron channels of 50–200 nm in size produced using self-aligned printing (SAP) methods (see Figure 16d).^[152,153] Very small gaps between electrodes were obtained by controlling the receding contact-line motion of the liquid conductive ink (either metal nanoparticles or PEDOT:PSS conducting polymers) droplets. These droplets were repelled by and flowed off of the surface of a previously deposited electrode, which was treated with a self-assembled monolayer or surfactant for the purpose of modifying the surface wettability with the subsequently dropped inks.^[152] Using the SAP technique, the same group developed inkjet-printed polymer transistors and circuits with sub-micrometer channel lengths. These submicron inkjet-printed

inverters can be switched at a frequency of up to 40 kHz (p -only inverter with PEDOT:PSS resistor load and F8T2 polymer semiconductor)^[152] and further enhanced up to ~1.6 MHz when combined with a self-aligned gate (SAG) electrode and the high-mobility (~0.6 cm²/Vs) polymer semiconductor, PBT_{TTT}.^[142]

Although Sirringhaus et al. used a conventional inkjet-printing method combined with a unique surface modification technique to produce short-channel-length electrodes, there are large challenges involved in using the conventional inkjet printing system for nanotechnology. The minimum volume of an inkjet droplet for a state-of-the-art inkjet print head is around 10 pL. This volume forms a sphere of approximately 13 μm in diameter, which limits the minimum available inkjet-printed feature size to ~15–20 μm in the very best case. Alternatively, Murata et al. and Rogers et al. modified conventional inkjet printing techniques to demonstrate superfine inkjet printing^[154] and EHD jetting,^[92] respectively (see Figures 16a and 16c). The superfine inkjet system allowed the arrangement of dots with minimum sizes of less than 1 μm, and several applications were demonstrated, such as direct printing of ultrafine silver nanopaste wiring of a few micrometres in width on a glass plate, the site-selective growth of carbon nanotubes using a catalyst, and organic transistors.^[154] The EHD jet printing technique uses electric fields, rather than the thermal or acoustic energy used in conventional inkjet heads, to overcome capillary forces in a small diameter nozzle and create the fluid flows necessary for delivering tiny volume of inks on a substrate. This was first adopted for modest-resolution applications (dot diameters ≥20 μm using nozzle diameters ≥50 μm) in GAPs.^[92,155] On the other hand, Rogers et al. successfully demonstrated the jet printing of complex patterns of inks ranging from insulating and conducting polymers, to solution suspensions of silicon nanoparticles and rods, to single-walled

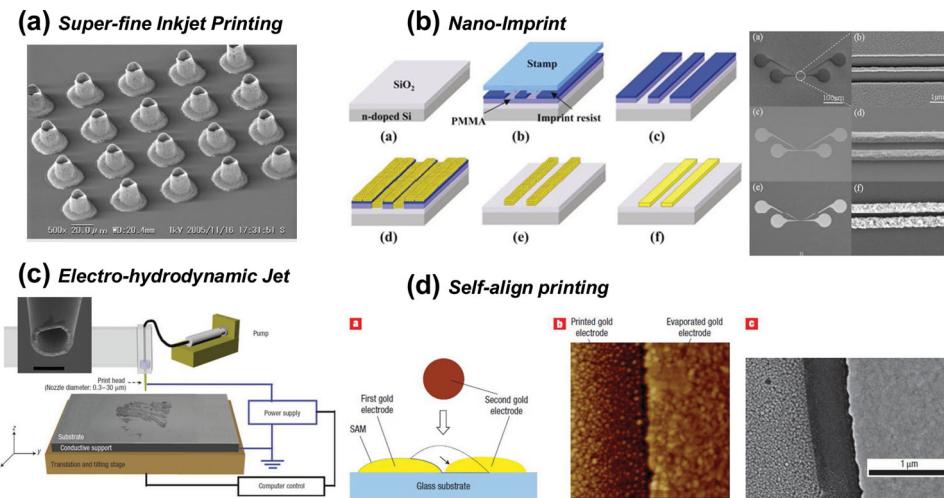


Figure 16. Submicron channel fabrication using printing processes; (a) super-fine inkjet printing,^[154] (b) NIL,^[156] (c) EHD jetting,^[92] and (d) self-aligned inkjet printing.^[142] Reproduced with permission from denoted references.

carbon nanotubes. They produced functional devices with submicron resolution by controlling the fluid flow using fine microcapillary nozzles.^[92]

NIL is also a very promising method for high-throughput and high-resolution nanometre-scale patterning. A few reports in literature deal with the fabrication of nanoscale organic transistors based on NIL; in particular, a combination of lamination, nano-transfer printing, and hot embossing (HE) was used.^[157] HE is the best established technique to achieve nanometric imprinting and has already proven to be useful for defining submicron channel lengths in OFETs.^[158–161] Recently, R2R NIL technology has been developed to enable continuous printing of nanostructures (polymer patterns with 70 nm feature sizes) on a flexible web with drastically increased throughput.^[93,162] Furthermore, the reverse nanoimprinting^[163] or nano-transfer-printing methods^[164] produce positive-tone polymer or metal patterns that can also be applied to R2R printing processes. Jung et al. produced short-channel OFETs using the P3HT polymer semiconductor and solution-processed metal nanoparticle ink (Au).^[156] The ink was spin-coated onto NIL-processed patterns and thermally cured to form an Au S/D electrode, as can be seen in Figure 16b.^[157,162] Through a combination of the R2R process and solution-processed conductive inks, NIL can, in principle, be a promising methodology for fabricating electrodes with short channel lengths for high-speed printed organic electronic devices and ICs.

NIL using solution-deposited nanoparticles (NPs) could achieve submicrometer resolution patterning of metal electrodes but still needs a master mold fabricated by conventional electron-beam lithography.^[165] Recently, laser machining with a continuous wave or femtosecond laser has been proposed as a complementary method to be combined with different printing techniques,^[166,167] in order to improve the patterning capabilities through controlled laser ablation or sintering of conductive metal NPs inks.^[165] Notably, a femtosecond laser enables the fabrication of nanoscale metallic patterns from solution-deposited metal NPs, in which high resolution is

achieved due to the very short pulse of the femtosecond laser overcoming light diffraction limit of the continuous wave laser.^[165]

5.3. Reducing Contact Resistance

When the channel length (L) of the OFETs is reduced to the submicron scale, R_c should be seriously taken into account as an important issue, because in polymer transistors it tends to become comparable, or higher, than the channel resistance (R_{ch}), thus causing the apparent device mobility μ_{app} to drop significantly below the intrinsic mobility (μ_o).^[101,168–170] μ_{app} in the saturation region can be expressed by the following Equation:^[168,169]

$$\mu_{app} \approx \mu_o \left[1 - \left(\frac{\mu_o C_i W R_c (V_g - V_{Th})}{L + \mu_o C_g W R_c (V_g - V_{Th})} \right)^2 \right] \quad (11)$$

This is one of the main reasons why most organic transistors with short channel lengths (< 1 or 2 μm) have much lower μ_{app} and f_T values, typically well below 1 MHz, than expected without taking R_c into account. For example, theoretically, f_T values of 10 MHz and 100 MHz should be achievable at voltages of 3 V and 30 V, respectively, when a transistor device has an intrinsic field-effect mobility of 1 cm^2/Vs and lateral dimensions (L and L_{ov}) of 1 μm .^[101] However these performances have not been demonstrated yet in the literature.

Recent literature data on the R_c values of OFETs with more standard device configurations are shown in Figure 17a, where the W -normalized R_c values are plotted against the charge carrier mobility (μ).^[171] When the degree of downscaling for OFETs and circuits is increased, the shortest channel length (L_{MIN}), the distance where $R_{ch} = R_c$, should also be properly taken into account. As can be seen in Figure 17b, Natali et al. verified that the R_c should be smaller than 1 $\text{k}\Omega\cdot\text{cm}$ or

100 $\Omega\text{-cm}$ for correct downscaling of the channel length below 10 μm when μ is in the range of 0.1 to 1 cm^2/Vs or in excess of 1 cm^2/Vs , respectively.^[171] Currently, most of the published short-channel OFETs, though showing typical field-effect behaviour, are contacts limited. There have been a number of reported approaches to reduce R_c , including energy level matching by varying the metal electrodes,^[172–174] control of the interfacial dipoles using thiol-based self-assembled monolayers (SAMs),^[142,175,176] incorporation of charge injection interlayers,^[79,177–179] and the use of polymer and other carbon nano-material-based electrodes.^[180–182] The fundamental contact electrode interface physics and chemistry and recent approaches to obtaining optimized charge injection states can be found in a few review articles.^[171,183–185]

5.4. Reducing Parasitic Overlap Capacitance

When the transistor is downscaled and highly integrated for complex printed circuitry, the parasitic capacitances mainly due to the overlap L_{ov} between the gate and source/drain electrodes become a critical issue, strongly limiting f_T (Equation 10). Notably, most GAP tools for state-of-the-art printed electronics applications have relatively large feature sizes of more than a few tens of μm , which typically provide large overlap areas. Therefore, proper approaches have to be introduced in the fabrication of printed OFETs in order to minimize this parasitic capacitance and to achieve the highest possible operation frequency for the printed transistors and their ICs.^[101,142,186]

Noh et al. significantly reduced the parasitic overlap capacitance down to values as low as 0.2–0.6 pF/mm by using a self-aligned gate (SAG) technique (see Figure 18a). The SAG structure was fabricated by (i) deposition of a photoresist as a second dielectric on top of the semiconductor and gate dielectric, (ii) UV illumination from the back of the substrate through the channel area, (iii) development of the second dielectric to remove the exposed region, and (iv) deposition of the gate electrode.^[142] As shown in Figure 18b, the overlap capacitances between a printed PEDOT:PSS gate and photo lithographically defined or inkjet-printed Au source/drain electrodes were measured to be 0.1–0.3 pF/mm or 0.6–0.8 pF/mm, respectively, which were at least a factor of 5–10 lower than those of reference devices without the SAG structure.^[142] This SAG structure was successfully used to achieve the f_T of ~1.6 MHz when combined with self-aligned inkjet printing for defining submicron channels, a high-mobility PBTETT polymer semiconductor, and cross-linked thin polymer gate dielectrics for low-voltage operation.^[142]

Importantly, for staggered organic transistors, it is noted that L_{ov} should be optimized both to reduce R_c and to reduce the parasitic overlap capacitance (C_{ov}). In fact, compared to coplanar OFET devices, where effective charge injection at the semiconductor-contact interface is limited to the narrow region mostly at the contact edge near the active channel, staggered OFET devices have much larger charge injection areas because the source/drain electrode is located opposite to the semiconductor, so that the channel can extend beyond the contact edge over overlap length (L_{ov}) with the gate (see inset in Figure 19b).^[101] This large charge injection area generally leads to smaller R_c .

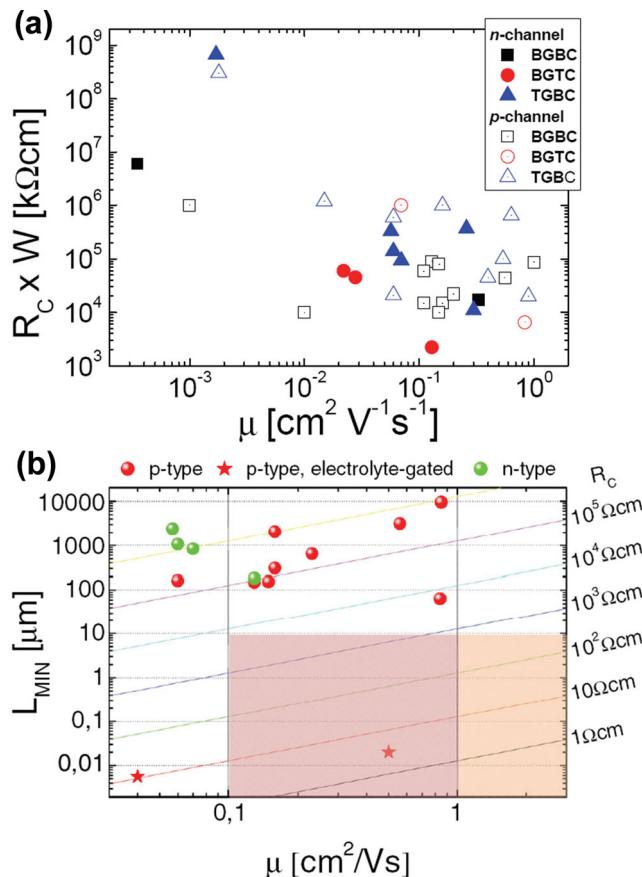


Figure 17. (a) Width-normalized R_c values in OFETs with solution-processed semiconductors, plotted versus the device mobility, as obtained from a survey of the scientific literature published in the last 12 years. (b) Plot of the channel length L_{MIN} for which the current is half that which would flow in case of Ohmic contacts, calculated for various R_c values (given on the right). L_{MIN} is calculated using data from the survey, as well, for a p-type standard OFET (red circles), p-type electrolyte-gated OFET (red stars), and n-type standard OFET (green circles). Only survey data in the linear regime were considered. For the calculation of R_{ch} , a carrier density of $8 \times 10^{12} \text{ cm}^{-2}$ was assumed. For L_{MIN} to go below 10 μm when μ is in the range 0.1–1 cm^2/Vs , R_c should be no larger than $10^{-1} \text{ k}\Omega\text{-cm}$ (pale pink shaded area). Mobilities larger than 1 cm^2/Vs will require R_c to be at least below 100 $\Omega\text{-cm}$ (pale orange shaded area). In panel (a) OFET device architectures are indicated by the following acronyms: Bottom-gate/bottom-contacts (BGBC), bottom-gate/top-contacts (BGTC) and top-gate/bottom-contacts (TGBC). Reproduced with permission from Ref. [171]. Copyright 2012, John Wiley & Sons, Inc.

Unfortunately the two requirements on low R_c and low C_{ov} are in obvious competition and a trade-off should be found to compromise these two opposite constraints. Notably, the W -normalized R_c is related to L_{ov} as follows:

$$R_c W = 2 R_{sheet} L_T \coth \left(\frac{L_{ov} + L_{ext}}{L_T} \right) \quad (12)$$

where L_{ext} is the extended contact length, namely a further contribution to the charge injection in a non-perpendicular direction between the source contact and the gate due to the electrostatic potential distribution in the organic semiconductor layer,

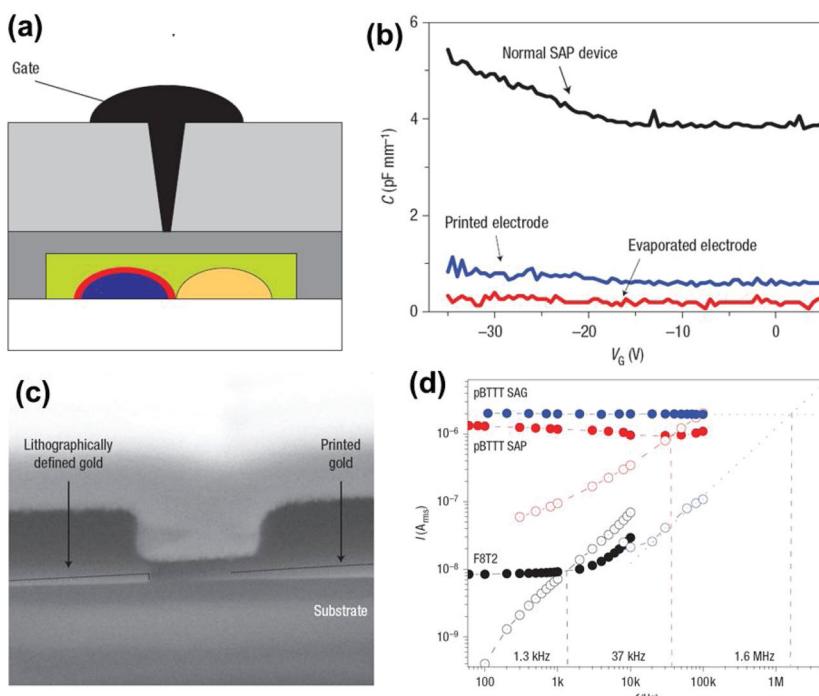


Figure 18. (a) Self-aligned gate (SAG) architecture. (b) Cross-sectional view of the SAG structure measured using FIB-SEM. (c) Capacitance-voltage characteristics of an F8T2/cPMMA FET with self-aligned printed S/D electrodes and unconfined PEDOT:PSS TG electrodes (black line). (d) Fully downscaled SAG PBTTT transistor and switching speed. Reproduced with permission from Ref.[142]. Copyright 2007, Nature publishing group.

L_T is the transfer length, the characteristic length over which 63% of the charge carrier exchange between the contacts and the semiconductor occurs, and R_{sheet} is the sheet resistance of the semiconductor layer.^[101] For typical organic semiconductors with $\mu_{\text{app}} \approx 1 \text{ cm}^2/\text{Vs}$ and $R_c \approx 0.6 \text{ k}\Omega\text{-cm}$, L_T is measured to be around 10 μm .^[187] Thus, the R_c increases significantly as L_{ov} is decreased below $L_T \sim 10 \mu\text{m}$, which decreases the apparent mobility of the OFETs, as can be seen in Figure 19. By considering the R_c and L_{ext} , Klauk et al. verified that the f_T reaches

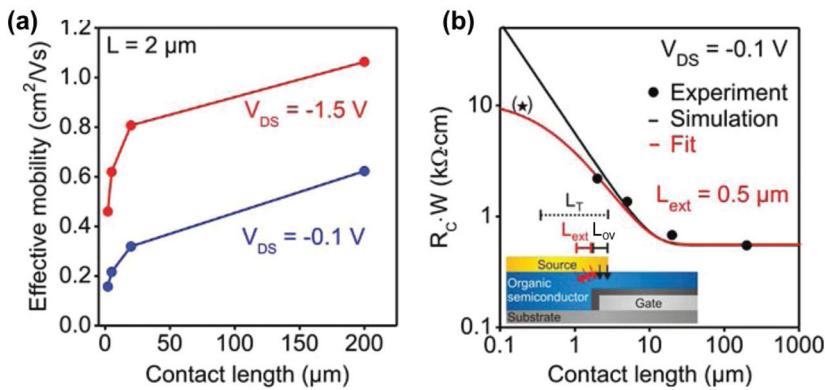


Figure 19. (a) Effective mobilities (apparent mobility in this review paper) of DNTT TFTs with a channel length of 2 μm as a function of the contact length in the saturation region (red curve) and in the linear region (blue curve). (b) Width-normalized R_c as a function of the contact length. Reproduced with permission from Ref. [101]. Copyright 2012, John Wiley & Sons, Inc.

a plateau for a $L_{\text{ov}} \approx L_T$ and then remains approximately constant when L_{ov} is reduced further.^[101] This result reveals that achieving a high f_T in staggered OFETs may not necessarily require a minimization of L_{ov} ; instead, the maximum f_T in most practical OFETs (assuming that $\mu_{\text{app}} \approx 1 \text{ cm}^2/\text{Vs}$ and $R_c \approx 0.6 \text{ k}\Omega\text{-cm}$) would be limited to slightly above 1 MHz because of the L_T value.^[101] This provides useful insight into the development of high-speed printed organic electronic circuits. The L_T of the organic semiconductors (including polymers) must be reduced either by developing new semiconductor materials with short L_T values, by using electrodes with excellent charge injection, or by performing selective-contact-area doping in staggered OFETs.^[188]

5.5. High Dielectric Capacitance

The selection and processing of the gate dielectric is very important for achieving high-performance OFET devices and ICs. Because most charge carrier transport in OFETs occurs within a few molecular layers from the semiconductor-dielectric interface, gate dielectrics must form a high-quality interface with the semiconductor (a low interface roughness with low interfacial and/or bulk

trap density). Notably, as can be seen in Table 4, most high-speed printed organic electronic devices and circuits operate under relatively high bias conditions. The operating voltage has to be reduced to at least the 5–10 V range for practical applications of printed circuitry, e.g. printed RFID tags,^[189] and the operating frequency (f_{osc}) must also remain high for fast data processing, and this can be achieved only by a stronger capacitive coupling between the gate contact and the channel region. Moreover, the correct scaling of the gate dielectric capacitance is vital for the operation of downscaled devices and therefore we want here to review different approaches adopted to realize this. The dielectric capacitance per unit area C_i is expressed as:

$$C_i = \frac{\epsilon_0 k}{d} \quad (13)$$

where ϵ_0 is permittivity of vacuum, k the permittivity of dielectric, and d the dielectric layer thickness. C_i can therefore be increased either by using high- k dielectric materials or by decreasing d .^[190] Traditionally, there has been controversy over whether high- k dielectrics are suitable for organic transistors. Veres et al. reported on OFETs based on amorphous polymer semiconductors, such as PTAA derivatives, which showed optimal field-effect mobilities of up to $6 \times 10^{-3} \text{ cm}^2/\text{Vs}$, small V_{Th} ,

and good device stability when an apolar low- k polymer dielectric was used, while showing strongly degraded performance with higher k dielectrics.^[191,192] This result is attributed to an energetic disorder induced on the localized transport states at the semiconductor-dielectric interface due to disordered polar groups in high- k dielectrics.^[191] However, it was also found that these energetic disorder effects are not a concern for some highly ordered polymeric semiconductors, likely due to an effective screening provided by the ordered, apolar solubilising alkyl chains sticking out of the polymeric backbone.^[193]

As shown in Figure 20, there have been a variety of approaches to increase C_i , such as the use of relaxor high- k polymer dielectrics,^[194] high- k polymer dielectric blends,^[195–197] cross-linked thin gate dielectrics,^[140,198,199] self-assembled monolayers (SAMs)^[113] or self-assembled nano-dielectrics (SANDs),^[198,200] organic-inorganic hybrid dielectrics,^[201] and ion-gels or electrolyte gates.^[139,194,202–206] Recent advances in the development of high-capacitance dielectrics can be found in comprehensive reviews by Facchetti et al.^[190,207] All these approaches, i.e. SAMs, SANDs, ion-gels, solution-processed oxide dielectrics, and organic-inorganic hybrid dielectrics, have been used successfully for OFETs operating at low voltages, even below 1 V. However, they are still not completely suitable for printed and/or flexible organic electronics devices and circuits because of their low throughput and their requirement of very flat surfaces in the case of SAMs and SANDs, their high processing temperatures above >300 °C that are

mostly incompatible with plastic substrates in the case of solution-processed oxides, and their slow response times in the case of ion-gels.

Alternatively, easily processable high- k relaxor polymers and blend dielectrics (polymer-polymer or inorganic-polymer) could be promising candidates for printed and flexible organic electronics.^[194,202–206,208] Baeg et al. used poly(vinylidenefluoride-trifluoroethylene) P(VDF-TrFE) high- k polymer dielectric blends with an amorphous polymer, poly(methyl methacrylate) (PMMA), to demonstrate low-operation-voltage, relatively high-speed printed complementary electronic circuits based on *p*-type and *n*-type polymer semiconductors.^[195,196,209] The high- k polymer P(VDF-TrFE) shows ferroelectric memory behaviour (large bias hysteresis in the transfer plots) attributed to strong dipolar polarization in a crystalline β -phase of the polymer film. Therefore, the P(VDF-TrFE) was mixed with PMMA, an amorphous polymer, to reduce the amount of ferroelectric crystalline phase formed, thus avoiding hysteresis in the device while profiting from an overall increased k .^[197] Moreover, Baeg et al. demonstrated that the *p*-type and *n*-type OFET characteristics could be controlled by changing the blend ratios of the two dielectrics.^[195] In a complementary inverter, the *p*-channel transistor saturation current was appreciably increased when the P(VDF-TrFE) content relative to PMMA was increased in the blended dielectric, whereas the *n*-channel transistor saturation current was slightly decreased. For various *p*-type and *n*-type polymer semiconductors with different electron and

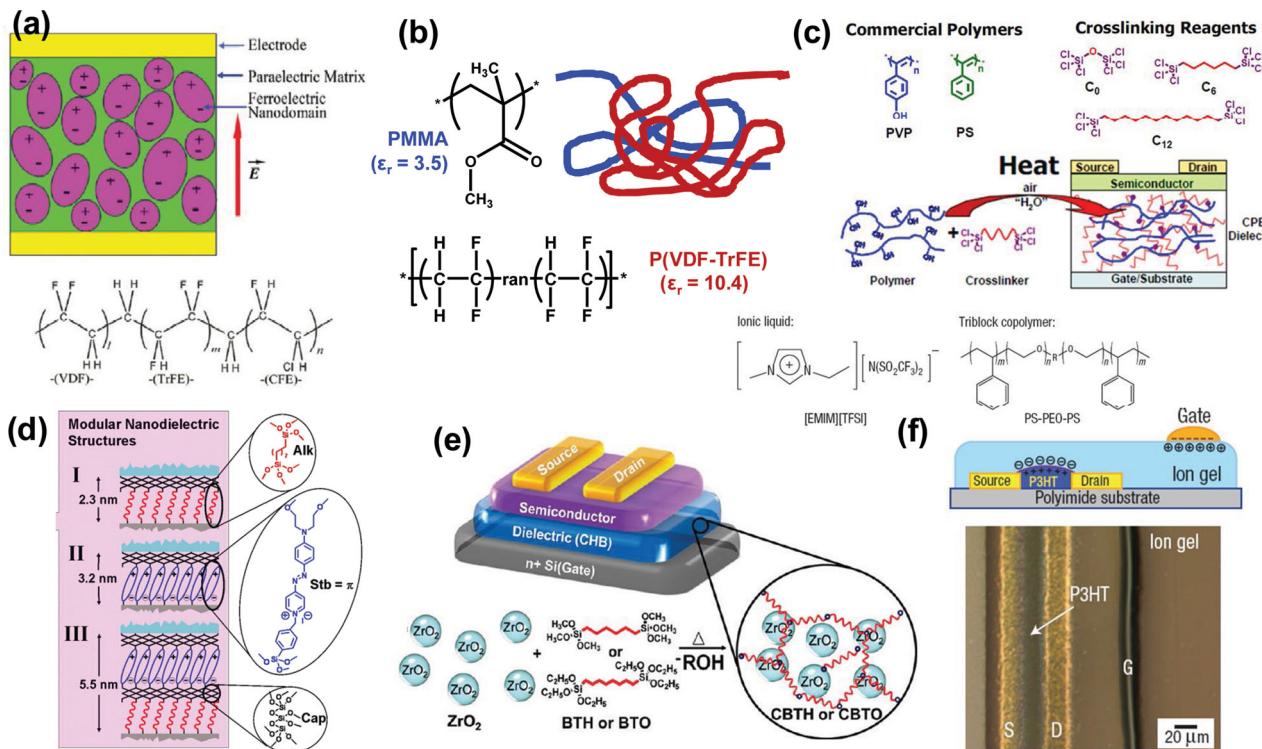


Figure 20. Various approaches to obtain high-capacitance gate dielectrics for low-voltage operating OFETs; (a) Relaxor high- k polymer dielectrics,^[194] (b) high- k polymer dielectric blends,^[195] (c) cross-linked thin gate dielectrics,^[140,199] (d) self-assembled nano-dielectrics,^[198] (e) organic-inorganic hybrid dielectrics,^[201] and (f) ion-gels and electrolyte gates.^[139] Reproduced with permission from denoted Refs.

hole mobilities and threshold voltages, these blend dielectrics with adjustable blend ratios provide a quite useful method for achieving equivalent *p*-channel and *n*-channel transistor properties in CMOS-like ambipolar circuits. Baeg et al. used the P(VDF-TrFE):PMMA blend dielectric with an optimum blend ratio of a 7:3 wt%. In combination with inkjet-printed *n*-type P(NDI2OD-T2) OFETs and both *p*-type polymer semiconductors containing alkyl-substituted thiénylenevinylene (TV) and dodecylthiophene (PC12TV12T) and ActivInk™ P2100 devices, this ratio led to large gains ($g_{inv} > 25$) and noise margins (75% of half V_{DD}) for inverters^[195] and to a high f_{osc} of ~80 kHz at $V_{DD} = 30$ V for a ring oscillator.^[209] In addition, various inkjet-printed flexible logic gates on a plastic substrate,^[196] including NAND, NOR, OR, and XOR gates, were obtained.^[196]

For R2R printed electronic devices, such as extremely low-cost printed RFID tags for item-level tagging, the printed features typically show surfaces with roughness of more than a few tens of nanometres because of rheological issues with ink or pastes.^[210] Therefore, the minimum dielectric layer thickness should be more than a few hundred nanometres to prevent electrical short-circuits and large leakage currents. Typically, most high- k polymer dielectrics such as P(VDF-TrFE) have dielectric constants of around 10. However, this value produces a specific capacitance of only ~20 nF/cm² for a 400 nm thick dielectric. Thus, a high- k polymer or its blend dielectric is not sufficient for decreasing the operation voltage of R2R printed electronic circuits, and does not fulfil the correct scaling required to drive a very short channel <1 μ m. To solve this, polymer electrolytes and ion-gels have been proposed as promising candidates for low-voltage applications regardless of the dielectric layer thickness. In a polymer electrolyte, mobile ions can migrate to the surface and screen electric fields in the bulk, so that the applied gate voltage is localized at the interface.^[211,212] Because of the formation of a nanometric electric double layer, an extremely high carrier density can be achieved by applying a relatively low voltage (even below 1 V), and a very large dielectric capacitance on the

order of 10 μ F/cm² is obtained, independently of the film thickness. However, the relatively slow switching frequency, which is mostly due to the small ion conductivities of the commonly used polymer electrolytes, must be addressed before these polymer electrolytes can be applied to printed electronic circuits. There have been successful approaches to increase f_{osc} either by using ion-gels (mixtures of an ionic liquid and a triblock copolymer)^[139] or by using polymers that consist of charged polymer chains and mobile counter ions.^[129,213] Cho et al. used an ion-gel dielectric to develop unipolar printable organic electronic circuits using a *p*-type polymer semiconductor. Owing to the relatively large conductivity of the ionic liquid, transistors based on ion-gels could be switched at a frequency as high as 10 kHz.^[139] As shown in Figure 21, Herlogsson et al. reported unipolar or complementary electrolyte-gated transistor circuits based on *p*-type polythiophenes and *n*-type P(NDI2OD-T2) polymer semiconductors. These circuits operated below 1 V and showed relatively fast propagation delay times down to 0.2–0.3 ms.^[126,129,214]

For practical applications in integrated printed electronic circuits, patterning of the gate dielectric is also required. This can be achieved either by direct printing onto the desired area or by removal from undesired areas and *via*-hole positions. Punching of the *via* holes should be easy and accurate in order to make ohmic interconnections between the upper and bottom electrodes.^[215]

6. Complementary Circuits Based on High-Mobility Ambipolar Polymers

In the construction of complementary printed electronic circuits, each *p*-type and *n*-type organic semiconductor region has to be patterned. While high-resolution photolithographic methods compatible with semiconductors have been demonstrated,^[216–218] direct printing methods, such as inkjet,^[100]

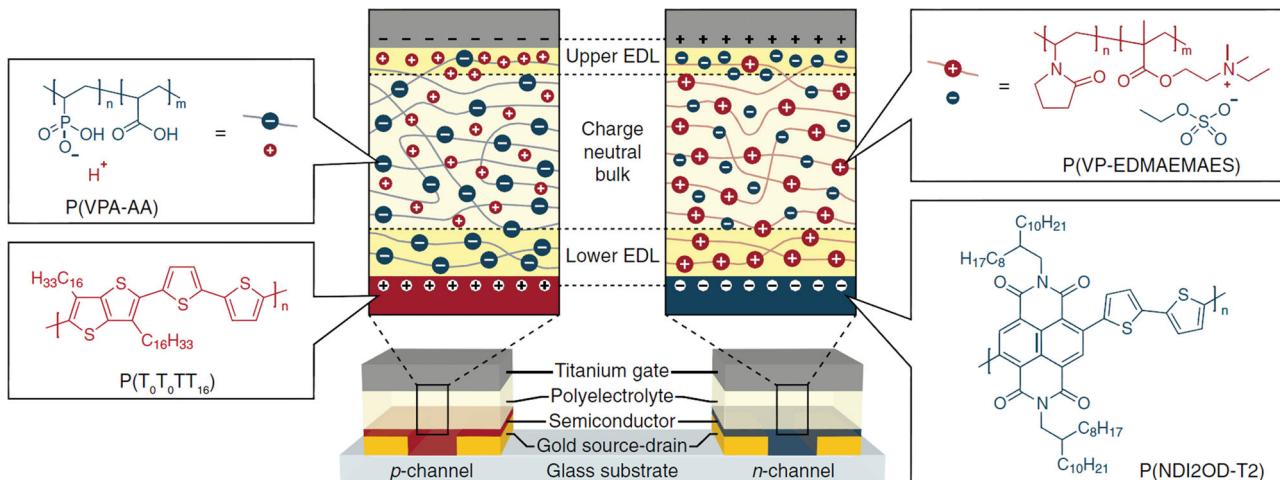


Figure 21. Material systems for complementary polyelectrolyte-gated transistors and schematic cross sections and illustrations of the charge distribution within the polyelectrolyte gate insulator layers in *p*- and *n*-channel transistors that are gated with negative and positive gate voltages, respectively. The chemical structures of the organic materials are also displayed. Reproduced with permission from Ref. [129]. Copyright 2011, John Wiley & Sons, Inc.

spray,^[219] and gravure^[68] printing, are clearly preferable in the context of cheap manufacturing of large area electronics. This poses a severe limitation on the patterning resolution, since, as previously discussed, state-of-the-art printing methods have limits in the feature sizes they can achieve and in their printing accuracy, usually not better than a few μm . As an alternative to the individual *p*-type and *n*-type organic semiconductors, also solution-processable ambipolar semiconductors have been investigated for their use in complementary organic ICs.^[220] An ambipolar film can typically consist of a single component (ambipolar semiconductors with equivalent hole and electron mobilities and V_{Th} values) or multiple components (blend or double-layer stack of *p*-type and *n*-type organic semiconductors). These ambipolar complementary circuits can be fabricated very easily using mass production printing processes, especially compared to complete complementary circuits based on both *p*-type and *n*-type semiconductors, since the ambipolar semiconductor active region can be deposited without any need for sophisticated and accurate patterning for both *p*- and *n*-type OFETs.^[75,221–223]

6.1. Operation of Ambipolar OFETs

The various operation regimes of the ambipolar OFETs are described in **Figure 22**. An ambipolar transistor can work in the usual driving scheme of a *p*-type (gate voltage $V_g < 0$ V and drain voltage $V_d < 0$ V) and *n*-type ($V_g > 0$ V and $V_d > 0$ V) OFET. In the case of balanced μ and V_{Th} , for the *n*-type driving scheme, electron transport is dominant for small positive V_d and positive V_g , and ambipolar transport of both electrons and holes is exhibited under high positive V_d and positive V_g

conditions.^[220,224] Similarly, for the *p*-type driving scheme, hole-only *p*-channel transport is dominant for small negative V_d and negative V_g , while ambipolar transport of both electrons and holes is exhibited for large negative V_d and negative V_g .^[220,224] As shown in **Figure 22**, the four operating regions of an ambipolar OFET driven in the usual scheme of an *n*-type transistor can be divided into an *n*-channel linear region (Equation 14), an *n*-channel saturation region (Equation 15), an ambipolar region (electrons and holes, Equation 16), and a *p*-channel saturation region (Equation 17),^[224] as follows. (i) For $V_d < (V_g - V_{\text{Th},n})$, the ambipolar transistor operates in the linear region, *n*-channel region:

$$I_d = \mu n C_i \frac{W}{L} \left(V_g - V_{\text{Th},n} - \frac{V_d}{2} \right) V_d \quad (14)$$

(ii) For $(V_g - V_{\text{Th},n}) \leq V_d \leq (V_g - V_{\text{Th},p})$, the electrons channel current of the transistor is saturated and I_d is given by

$$I_d = \mu n C_i \frac{W}{2L} (V_g - V_{\text{Th},n})^2 \quad (15)$$

(iii) For $V_d \geq (V_g - V_{\text{Th},p})$ and $(V_g - V_{\text{Th},n}) > 0$, an ambipolar transistor behaviour is exhibited, where both holes and electrons carriers contribute to the I_d current flow:

$$I_d = \frac{W2L}{2} [\mu_n(V_g - V_{\text{Th},n})^2 + \mu_p(V_d - (V_g - V_{\text{Th},p}))^2] \quad (16)$$

(iv) For $V_d \geq (V_g - V_{\text{Th},p})$ and $(V_g - V_{\text{Th},n}) < 0$, the current flow in the transistor is mainly determined by holes, resulting in the following expression:

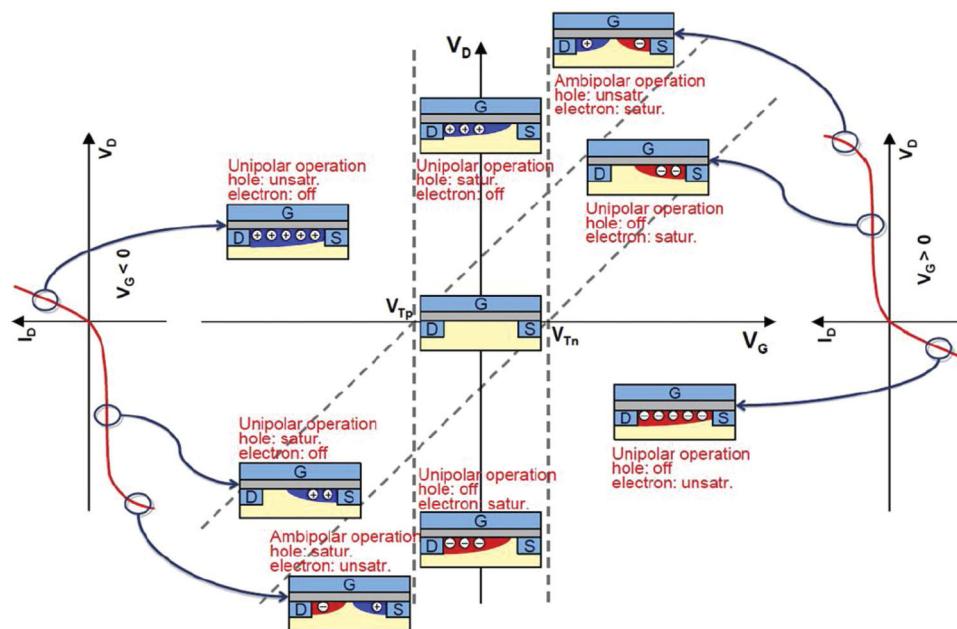


Figure 22. Different operation modes of an ambipolar TFT depending on the applied bias voltages. Reproduced with permission from Ref. [224]. Copyright 2012, Elsevier B.V.

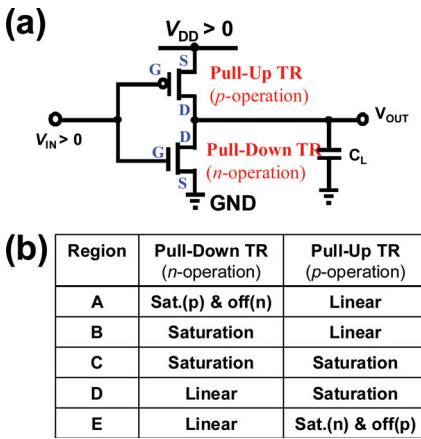


Figure 23. Ambipolar inverter circuit. (a) Circuit configuration, (b) various operation regions, and (c) corresponding voltage transfer characteristics of the ambipolar inverter.

$$I_d = \frac{W}{L} \mu_p (V_d - (V_g - V_{Th,p}))^2 \quad (17)$$

In these equations, μ_n and μ_p are the electron and hole charge carrier mobilities, respectively. A detailed description of the device physics of ambipolar organic transistors can be found in a comprehensive review by Zaumseil et al.^[220]

6.2. Operation of Circuits Based on Ambipolar Semiconductors

Since an ambipolar OFET can work in both accumulation modes, this can in principle be used both as the *p*- and *n*-channel device in a complementary architecture (**Figure 23**). However, the voltage transfer characteristic VTC of such an inverter directly reflects the characteristic behaviour of the ambipolar devices. In the following the VTC of a complementary inverter based on ambipolar semiconductors, referred as complementary-like inverter, is described with reference to the five operating regions of Figure 23.

In region A, both the pull-down and pull-up transistors in the ambipolar inverter are ON and operate in a unipolar, *p*-channel regime. Only the *p*-channel in the pull-up ambipolar transistor is operating in the saturation region, while the *p*-channel in the pull-down ambipolar transistor is also operating in linear mode.^[224] When the equations for the current of both transistors in the respective operation modes are solved, the output voltage for the ambipolar inverter (V_{OUT}^{ambi}) in this region A leads to the following Equation (18):

$$V_{OUT}^{ambi} = (V_{IN} + |V_{Th,p}|) + \sqrt{(V_{DD} - (V_{IN} + |V_{Th,p}|))^2 \cdot \frac{\beta_p^p}{\beta_p^p + \beta_N^n}} \quad (18)$$

where $\beta_N^n = \frac{\mu_n^n C_g W_N}{L_N}$ and $\beta_p^p = \frac{\mu_p^p C_g W_p}{L_p}$ are the design factors for pull-up (subscript *P*) and pull-down (subscript *N*) transistors in the *p*-channel (superscript *p*) or *n*-channel (superscript *n*) operation regions. Furthermore, μ_p^N , W_N , and L_N are the hole mobility, channel width, and channel length of the

pull-down ambipolar OFET, while μ_p^P , W_p , and L_p are the hole mobility, channel width, and channel length of the pull-up ambipolar OFET, respectively. Notably, in region A, μ_p^N would become zero for a truly complementary inverter, where a unipolar *p*-type pull-up transistor and a unipolar *n*-type pull-down transistor are adopted. Therefore, the β_p^N term is removed for the output voltage (V_{OUT}) equation of a CMOS-like inverter, i.e. $V_{OUT} = V_{DD}$ at $V_{IN} = 0$ V.

In region B, the pull-up transistor operates in the saturation regime with ambipolar behaviour (both electrons and holes contribute to the current flow), while the pull-down transistor operates in a linear *p*-channel regime. Therefore, the V_{OUT}^{ambi} in region B is

$$V_{OUT}^{ambi} = (V_{IN} + |V_{Th,p}|) + \sqrt{(V_{DD} - (V_{IN} + |V_{Th,p}|))^2 \cdot \frac{\beta_p^p}{\beta_p^p + \beta_N^n}} \times \sqrt{-(V_{IN} - V_{Th,n})^2 \cdot \frac{\beta_N^n}{\beta_p^p + \beta_N^n}} \quad (19)$$

where $\beta_N^n = \frac{\mu_n^n C_g W_N}{L_N}$ and μ_p^N are the design factor and the electron mobility for *n*-channel operation in the pull-down ambipolar transistor, respectively.^[224]

In region C, both the pull-up and pull-down transistors operate in the saturation regime. In this regime they show complementarity, as the pull-up FET operates in *p*-channel mode, and the pull-down in *n*-channel mode. Because there is no contribution from the ambipolar charge transport in the operation of inverter, the obtained equation is the same as that of an inverter composed of unipolar transistors, as follows:

$$V_{IN}^{ambi} = \frac{\sqrt{\beta_p^p} \cdot (V_{DD} - |V_{Th,p}|) + \sqrt{\beta_N^n} \cdot V_{Th,n}}{\sqrt{\beta_N^n} + \sqrt{\beta_p^p}} \quad (20)$$

As shown in Equation (20), V_{OUT} is not present since the gain is, theoretically, infinite because of the modelling limitations of the current equation.^[224] In this region C, we find the switching threshold V_{inv} , the point where $V_{IN} = V_{OUT}$. V_{inv} should be located around the middle of the supply voltage (i.e. at $\frac{1}{2}V_{DD}$), since this results in comparable values for NM_H and NM_L .^[94]

In region D, in contrast to region B, the pull-up ambipolar transistor exhibits *n*-channel unipolar operation in the linear region, while the pull-up transistor has ambipolar behaviour and operates in the saturation regime. Finally, in region E, the pull-up transistor exhibits *n*-channel operation with only electrons flowing and operates in the saturation regime, while the pull-down transistor also has only electrons contributing to the channel current and operates in the linear regime. The output voltages of this ambipolar inverter in regions D and E can be expressed by the following Equations (21) and (22), respectively:

$$V_{\text{OUT}}^{\text{ambi}} = (V_{\text{IN}} - V_{\text{Th},n})$$

$$- \sqrt{(V_{\text{IN}} - V_{\text{Th},n})^2 \cdot \frac{\beta_n^n}{\beta_n^n + \beta_p^n}} \\ \times \sqrt{-(V_{\text{DD}} - (V_{\text{IN}} + |V_{\text{Th},p}|))^2 \cdot \frac{\beta_p^p}{\beta_n^n + \beta_p^p}} \quad (21)$$

$$V_{\text{OUT}}^{\text{ambi}} = (V_{\text{IN}} - V_{\text{Th},n}) - \sqrt{(V_{\text{IN}} - V_{\text{Th},n})^2 \cdot \frac{\beta_n^n}{\beta_n^n + \beta_p^n}} \quad (22)$$

Based on these operation models, the VTC of both truly complementary inverters, based on unipolar transistors, and complementary-like ambipolar inverters were simulated for different charge carrier mobility ratios and threshold voltages, as shown in **Figure 24**.^[224] It is noted that for equivalent electron and hole transport properties of the *n*-type and *p*-type transistors, V_{inv} is in the middle of the supplied voltage, at $\frac{1}{2}V_{\text{DD}}$. On the other hand, for unbalanced charge carrier transport properties, the V_{inv} shifts to higher V_{IN} when the hole mobility exceeds the electron mobility and, conversely, to lower V_{IN} for superior electron mobility.^[224] As it can be seen in Figures 24b and 24d, an increase in V_{Th} also strongly affects the shape of the VTC characteristics of both the complementary and complementary-like inverters. From these simulations, limitations of adopting ambipolar polymers in a complementary design are evident: since both the *n*-channel in the pull-up transistor and the *p*-channel in the pull-down one cannot be switched off at

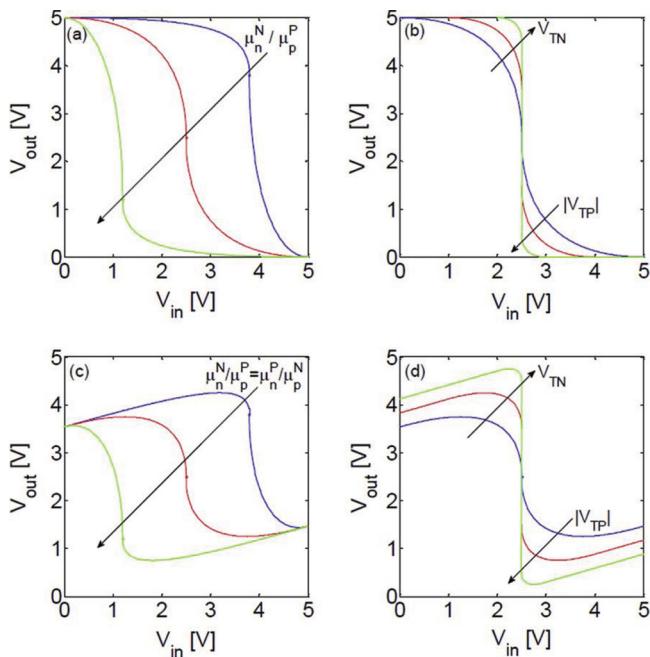


Figure 24. Simulated VTC of (a and b) a CMOS and (c and d) an ambipolar inverter for different (a and c) charge carrier mobility ratios ($V_{\text{DD}} = 5 \text{ V}$; $V_{\text{TN}} = V_{\text{TH}} = 0 \text{ V}$; $\mu_n^n/\mu_p^p = \mu_p^p/\mu_n^n = 0.1, 1, 10$) and (b and d) threshold voltages ($V_{\text{DD}} = 5 \text{ V}$; $\mu_n^n/\mu_p^p = \mu_p^p/\mu_n^n = 1$, $V_{\text{TN}} = V_{\text{TH}} = 0, 1, 2 \text{ V}$). The VTCs were simulated for $L_N = L_p = 2 \mu\text{m}$ and $W_N = W_p = 1000 \mu\text{m}$. Reproduced with permission from Ref. [224]. Copyright 2012, Elsevier B.V.

low and high V_{IN} values, respectively, rails are never achieved, the VTC shows a typical “Z-shape”, noise margins are strongly reduced with respect to truly complementary case and static power dissipation is higher.

6.3. Complementary-Like Circuits Using Ambipolar Polymers

As mentioned before, ambipolar organic transistors have been fabricated either by using a single ambipolar semiconductor, unipolar *p*-type/*n*-type semiconductor blends, or multi-layered semiconductor films. Obviously, a single-component/single-layer semiconductor would be the best choice from the perspective of facile IC fabrication. However, this approach inevitably requires efficient electron and hole charge transport at the same dielectric-semiconductor interface and efficient injection of both charge types from the electrodes, which in the literature regarding organic electronics are most typically made of Au, when lithography is adopted to define the source/drain metallization layer, or Ag, when a printing technique is instead adopted. These requirements represented major obstacles, especially regarding charge injection, since most common organic semiconductors have a band gap of 2–3 eV, making it difficult to optimize holes and electrons injection from electrodes made of the same conductor.

As described in Section 2, a variety of low-bandgap conjugated polymers based on alternating electron donor-acceptor units in the polymer backbone have been developed recently. Among them, DPP-based copolymers have shown impressively high and well balanced carrier mobilities for both electrons and holes ($>1 \text{ cm}^2/\text{Vs}$), along with a reduced bandgap of $\sim 1.2\text{--}1.3 \text{ eV}$.^[225] Notably, these carrier mobilities are close to and/or exceed those of the state-of-the-art unipolar conjugated polymers. The DPP acceptor core constitutes a planar moiety capable of forming $\pi\text{-}\pi$ stacks in the solid state, considered one of the key points which lead to efficient charge transport.^[74] For a CMOS-like ambipolar ring oscillator, high f_{osc} of up to 42 kHz were achieved using a DPP-based polymer with balanced and high electron and hole mobilities.^[130]

In Section 5, we described some strategies for improving the performance of printed electronic devices and ICs, which can be directly applied to complementary-like, ambipolar polymers based circuits. Kronemeijer et al. reported a high-performance complementary-like logic inverters and ring oscillators with downscaled channel lengths ($W/L = 120 \mu\text{m}/5 \mu\text{m}$) and thin dielectric thicknesses ($\sim 70 \text{ nm}$) produced using an ambipolar DPP-based selenophene copolymer with a benzothiadiazole (BT) acceptor unit (PSeDPPBT), showing high electron (up to $0.46 \text{ cm}^2/\text{Vs}$) and hole (up to $0.97 \text{ cm}^2/\text{Vs}$) mobilities, and the SAG technique.^[74] The SAG technique, which saw the adoption of a secondary $\sim 1\text{-}\mu\text{m}$ -thick self-aligned dielectric on top a $\sim 70\text{-nm}$ -thick primary dielectric, allowed the gate leakage current and overlap parasitic capacitance to be reduced. As shown in **Figure 25**, the SAG inverters operated with a high gain of >30 (>40) at a relatively low $V_{\text{DD}} = 10 \text{ V}$ (20 V), and they showed a V_{inv} very close to $\frac{1}{2}V_{\text{DD}}$. These inverters exhibited relatively good noise margins of $\sim 3.25 \text{ V}$ at $V_{\text{DD}} = 10 \text{ V}$ (65% of $\frac{1}{2}V_{\text{DD}}$) and $\sim 5.75 \text{ V}$ at $V_{\text{DD}} = 20 \text{ V}$ (58% of $\frac{1}{2}V_{\text{DD}}$), mainly limited by

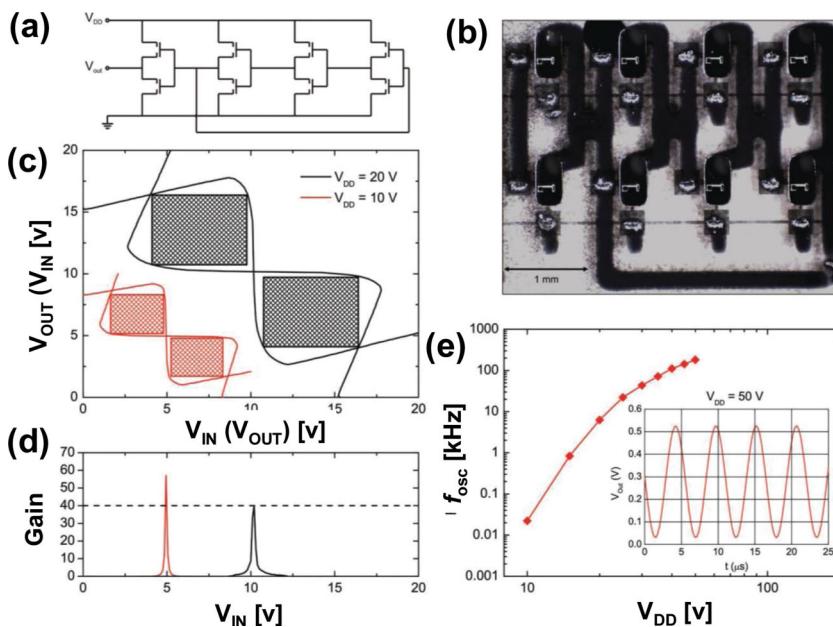


Figure 25. (a) Schematic representation and (b) micrograph of a three-stage ring oscillator with a thin gate dielectric and a low gate overlap capacitance. (c) Input-output characteristics, worst-case noise margin extraction, and (d) gain of constituent inverters at positive drive voltages of 10 V and 20 V. (d) f_{osc} versus V_{DD} for the three-stage ring oscillator. The inset shows the waveform of the oscillation at $V_{\text{DD}} = 50$ V. Reproduced with permission from Ref.^[74] Copyrights 2012, John Wiley & Sons, Inc.

characteristic Z-shaped VTC of complementary-like inverters.^[74] Due to relatively high and better balanced V_{Th} , these values are however relatively high compared to those of typical ambipolar-semiconductor-based inverters,^[76,77] making this logic more suitable for digital circuits.^[74] The SAG inverters were connected to form 3-stage ring oscillators, which showed record high f_{osc} of ~182 kHz (a stage delay of ~0.91 μ s) at $V_{\text{DD}} = 50$ V.

Although several groups have reported high-mobility ambipolar polymer semiconductors exhibiting relatively well-balanced charge carrier mobilities and V_{Th} values, as in the previous case, unbalanced transport is more typical for ambipolar π -conjugated polymers. Thus, the optimized design factor β (Section 6.2) needs to be considered for every electronic device and circuit in order to exactly match the saturation currents for both the *p*-type and *n*-type transistors. To this end, several methodologies for controlling the *p*-channel and *n*-channel OFET properties based on the same active semiconductor layer in complementary-like ambipolar circuits have been reported. These methodologies include (i) charge injection engineering at the semiconductor-contact electrodes^[226] and (ii) charge transport control at the semiconductor-dielectric interface.^[80] Charge injection engineering can on the one side be adopted to induce a unipolarization of an otherwise ambipolar device, providing a way to fabricate a truly complementary logic based on a single ambipolar semiconductor; this will be described in details in the following section. On the other hand, it can be adopted as a way to balance injection of both carriers from the same electrode. Cho et al. demonstrated a promising methodology for gradual control of the metal W_f by formation of the mixed SAMs consisting of alkyl- and perfluoroalkyl-thiols onto bottom-contact Au electrodes. Dipping the samples in

SAM-dispersed solutions with various mixing ratios enabled to control the W_f by changing the surface coverage of each alkyl- and fluorinated SAMs for decreasing and increasing the Au W_f from -5.0 eV to -4.4 eV or -5.6 eV, respectively.^[226] The mixed SAMs-treated Au electrodes were used as source/drain electrodes of the ambipolar polymer OFETs to obtain efficient charge injections for both electrons and holes carriers. The OFET devices showed relatively high ambipolar charge transport properties and complementary-like inverter characteristics with small contact resistances, as well as exhibiting systematical controls over the *p*- and *n*-channel behaviors of the ambipolar OFET devices at the specific mixed ratios of the mixed SAMs on Au electrodes.^[226] Baeg et al. reported that both the hole injection and hole transport for OFETs based on the typically *n*-channel dominant P(NDI2OD-T2) polymer semiconductor could be enhanced remarkably through the use of a fluorinated dielectric, P(VDF-TrFE) (see Figure 26). Interestingly, top-gated P(NDI2OD-T2) OFETs with P(VDF-TrFE) dielectrics showed relatively high hole mobilities (up to ~0.11 cm²/Vs) that were almost 100 times greater than those of OFET devices

with the same semiconductor and poly(methyl methacrylate) (PMMA) or polystyrene (PS) dielectrics (~5 × 10⁻³ cm²/Vs).^[80] This was mainly attributed to modulation of the directional interface state by the -C-F dipoles in P(VDF-TrFE), which simultaneously increased the positive (decreased the negative) charge carrier density in the channel and decreased (increased) the charge injection barrier for holes (electrons) from the source/drain electrodes.^[80] This experimental evidence, obtained at high charge density in the thin accumulated channel of a FET, is quite interesting since P(NDI2OD-T2) is known as a typical high-mobility *n*-type semiconductor and both theoretical calculations and measurements, at low charge density regime in diode structures, pointed to an intrinsically unbalanced electrons and holes bulk transport properties.^[227,228] By performing this semiconductor-dielectric interface modification, Baeg et al. successfully demonstrated well-balanced ambipolar OFETs, high-performance ambipolar complementary-like inverters, and ambipolar ring oscillators. In particular, the inverters had an inverter switching point close to half of the supply voltage, i.e. at $V_{\text{in}} \sim \frac{1}{2}V_{\text{DD}}$, a high voltage gain of ~25, and a high noise margin of 67% of the theoretical maximum value of $\frac{1}{2}V_{\text{DD}}$, and the ring oscillators exhibited high f_{osc} of ~3.5 kHz.

The interface dipoles in the gate dielectric and/or self-assembled monolayer on the dielectric surface have been reported to strongly modulate the charge carrier density and, thereby, the charge carrier mobility and the V_{Th} of the OFETs.^[229–232] Kobayashi et al. reported that fluorinated SAMs on the SiO₂ dielectric surface of pentacene OFETs typically enhance the hole carrier density in the channel close to semiconductor-dielectric interface, thus shifting V_{Th} to more positive voltages

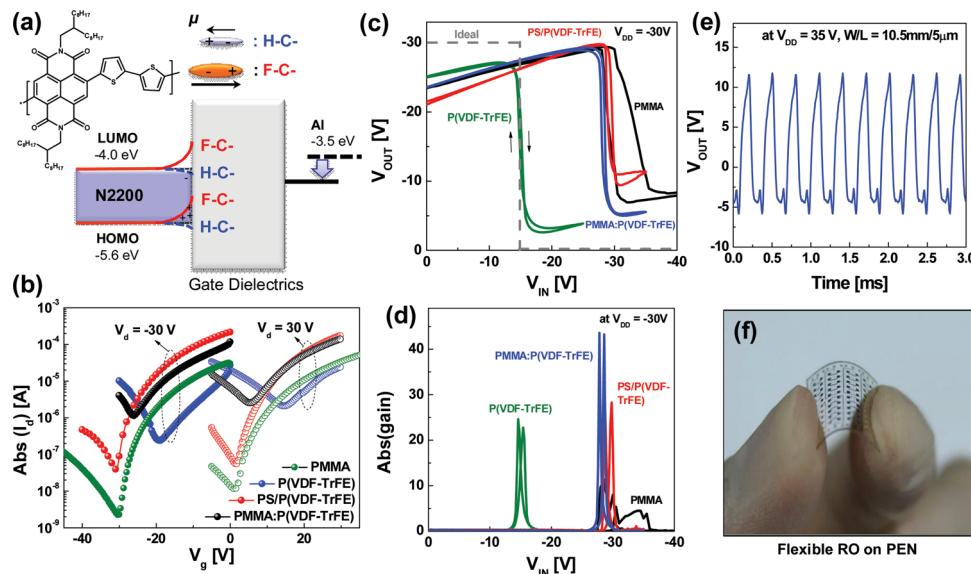


Figure 26. (a) Schematic illustration of semiconductor-dielectric interface modification for ambipolar polymer OFETs. (b) P-channel (at $V_d = -30$ V) and n-channel (at $V_d = 30$ V) transfer characteristics of the P(NDI2OD-T2) OFETs with different polymer gate dielectrics. (c) VTCs and (d) corresponding gain of the complementary-like inverters using the P(NDI2OD-T2) ambipolar polymer semiconductor and different polymer gate dielectrics. (e) Output voltage oscillation characteristics of the 5-stage RO using the P(NDI2OD-T2) with P(VDF-TrFE) gate dielectric, and (f) flexible RO circuits on PEN substrate. Reproduced with permission from Ref.^[80] Copyrights 2012, John Wiley & Sons, Inc.

and increasing the hole mobility.^[231] The opposite effect was also found for *n*-channel fullerene-based OFETs. Furthermore, Boudinet et al. recently presented evidence that charge transport in top-gated OFETs strongly depends on the bottom-substrate chemical functionalization, although the active channel is on the opposite side of the semiconductor film from the chemical functionalized substrate. This conclusion was based on the dramatic changes of V_{Th} and surface carrier density (OFF current) variations which exhibited opposite trends for *p*-type and *n*-type OFETs.^[229] Therefore, using the semiconductor-dielectric interface to control the selective charge transport of either electrons or holes in the same ambipolar semiconductor OFETs could be a promising strategy for realizing complementary-like electronic circuits based on ambipolar polymer semiconductors.

6.4. Truly Complementary Circuits Using Unipolarized OFETs Based on Ambipolar Polymer Semiconductors

The performance of the complementary-like circuits using ambipolar organic semiconductors is strongly determined by the charge injection from the source/drain contact electrodes. It should be noted that efficient charge injection both of electrons and holes from the common metal electrodes is frequently hindered by the charge injection barriers.^[171] The use of high- W_f electrodes made of metals, such as Au and Pt, to facilitate hole injection obviously increases the electron injection barrier height, and low- W_f electrodes have the opposite effect. The low-bandgap polymer semiconductors can simultaneously decrease the injection barriers both for electrons and holes so that ambipolar OFET devices can exhibit relatively high and equivalent electron and hole apparent

device mobilities. The state-of-the-art ambipolar polymer semiconductors show both electron and hole carrier mobilities of more than $1.0 \text{ cm}^2/\text{Vs}$ with the same contacts.^[78] It should also be noted that certain device geometries, such top-gate/bottom-contact (TG/BC) with hydroxyl-group-free polymer dielectrics, exhibit superior ambipolar OFET performance. The reason is that, as we have previously discussed, an overlap between source/drain and gate electrodes can reduce R_c . Moreover, in bottom-contact architecture, a high W_f metal such as Au typically shows a slightly reduced W_f when it comes into contact with the organic semiconductor deposited on top due to the push-back effect on the electron tails near the metal surface induced by the physi-sorbed organic molecules.^[171] Meanwhile, the polymer dielectrics have excellent compatibility with the semiconductor charge transport layer at the interface, without any significant electron or hole trap states, such as those due to hydroxyl groups.^[65] In addition, the polymer dielectrics and the gate metal electrode that are deposited on top can improve the device ambient stability by effectively preventing diffusion of oxygen and moisture to the channel area. For these reasons, the TG/BC-structured ambipolar polymer semiconductor OFETs demonstrated superior *p*-type and *n*-type OFET properties and enabled various high-performance optoelectronic organic devices, such as light-emitting OFETs and photo-sensors.^[233]

Although the efficient electron and hole injection and transport in ambipolar OFET devices is very advantageous for these innovative applications, in electronic circuitry with a complementary-like operation mode this generally causes significant drawbacks, such as reduced noise margins (NMs) and strongly increased static power consumption, as already pointed out in Section 6.2. The decreased NMs critically deteriorates the robustness to noise in digital logic circuits in comparison to

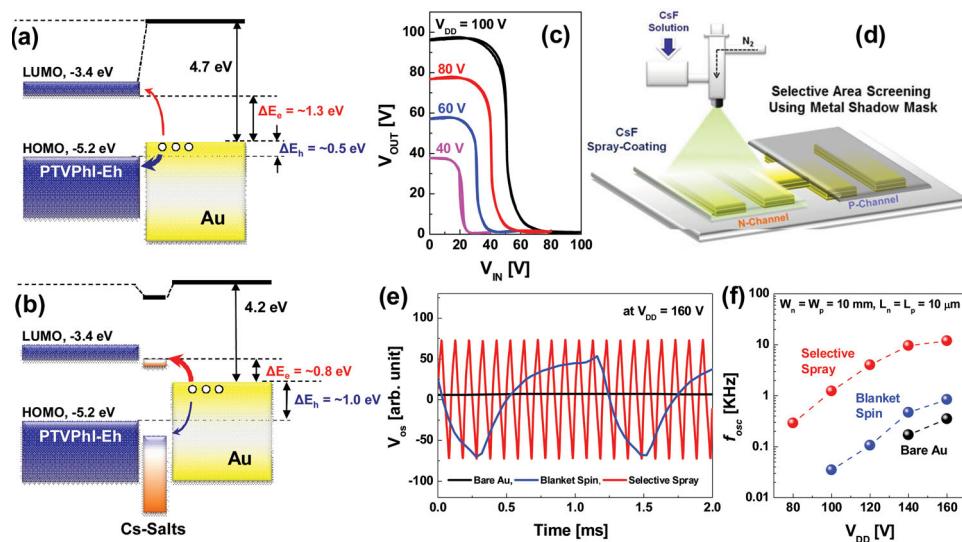


Figure 27. Charge injection engineering using area-selective spray-printed Cs-salts interlayers. Energy level alignment of an organic semiconductor (a) on a pristine Au S/D electrode; and (b) after incorporation of the Cs-salts between the semiconductor and Au electrode. (c) Voltage transfer characteristics after selective spray-deposited CsF layer. (d) Schematic illustration of the area-selective spray printing process. (e) Voltage oscillation (V_{osc}) at $V_{\text{DD}} = 160$ V of the RO under various Au S/D electrode conditions. (f) Dependence of the f_{osc} on the V_{DD} in the 80 to 160 V range. Reproduced with permission from Ref. [79]. Copyright 2011, American Chemical Society.

those of complementary circuits that consist of unipolar *p*-type and *n*-type transistors, and the increased power dissipation obviously causes more heat production during operation and limited operation times for mobile applications in which lightweight portable batteries are used. Therefore, these issues with ambipolar circuits must be solved before they can be applied into commercial applications.

Baeg et al. reported on truly complementary inverter and ring oscillator circuits using unpolarized devices based on the ambipolar poly(thienylenevinylene-co-phthalimide) semiconductors functionalized at the imide nitrogen with 2-ethylhexyl (PTVPhI-Eh) and -dodecyl (PTVPhI-C12) chains (see Figure 27).^[79] The concept proposed is to turn an OFET based on an ambipolar semiconductor in a unipolar device by selectively modifying the charge injection barriers for holes and electrons. In the proposed case, the OFET based on the PTVPhI polymers with Au contacts was found to be mainly a *p*-type device, with a good hole injection, and consequently a hole mobility of 0.1–0.6 cm²/Vs, but much poorer electron injection, which turned out in a suppressed electron apparent mobility of 0.01–0.02 cm²/Vs. It was then demonstrated that it is possible to turn such a device in a prevalently *n*-type OFET by inserting a thin caesium carbonate (Cs_2CO_3) or caesium fluoride (CsF) interlayer as an electron-injection/hole-blocking layer at the semiconductor-Au electrode interface. The OFETs with the Cs-salt charge injection layer demonstrated remarkably improved *n*-channel characteristics, where the electron mobility was increased by >10 times and the holes apparent mobility was decreased by a similar factor. This remarkable change in the ambipolar polymer semiconductor OFET was mostly attributed to the different charge injection barrier height obtained before and after the Cs-salt electron-injection/hole-blocking layer was incorporated. This

methodology was successfully adopted for the first time to realize high-performance truly complementary inverters based on ambipolar polymers thanks to a selective deposition of the contact interlayer onto the *n*-type electronic circuit regions via thermal evaporation or a simple spray printing process. As shown in Figure 27, the resulting inverter exhibited textbook complementary CMOS-like VTC. Importantly, the V_{OUT} loss was also markedly decreased to <+4 V in the static OFF state ($V_{\text{IN}} = 0$ V), and it is negligible in the ON state ($V_{\text{IN}} = +80$ V) because of the suppressed hole current at $V_{\text{IN}} = 0$ V and the enhanced electron current at $V_{\text{IN}} = +80$ V in the *n*-channel pull-down transistor.^[79] This complementary inverter is also characterized by a high voltage gain >50 (at $V_{\text{DD}} = +100$ V), a negligible bias hysteresis, and good NMIs >75% of $\frac{1}{2}V_{\text{DD}}$. In addition, high-speed ambipolar ring oscillators ($f_{\text{osc}} \sim 12$ kHz) were also obtained using the ambipolar polymer semiconductors. Thanks also to other solution-processed charge injection layers and surface modifiers, such as the recently developed polymers containing simple aliphatic amine groups,^[234] demonstrating the possibility to continuously tune the W_f of a given electrode over a large window of values, this pioneering study demonstrated that complementary electronic circuits based on ambipolar polymer semiconductors may become a promising option for the fabrication of a variety of extremely low-cost, large-area organic ICs using R2R GAP techniques.

7. Conclusions

The great progress in developing high mobility, solution-processable, unipolar and ambipolar polymer semiconductors, together with recent advancements in printing deposition techniques, is closing the gap towards real applications of low-cost,

flexible, printed organic electronics. The possibility to fabricate large-area complex ICs at a high throughput with mass-production R2R tools, which represents a huge opportunity that would pave the way for an ubiquitous, widespread adoption of cheap electronic applications, from wearable electronics and sensors, to NFC, RFID tags and devices, has been stimulating a great effort in synthesising novel polymer structures, optimising the rheological properties of inks formulations, overcoming limitations offered by standard printing technologies, developing suitable transistors and logic architectures.

Indeed the recent development of solution-processed D-A copolymers that have overcome another threshold by reaching $10 \text{ cm}^2/\text{Vs}$ charge carrier mobility has once more clearly underlined the huge potentiality of this approach, as on the one side crucial circuits figure of merits, such as the switching speed, scale with mobility, and on the other a higher mobility value obtained at the laboratory scale corresponds to more relaxed constraints in the production step, simplifying the very difficult transition of any potential technology from academic demonstrations to complex and reliable products. Another important factor we like to underline is that such mobilities are being demonstrated in a short time by various groups with different materials, with more and more environmentally stable polymers that show well balanced electrons and holes mobility in the 1 to $10 \text{ cm}^2/\text{Vs}$ range. This is an exciting news which really enables to design complementary logic ICs, benefiting from the same advantages that dictated the fortune of CMOS technology. Thanks to this, complicated dual-gate architectures^[235] or gates with level-shifters^[236] adopted in the recent past for the design of robust unipolar organic circuits, greatly increasing the circuit complexity, are no longer necessary.

Still there are clear challenges to be overcome, that are related both to materials and processes to fulfil the stringent constraints on yield and uniformity needed in a production environment. Regarding materials, while it is expectable that polymers with continuously improved mobility and stability will be developed in the next future, there is a clear requirement for suitable dielectrics that can provide at the same time a high specific capacitance to reduce operating voltages, and processability over large areas by means of simple coating techniques. Printable high- k polymers and relaxors, and in particular the use of electrolytes to gate transistors, represent excellent approaches, that will have to be further developed to show compatibility with integrated fabrication processes. As far as the electrodes and interconnects metalizations are concerned, if from the one side low sintering temperature Ag inks have been developed and are now widely commercial available, on the other a simple costs calculation urges for the development of cheaper, solution processable conducting inks, either carbon-based or inorganic, such as Cu based. This will also widen the possibility to implement ohmic contacts, in combination with stable and reproducible charge injection layers, in devices where the channel length has been downscaled to boost the maximum operation frequency.

Regarding the printing tools, the development of evolved techniques derived from graphical arts printing tools is still undergoing, especially to meet uniformity requirements needed to reduce parameters scattering in circuits and to improve

reliability. Many approaches can be integrated to realize next generation R2R tools, in order to address the other very critical aspects represented by the lateral resolution and registration. If the use of ambipolar polymers relaxes these constraints at the semiconductor level, requiring only a very coarse resolution, the need for short channel lengths on the micron and even submicron scale, and at the same level of importance, reduced parasitic capacitances that require small line-widths definition and control over the alignment of different layers, do not leave room for compromise. To this extent, we believe that recently proposed advanced approaches, based on self-aligned techniques for proper reduction of gate capacitances, and on modification of high resolution printing techniques, such as NIL, for R2R patterning of short channels, combined, when required with laser assisted local sintering and ablation of tiny features, are among the best candidates to enhance the patterning capabilities and produce a convincing answer to these open issues.

Acknowledgements

This research was financially supported by a grant (code no. 2011-0031639) from the Centre for Advanced Soft Electronics under the Global Frontier Research Program of the Ministry of Education, Science and Technology (MEST), Korea and was supported by the Dongguk University Research Fund of 2013; a grant (code No. 13-12-N0101-41) from the Primary Research Program of Korea Electrotechnology Research Institute (KERI). M. C. acknowledges the useful discussions with A. Luzio, S. Bucella, G. Dell'Erba and D. Natali, the partial financial support from Fondazione Cariplo under project Indixi, Grant n. 2011-0368, and from European Union through the Marie-Curie Career Integration Grant 2011 "IPPIA", within the European Union Seventh Framework Programme (FP7/2007-2013) under grant agreement n° PCIG09-GA-2011-291844.

Received: December 31, 2012

Revised: March 12, 2013

Published online:

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