SESSION VIII: Digital Integrated Circuits

THPM 8.3: A Simple Integrated Realization of a New Bistable Circuit*

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THIS PAPER will describe an integrated circuit resulting from the application and extension of a recently developed synthesis procedure for bistable circuits[1]. The synthesis procedure aims to obtain optimum bistable circuits for semiconductor integrated realization. In the synthesis a restriction is made to conventional and field-effect transistors as the active devices. Tunnel diodes, unijunction transistors, and avalanche transistors are less compatible in structural and/or processing requirements. Non-electronic effects in semiconductors are not considered.

Under the foregoing conditions, the synthesis is used to develop systematically all possible bistable circuits using two active devices. This group is examined to find those circuits best suited for silicon integrated realization, applying the following criteria:

(a)—Minimum number of isolated devices and regions.
(b)—Compatible dimensions and impurity concentrations for common regions.
(c)—Minimum number of processing steps.
(d)—Noncritical processing techniques.

The simple bistable circuit illustrated in (*a*) of Figure 1, is an example of the results of this technique[2]. This circuit has been fabricated in silicon integrated form. Section and plan views are shown in Figures 1(*b*) and 2. These experimental circuits switch approximately 30 v across the internal load resistance in less than a microsecond. Two have been operated in cascade, demonstrating logic gain. Bistable operation is not critically dependent on supply voltages, trigger characteristics or temperature. With minor modification of this design, it should be possible to obtain circuits operating at different voltage and current levels, and to increase the switching speed.

The structure shown in Figures 1(*b*) and 2 was formed using only five photoresist masking steps and three diffusions. It will be noted that the n-type substrate serves simultaneously as the collector of the transistor T_1 and the gate of the field-effect transistor T_2. Because these elements are common, no isolation of the active devices is necessary and the attendant isolation junction capacitances are avoided. Note also that all but one of the necessary interconnections are formed within the silicon rather than on the surface.

The p-type epitaxial layer serves as the base of T_1, the channel of T_2, and the isolating background for the load resistor. The properties of this region determine junction breakdown voltages, which for the experimental circuits were over 100 v.

The three diffusions have high surface doping concentrations and are therefore relatively easy to control. The sheet resistance and junction depth of the second n-type diffusion (n_2) should be well-controlled; the specifications for the other two diffusions are noncritical. Because no pn junctions are formed by double diffusion, defects due to pinholes and pipes are avoided. Furthermore, bistable circuits with similar characteristics may be obtained for a considerable range of epitaxial layer thickness and sensitivity simply by adjusting the depth of the second n-type diffusion. For these reasons it should be possible to produce this circuit with a very high yield.

The bistable circuit (Figure 1 (*a*)) can function as a set-reset flip-flop when triggered as indicated. The circuit may be modified to have the counting property, i.e., so that trigger pulses of one polarity will cause the circuit to alternate between its two stable states. Our most recent synthesis work[3] shows that one way to obtain the counting property is to include a parallel RC combination in the lead from base to ground; Figure 3. The triggering technique shown is the most satisfactory of several possibilities.

The additional resistor and capacitor are included in the integrated structure shown in Figure 4. Experimental circuits of this design have been fabricated and are found to count as predicted. Switching time for this circuit is about 1 μsec; maximum repetition rate is 120 kc. Analysis indicates that by altering dimensions it should be possible to obtain integrated realizations of this circuit which would switch faster.

In comparison with commercially available integrated bistable circuits, the advantages of this circuit are its simple structure, its relatively nonstringent process control requirements, and its high breakdown voltages. On the negative side, fan-out capability and switching speed appear to be limited in comparison with other bistable integrated circuits.

One possible application for the circuit proposed is as a combined binary element and *Nixie* tube driver in digital readout equipment. As indicated it should be possible to build units which would switch the required voltage.

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[1] Hill, L. O., Pederson, D. O., and Pepper, R. S., "Synthesis of Electronic Bistable Circuits," *IEEE PTGCT*, p. 25-35; March, 1963.

[2] A related circuit, called the BIFET, has been developed at Texas Instruments.

[3] Hodges, D. A., Pederson, D. O., and Pepper, R. S., "Systematic Generation of Monostable and Counting Bistable Circuits," *Proc. NEC*, p. 261-281; 1963.

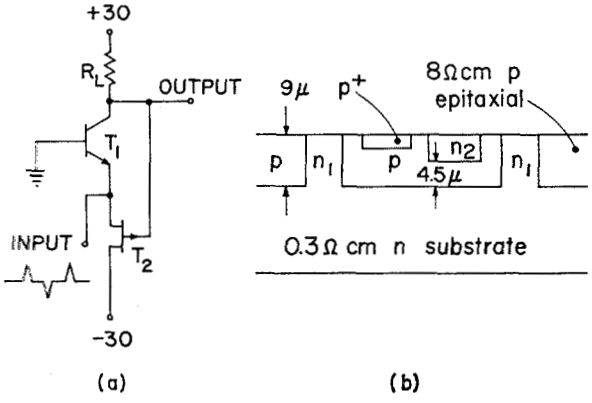

FIGURE 1—At left (*a*), the basic bistable circuit. A section view of integrated realization is shown in (*b*). All three diffusion surface concentrations (n_1, n_2, p^+) are approximately 10^{20} atoms per cm^3.

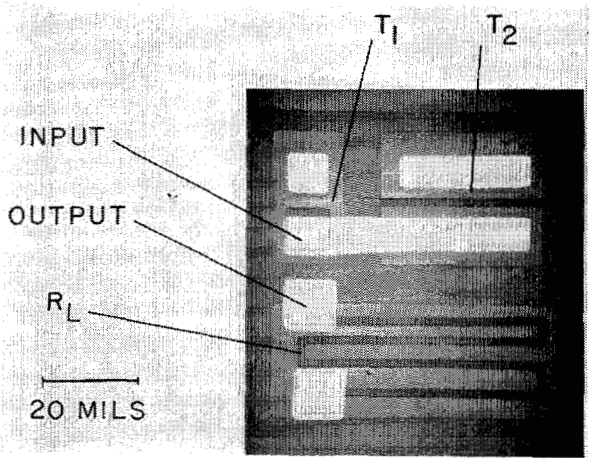

FIGURE 2—Plan view of integrated realization of the circuit shown in Figure 1 (a). Bright areas are evaporated aluminum.

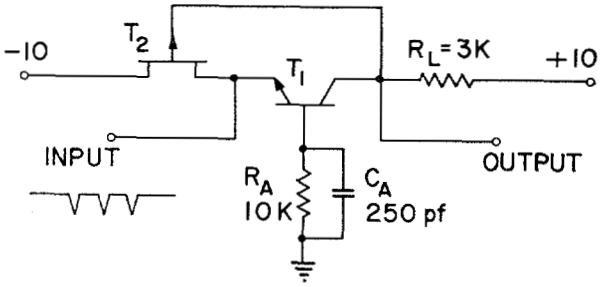

FIGURE 3—Binary counting circuit. The counting operation of this circuit is explained in reference 3.

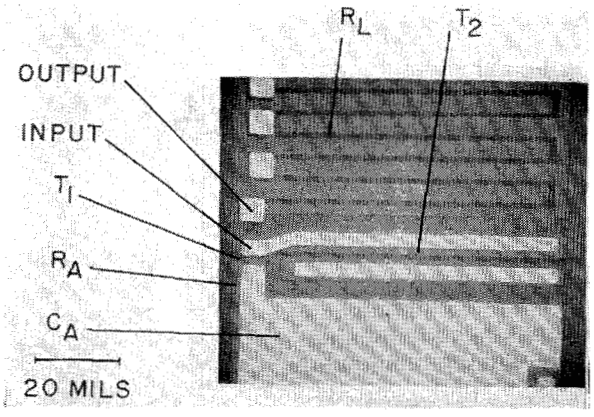

FIGURE 4—Integrated realization of the binary counting circuit. Resistance R_A is formed in the bulk epitaxial material. Capacitance C_A is metal-oxide-silicon.