Ajay Panyala

Scientist
High Performance Computing Group
Pacific Northwest National Lab
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Research Interests

Compiler optimizations and programming models for High Performance and Parallel Computing. Source-to-source program transformations and analysis, out-of-core algorithms, loop transformations, data layout, power/energy optimizations for modern HPC architectures.

Education

Louisiana State University, Baton Rouge
Ph.D., Computer Science (Aug 2007 - Aug 2014)
Advisors: Dr. Gerald Baumgartner, Dr. J. Ramanujam

Jawaharlal Nehru Technological University, Hyderabad, India
B.Tech., Computer Science (Aug 2003 - May 2007)

Professional Experience

Pacific Northwest National Lab
Scientist (Mar 2018 - present)
High Performance Computing Group

Pacific Northwest National Lab
Post Doctorate Research Associate (Oct 2014 - Dec 2017)
High Performance Computing Group

Journal Publications

1. **Exploring performance and energy tradeoffs for irregular applications: A case study on the Tilera many-core architecture.**
   Ajay Panyala, Daniel Chavarría-Miranda, Joseph B Manzano, Antonino Tumeo, Mahantesh Halappanavar.
   Journal of Parallel and Distributed Computing (JPDC), June 2017.
2. **Algorithms for Balanced Graph Colorings with Applications in Parallel Computing.**

H Lu, M Halappanavar, D Chavarría-Miranda, A Gebremedhin, A Panyala, and A Kalyanaraman.
IEEE Transactions on Parallel and Distributed Systems (TPDS), May 2017.

3. **Global Transformations for Legacy Parallel Applications via Structural Analysis and Rewriting.**
Daniel Chavarría-Miranda, Ajay Panyala, Wenjing Ma, Adrian Prantl, Sriram Krishnamoorthy.
Journal of Parallel Computing (PARCO), March 2015.

Conference Publications

1. **Approximate Computing Techniques for Iterative Graph Algorithms.**
Ajay Panyala, Omer Subasi, Mahantesh Halappanavar, Ananth Kalyanaraman, Daniel Chavarría-Miranda, Sriram Krishnamoorthy.
International Conference on High Performance Computing, Data, and Analytics (HiPC) 2017.

2. **Optimizing Irregular Applications for Energy and Performance on the Tilera Many-core Architecture.**
Daniel Chavarría-Miranda, Ajay Panyala, Mahantesh Halappanavar, Joseph B. Manzano, Antonino Tumeo.
Proceedings of the 12th ACM International Conference on Computing Frontiers (CF), May 2015.

3. **On the use of term rewriting for performance optimization of legacy HPC Applications.**
Ajay Panyala, Daniel Chavarría-Miranda, Sriram Krishnamoorthy.
International Conference on Parallel Processing (ICPP), September 2012.

Technical Reports

COMPOSE-HPC: A Transformational Approach to Exascale.
David E. Bernholdt, Benjamin A. Allan, Robert C. Armstrong, Daniel Chavarria-Miranda, Tamara L. Dahlgren, Wael R. Elwasif, Tom Epperly, Samantha S. Foley, Geoffrey C. Hulette, Sriram Krishnamoorthy, Adrian Prantl, Ajay Panyala, Matthew Sottile.
Technical Report ORNL/TM-2012/85, Oak Ridge National Laboratory (ORNL), March 2012.

Workshop Publications

Model-Driven Search Based Loop Fusion Optimization for Handwritten Code
A Panyala, P. Bhattacharya, G. Baumgartner, J. Ramanujam.
Proceedings of the 17th Workshop on Compilers for Parallel Computing (CPC), July 2013.

Workshop Presentations

Optimizing Handwritten Tensor Contraction Code: Our Experience.
A Panyala, P. Bhattacharya, G. Baumgartner, J. Ramanujam.
SIAM Conference on Parallel Processing for Scientific Computing (PP), February 2014.

Technical Referee for Journals

International Journal of Parallel Programming (IJPP): 2016, 2017

External Reviewer for Conferences/Workshops

IEEE International Parallel and Distributed Processing Symposium (IPDPS): 2016
International Workshop on Accelerators and Hybrid Exascale Systems (AsHES): 2016
ACM Symposium on High-Performance Parallel and Distributed Computing (HPDC): 2016
International Conference on Parallel Processing (ICPP): 2015
IEEE/ACM International Symposium on Cluster, Cloud and Grid Computing (CCGRID): 2015
IEEE International Symposium on Parallel and Distributed Processing with Applications (ISPA): 2015