

## Education & Scholastic Achievements

Course	College	Year	CGPA/%
Bachelor of Technology in Engineering Physics	IIT Madras	2016-20	7.74

- Qualified for Indian Olympiad: **INOI, INMO, INAO** 2016, KVPY Scholar 2016, NTSE Scholar 2014
- JEE(Advanced) 2016; Achieved **99 percentile** score; attaining All India Rank of 2012

## Work Experience

**Intel Technology India Pvt Ltd | *Product Development Engineer*** **July'20 – Present**

*Pre and Post Silicon Validation on ATE; High Volume Manufacturing*

- Promoted within 2 years from Grade 3 to Grade 5 for exceptional performance.
- Won multiple awards and got recognised 36 times over the last 4+ years for the significant contributions and impact.
- Released scripts to assist in bringing down time for test program development and volume data analysis significantly as part of Automation Workgroup.
- Worked on products using the Intel 7(10nm Enhanced SuperFinFet) and TSMC N3B (3nm) Technology nodes.
- Undergoing a mentorship program in the design team to gain exposure on all aspects of VLSI.

## Internship Experience

**Texas Instruments India | *Summer Internship in Analog Design*** **May'19 – Jul'19**

- Programmed a Python based tool that could efficiently analyse high speed amplifier performance test data.
- Implemented OOP concepts to develop efficient and readable code to help with all functionality requested.
- Implemented a GUI using PyQt5 module for good UX.

## Projects

**NAND2TETRIS | *Ongoing self study from nand2tetris.org*** **July '24 - Present**

- Completed course curriculum on the HDL definition of all building blocks of a custom RISC Microprocessor.
- Covered concepts of behavioral and structural definitions, modularity, standard cell libraries, ISA, Assembly language.

**Digital IC Design | *Signed 8 bit multiplier*** **Jan'19-Apr'19**

- Designed the schematic and layout of a signed 8 bit by 8 bit multiplier from the gate level.
- Implemented Booth's Algorithm for the multiplier stage and a Carry Look Ahead adder for the final stage.
- Inserted a single stage pipeline to improve bandwidth with minimal impact on latency.
- Ensured DRC, LVS clean layout with optimised placement and interconnects to minimise area.

**Analog IC Design | *Two stage Miller Compensated Opamp*** **Jan'20-Apr'20**

- Designed the gate level schematic and parameters for a two stage Miller Compensated Opamp to match the demanded spec of gain, bandwidth and power.
- Used PMOS input pair and a cascode design in the first stage to meet gain requirements.
- Calculated Miller Capacitance to ensure good phase margin, ensured that the device is meeting the specification using LTSpice.
- Used a Common Source Amplifier at the second stage to ensure capacity for large output swing.

## Courses & Technical Skills

**Courses:** Digital IC Design, Analog IC Design, Analog Circuits, Digital Systems and Lab, Analog Systems and Lab, Signals and Systems, Data Structures and Algorithms

**Skills:** JTAG, JMP, JSL, Python, Pandas, PyQt5, C++, Unix, Bash, DFT, SCAN, IO, HDL, Verilog, ISAs

## Positions of Responsibility

**Non Competitive Events Head | *Saarang19*** **Mar'18 –Feb'19**

- Led 3 independent teams adding up to 30 members; conducted multiple events with the core value of inclusivity
- Conducted professional workshops, shows, fun games, engaging activities in Saarang 2019.

## Co-Curricular Activities

- **Volunteer, NSS;** Selected as **Star Volunteer** for the project 'Drishti' NSS IIT Madras for the year 2016-17; Involved in helping the children in St. Louis Institute for the Deaf and Blind learn.
- **Sports;** Represented hostel in Inter Hostel Sports Championship for Badminton(Runners Up), Chess(3rd position).