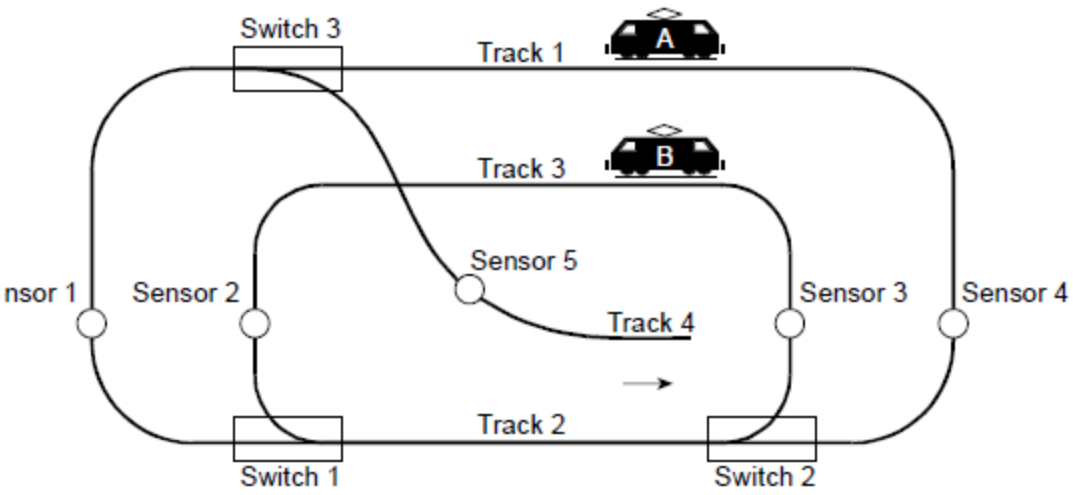


Assumptions

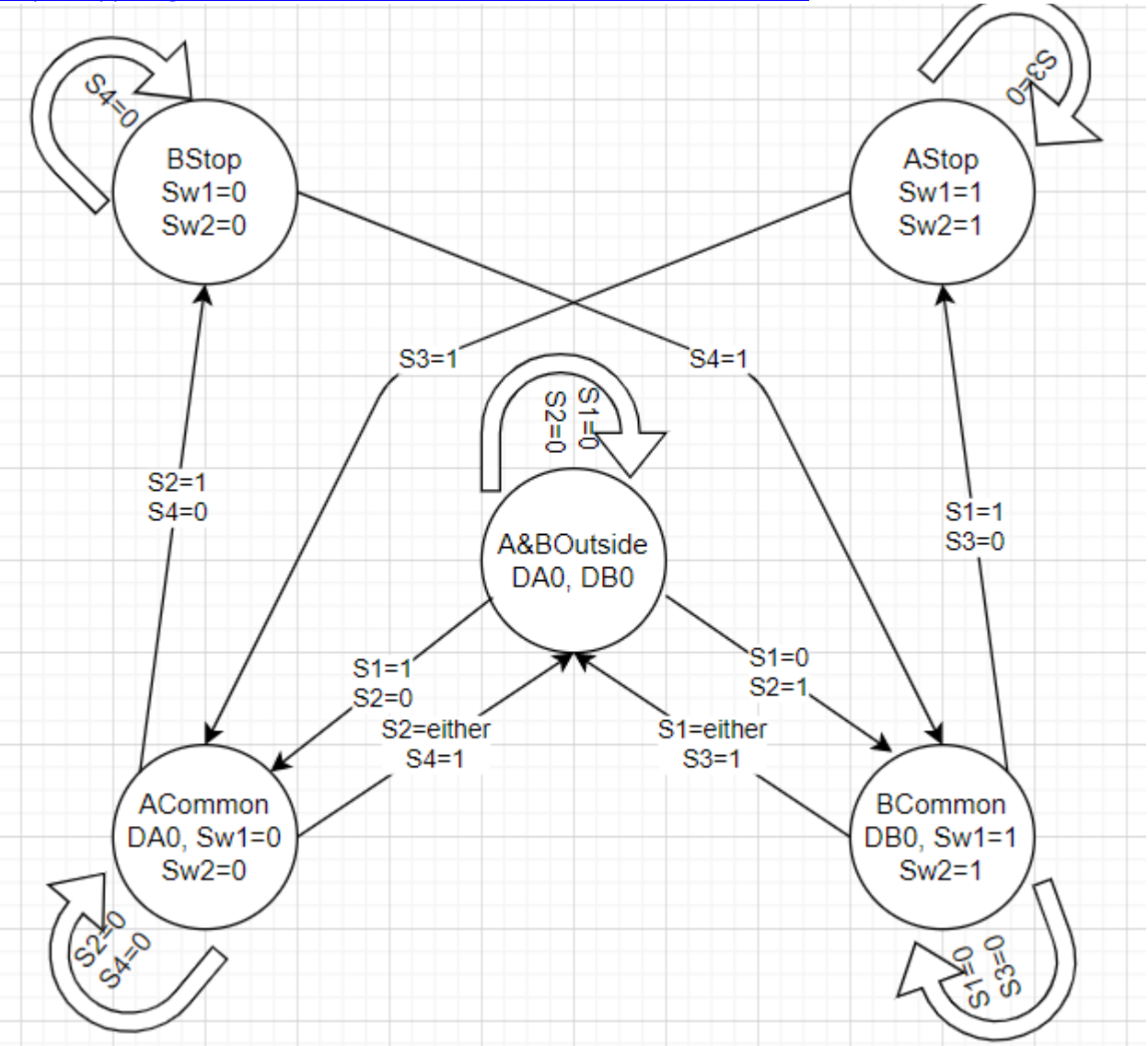
1. The trains start at ABoutside
2. Trains only move forward or backwards
3. Train A cannot enter common track until Train B hits sensor 3
4. Train B cannot enter common track until Train A hits sensor 4
5. Clock rate is fast enough relative to trains speed
6. Trains length doesn't exceed segment of track
7. Reset is synchronous

Output State Table

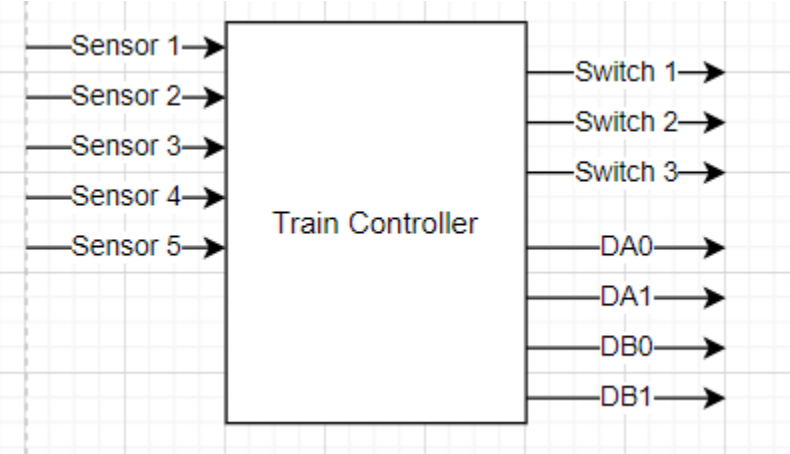
STATE	A&B Outside	Acommon	Bcommon	Astop	Bstop
DA0	01	01	01	00	01
DB0	01	01	01	01	00
S1	0	1	1 or 0	1 or 0	1
S2	0	1 or 0	1	1	1 or 0
S3	0	1 or 0	0	0	1 or 0
S4	0	0	1 or 0	1 or 0	0
S5	0	0	0	0	0
Swtch1	0	0	1	1	0
Swtch2	0	0	1	1	0
Swtch3	0	0	0	0	0
Comments		A track2	B track 2	A @ sensor 1	B @ sensor 2

VISUAL STATE TRANSITION DIAGRAM

https://app.diagrams.net/#G1N2YOVv627QvM0e7RvxwN5kMWzCNE0r6L



BlackBox Diagram



Output Table

```
[2021-01-19 23:09:40 EST] vlib work && vlog -writetoplevels questa.tops '-timescale'
'1ns/1ns' design.sv testbench.sv  && vsim -f questa.tops -batch -do "vsim -
voptargs=+acc=npr; run -all; exit" -voptargs=+acc=npr
QuestaSim-64 vlog 2020.1_1 Compiler 2020.03 Mar  4 2020
Start time: 23:09:40 on Jan 19,2021
vlog -writetoplevels questa.tops -timescale 1ns/1ns design.sv testbench.sv
-- Compiling module ECEAssignment1
-- Compiling module test

Top level modules:
       test
End time: 23:09:40 on Jan 19,2021, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
# vsim test -batch -do "vsim -voptargs=+acc=npr; run -all; exit" -voptargs="+acc=npr"
# Start time: 23:09:40 on Jan 19,2021
# ** Note: (vsim-3812) Design is being optimized...
# //  Questa Sim-64
# //  Version 2020.1_1 linux_x86_64 Mar  4 2020
# //
# //  Copyright 1991-2020 Mentor Graphics Corporation
# //  All Rights Reserved.
# //
# //  QuestaSim and its associated documentation contain trade
# //  secrets and commercial or financial information that are the property of
# //  Mentor Graphics Corporation and are privileged, confidential,
# //  and exempt from disclosure under the Freedom of Information Act,
# //  5 U.S.C. Section 552. Furthermore, this information
# //  is prohibited from disclosure under the Trade Secrets Act,
# //  18 U.S.C. Section 1905.
# //
# Loading sv_std.std
# Loading work.test(fast)
# Loading work.ECEAssignment1(fast)
#
# vsim -voptargs=+acc=npr
# run -all
#                 Time Clear DA0  DB0  S1  S2  S3  S4  S5  SW1 SW2 SW3
#
#                    0   1    x    x    0   0   0   0   0   x   x   x
#                   10   1    1    1    0   0   0   0   0   0   0   0
#                   40   0    1    1    0   0   0   0   0   0   0   0
#                  120   0    1    1    1   0   0   0   0   0   0   0
#                  240   0    1    1    0   1   0   0   0   0   0   0
#                  250   0    1    0    0   1   0   0   0   0   0   0
#                  360   0    1    0    0   1   0   1   0   0   0   0
#                  370   0    1    0    0   1   0   1   0   1   1   0
#                  480   0    1    0    0   0   1   0   0   1   1   0
#                  490   0    1    1    0   0   1   0   0   0   0   0
#                  600   0    1    1    0   1   0   0   0   0   0   0
#                  610   0    1    1    0   1   0   0   0   1   1   0
#                  720   0    1    1    1   1   0   0   0   1   1   0
#                  730   0    0    1    1   1   0   0   0   1   1   0
#                  840   0    0    1    1   0   0   0   0   1   1   0
# ** Note: $stop    : testbench.sv(91)
#    Time: 960 ns  Iteration: 1  Instance: /test
# Break at testbench.sv line 91
# exit
# End time: 23:09:41 on Jan 19,2021, Elapsed time: 0:00:01
# Errors: 0, Warnings: 0
Finding VCD file...
./dumps.vcd
[2021-01-19 23:09:41 EST] Opening EPWave...
Done
```

EDA PLAYGROUND URL

https://www.edaplayground.com/x/NXVD