ECE 611 – Assignment 4 (1 week assignment, 100 points) Due before 11:59 pm 04/05/2017 Electrical and Computer Engineering

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1. Objective

Finding the optimum cache size for a given application.

In this assignment, for **three benchmarks of your choice**, you need to vary the cache size and the cache associativity, and then observe how it affects the processor IPC and the cache power dissipation . From these observations, you need to find a sweet spot. A sweet spot would be the configuration at which you get the highest **IPC/Power** value.

Unit(s)configurations L1 (I-Cache &D-Cache)16KB, 32KB,	64KB, 128KB
L264KB, 128KB, 256KB, 512KB L3 (8way)1MB Associativity(for both L1 &L2)1way,	2way, 4way, 8way, 16way

^{*}The L1 & L2 cache sizes need to be varied for both I-Cache & D-Cache simultaneously.

Once you get the IPC for the above configurations, you need to find the cache power dissipation as well. You should estimate the cache power dissipation using CACTI. CACTI has been developed by HP Lab. You can find it at the following link:

http://quid.hpl.hp.com:9081/cacti/index.y?new

The power dissipation calculation can be done in two ways:

- 1. study all possible cases using CACTI.
- 2. study a few cases and use regression model to calculate the rest. (Studying the power consumption of large number of cache configurations using CACTI tool could be a time consuming task. Instead, you could simply choose to find the power of few cases using CACTI tool and then use a simple regression model to estimate the power of cache as a

function of cache size and cache associativity.)

^{**}You will have 80 cases for SMTsim simulations.

Based on the IPC results and power results, you need to find the right cache configuration for L1 and L2 cache that gives us the highest Performance/Power (IPC/Watt).

2- Instruction

- 1. Run the simulations for all the cash configurations to get the processor IPC.
- 2. Calculate the cache power dissipation for all the configurations. You can do one of the followings:
 - a. Use CACTI for all the configurations.
 - b. Use CACTI for a few configurations and then use the regression model to predict the rest.
 - *As the memory subsystem has three level of caches, for each configuration, you need to run CACTI up to three times (L1 + L2 + L3). The summation of all three runs will be the total power. Please notice that in each run, you need to gather both the dynamic and the leakage power.
 - ** You will have 6*5 = 30 + 1 = 31 (30 L1&L2 + L3) cases. (Some L1 and L2 cases overlap).
 - ***If you choose to use regression model, you need to do it for both dynamic and leakage power **separately**.
- 3. Calculate the target function (IPC/power) for all the configurations.

CACTI

For cacti configuration use the following parameters:

Cache size: all studied cases (make sure to multiply cache size by 1024, instance a cacheso for

size of 16KB is going to be 16*1024 byte)

Line size: keep this at 64

Associativity: change this based on what discussed

Nr. of Banks: always keep this at 1 Technology node: keep this at 90

The figure below show and example of cacti output.

Your total power is "Total read dynamic power per read port at max freq (W)" +

"Total standby leakage power per bank (W)"

Figure below shows how CACTI look:

	Normal Interface	Cacho Size (bytes)	32768
	Detailed Interface	Line Size (bytes)	64
	Pure RAM Interface	Associativity	4
	FAQ	Nr. of Banks	1
		Technology Node (nm)	90
		Submit	12000.00
Cac	he Parameters:		
Nur	mber of banks:1		
	al Caono Size (bytes): e in bytes of bank:327		
Nur	mber of sets per bank:		
Blo	sociativity:4 ck Size (bytes):64		
	sd/Write Ports per bank ad Ports per bank:0	s:1	
Wri	te Ports per bank:0		
	thnology Size (nm):90 1:1.2		
313			
	oces time (ns): 1.83589 odom cycle time (ns):1		
		ycle time (of data array) (ns):0.589	919425074
		y per read port(nJ): 0.36615381941; per read port at max freq (W): 0.31	
		wer per bank (W): 0.0062083365360	
		e of standby leakage power): 0.0	
	al area (mm^2): 2.6571 AM array refresh interv		
	AM array avallability (p		
	at number of wordline s at number of bitline sec		
Bor	st number of sets per v	vordline (data): 1.0	
	st degree of bitline mus		
		o level 1 muxing (data): 4 o level 2 muxing (data): 1	
	at number of wordline s		
	st number of bitline seg st number of sets per v		
	st number of sets per v st degree of bitline mus		
Bes	at degree of sense-amp	level 1 muxing (data): 2	
1368	at degree of sense-ami	level 2 muxing (data): 2	

For this example the power would is 0.3102 Watt

List of Deliverables:

- An XLS file containing all the IPCs, total power numbers and IPC/Power numbers
- A report file in PDF format that includes the followings:
 - 1- For each application: A graph showing the IPC as a function of L1 cache size and associativity when L2 cache size and associativity is 512KB and 4
 - 2- For each application: A graph showing the IPC as a function of L2 cache size and associativity when L1cache size and associativity is 32KB and 4.
 - 3- For each application: Find the configuration with the highest IPC among all studied configurations.
 - 4- For each application: Find the configuration with highest IPC/Power among all studied configurations.

- 5- For each application: The regression models (in case you choose to use regression model).
- 6- For each application: Discussion on the trend you observe relating IPC and power to cache size and cache associativity.

Once completed, submit a **ZIPPED** file with the following syntax **assignmentnumber_first_last.zip** where first_last is your first and last name. For instance, file should be named like this \rightarrow assignment1_Bhoopal_Gunna.zip. Submit the zipped file through the blackboard. Please submit a pdf copy of your report.

WARNING: Points will be taken off if you do not follow the above instructions