ECE 611 – Assignment 5
Spring 2017
(1 week assignment, 100 points)
Electrical and Computer Engineering
George Mason University

1. Objective

Hacking SMTSIM code to generate a memory trace.

In this assignment you are assigned to gather the memory accesses to main memory. You can do that by printing out the required data when the **last level cache (LLC) misses** happen. In order to do so, you need to understand the **cache.c** of SMTSIM simulator.

The data that you need to report as a single access to the main memory includes the following:
1- The **clock** at which the access happens.
2- The memory access **address.**
3- The memory **address type** (either read or write).

Here is an example of the output:

type	**clock**	**address**
read	115838	30f2fb00
read	115857	33af5ac0
write	116015	364288c0
read	116020	38d5b6c0
read	116205	30f30480
write	116435	36428900
read	116437	33af5b00
read	116439	38d5b700

Hints:
1- To print out the data, look for a section of the code (function) in which L3 cache accesses are processed or counted **(cache.c)**.
2- The function which keeps the current **simulation time** can be found in **main.h**.
3- In order to find about the memory access **address** the **CacheRequest** data structure members need to be understood.

You need to generate the traces for both single-core and dual-core simulations for **1M instructions** with **1M fast-forward**. Please use the table below to configure the memory-sub system. Please pick two benchmarks of your choice. So, finally you will have **three different memory traces.**

Unit (s)	Configurations
L1 (I-cache & D-cache)	32KB
L2	256KB
L3 (8-way)	1MB
Associativity (for both L1 & L2)	4-way

List of Deliverables:

- Three memory trace in txt format.
- A report file in PDF format that includes the followings:
  1- For all three simulations, two graphs showing the **number of access over time** with **different sampling intervals** (5k and 20k). So, you will have 200 and 50 samples respectively. In conclusion you need to present 6 graphs for this section.
  2- For all three simulations, the **ratio** of number of reads and number of writes to the total number of accesses (read/total, write/total).
  3- For all three simulations, a **histogram** of time gap between consecutive memory accesses. The bins are in terms of cycles and as followings:
  0 to 100, 100 to 200, 200 to 300,....., 1300 to 1400, 1400 to 1500 and above 1500.
  4- Any **analysis and discussion** on trends you observe in graphs.
  5- A brief exploitation on how you modified the code. Please include your modifications as well.

  Your submission is due before **11:59 pm, 04/19/2017.**

Once completed, submit a **ZIPPED** file with the following syntax **assignmentnumber_first_last.zip** where first_last is your first and last name. For instance, file should be named like this → assignment5_Bhoopal_Gunna.zip.
Submit the zipped file through the blackboard. Please submit a pdf copy of your report.

WARNING: Points will be taken off if you do not follow the above instructions