Alexander DeFalco

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Education

University of Central Florida – Orlando, FL **Fall 2023 – Expected Spring 2026**
Bachelor of Science in Computer Engineering – GPA: 3.84
Relevant Coursework: FPGA Design, Advanced Verification and Validation of Digital Systems, Advanced Computer Architecture, Hardware Description Languages, Hardware Security, Digital Signal Processing, Embedded Systems, Computer Science I/II

Experience

Hardware Assurance and Verification Engineering (HAVEN) Lab – Orlando, FL **October 2024 – Present**
Undergraduate Research Assistant

- Studied embedded FPGA (eFPGA) configurations for logic locking, safeguarding IP throughout the IC manufacturing process
- Explored open-source tools to construct eFPGA architectures, optimizing for area, power consumption, and design efficiency
- Developed eFPGA fabrics from HDL code, conducting PPA analyses in Cadence Genus, optimizing secure hardware designs
- Reviewing literature regarding Zero-Knowledge Proofs (ZKPs) with emphasis on hardware acceleration implementations

Northrop Grumman Corporation – Baltimore, MD **May 2025 – July 2025**
Computer Engineering Intern, Airborne Multifunction Sensors

- Analyzed MATLAB code of legacy RF/analog systems, documenting system architecture, functionality, and workflows
- Collaborated with systems engineers in an Agile environment, implementing software solutions to internal MATLAB toolchains
- Assisted with evaluation of simulated electronic warfare systems, identifying improvements to best model realistic behaviors

Projects

RISC-V Core ASIC Design and Verification with Custom Instruction Set Extension **Cadence EDA Tools**
Senior Design Capstone Project (In-Progress)

- Expanding an open-source RISC-V RTL design to implement instructions that mitigate timing/power-based side channel attacks
- Partaking in Cadence training courses to better comprehend the ASIC/digital design workflow

Single-Error Correcting, Double-Error Detecting (SECDED) Encoder/Decoder Design **Verilog, Tcl, Vivado, Artix-7 FPGA**
Personal Project

- Developed SECDED encoder/decoder modules in Verilog to improve error correction capabilities in data transmission
- Implemented syndrome-based error detection, applying bit-flip corrections for single-bit errors and flagging double-bit errors
- Verified design behavior using Tcl scripts, testbenches, and waveform analysis to ensure robust error handling
- Validated on Artix-7 FPGA through full input coverage of encoder and predictable error scenarios of decoder

Microarchitectural Covert Side-Channel Design **Linux, gem5, C**
Hardware Security & Trusted Circuit Design Lab

- Implemented a cache coherency attack in Linux using gem5, simulating MESI state transitions within an L2 inclusive cache
- Calculated eviction set via pagemap file, enabling CLFLUSH-equivalent behavior for precise cache state manipulation
- Analyzed cache access latencies to distinguish hits and misses, encoding data through cache timing side-channels
- Achieved 100% accuracy in transmitting 50-bit covert messages using E and I states, compensating for cache warm-up effects

FPGA Based Hardware Trojan Design in an AES Crypto-System **Verilog, Vivado, Artix-7 FPGA**
Hardware Security & Trusted Circuit Design Lab

- Explored literature regarding modern trojan detection methodologies, such as side-channel fingerprinting and functional testing
- Implemented three trojans on an AES system, studying impacts on area, power, confidentiality, integrity, and availability
- Designed trojans to minimize changes in logical footprint and power consumption, avoiding conventional detection methods

Ultrasonic Rangefinder PCB Design **Fusion360/Eagle, MSP430, C**
ECE Design Lab

- Designed custom PCBs in Fusion360 through schematic capture and library sourcing for main and 3.3V/5V regulator boards
- Assembled boards with SMD components, utilizing solder paste, stencils, reflow ovens, and pick-and-place machine
- Programmed MSP430 MCU to interface with ultrasonic sensor, LCD, and PWM-controlled LEDs in a battery powered system

Professional Affiliations & Student Involvement

Institute of Electrical and Electronics Engineers (IEEE): Student Member **February 2024 – Present**
Association for Computing Machinery (ACM): Student Member **August 2024 – Present**
STRONG-AI: 2024-2025 Scholarship & Cohort Member, 2025-2026 Scholarship & Peer Mentor **Fall 2024 – Present**

Skills

Programming Languages: C, SystemVerilog/Verilog, Python, Tcl, Java MATLAB, MIPS
Software: Linux, Xilinx Vivado, Cadence Genus, OpenFPGA, Verilog-to-Routing, Yosys, Pyverilog, gem5, LTSpice, MARS, EAGLE