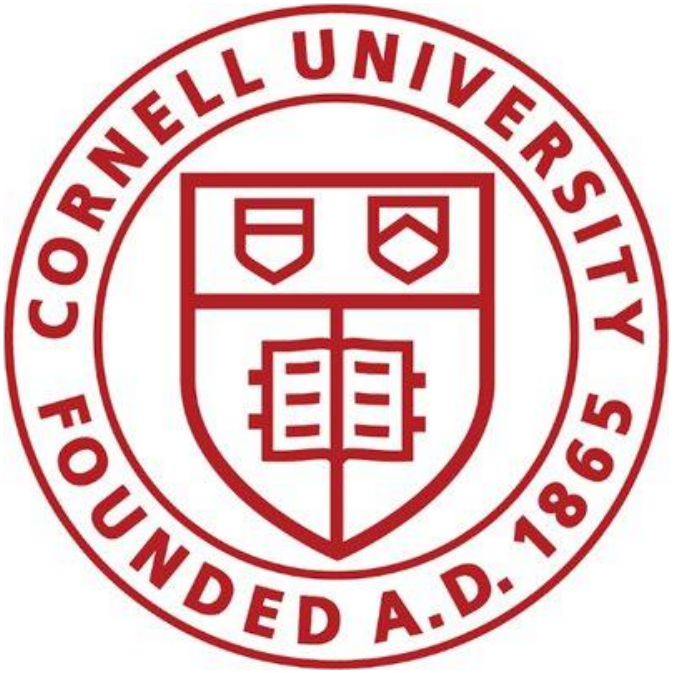
# Conway’s Game of Life implementacija na FPGA




19

Cornell University

United States

Cornell University
School of Electrical and
Computer Engineering

ECE 5760
Advanced Microcontroller Design
and system-on-chip
Spring 2019


# FPGA/Verilog student projects

83 videos • 146,980 views • Last updated on Sep 3, 2018

System-on-chip and embedded control on FPGAs. The following projects were mostly produced in the last month of ECE 5760 in the fall. The students were given the responsibility of choosing their project, then designing and building it. Projects were built using the Altera/Terasic DE2, CycloneII FPGA, educational board. More:
http://people.ece.cornell.edu/land/co...


Bruce Land

79


**virtual paint on FPGA**

Bruce Land

80


**video harp on FPGA**

Bruce Land

81


**3D pong with video paddle tracking**

Bruce Land

82

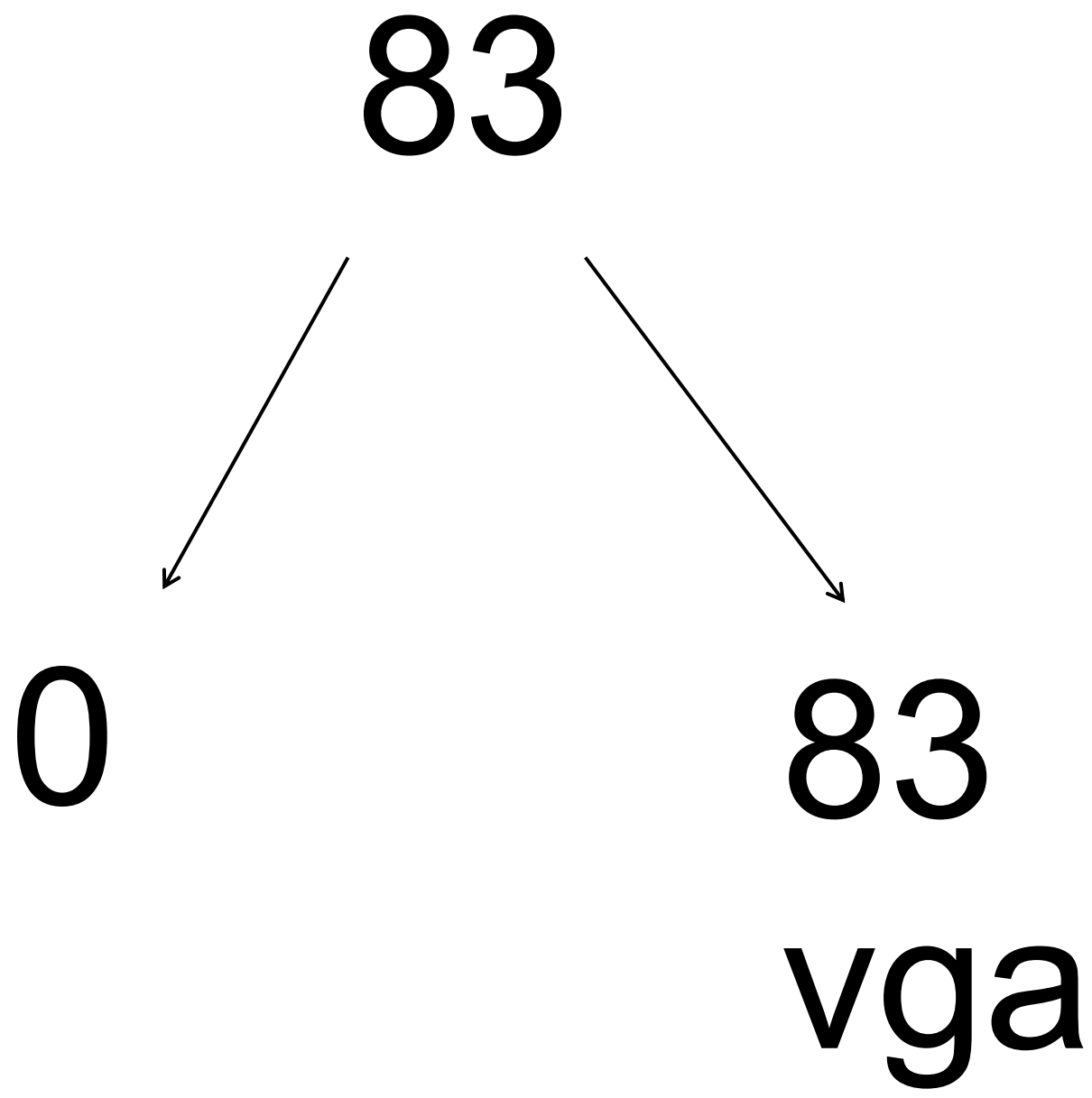

**Split screen for games**

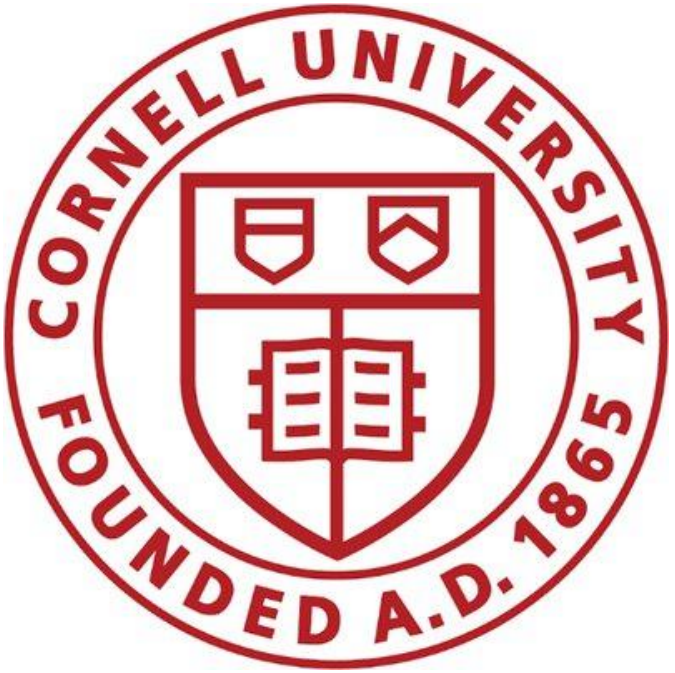
Bruce Land

83


**vioce game**

Bruce Land


83
0
83
vga

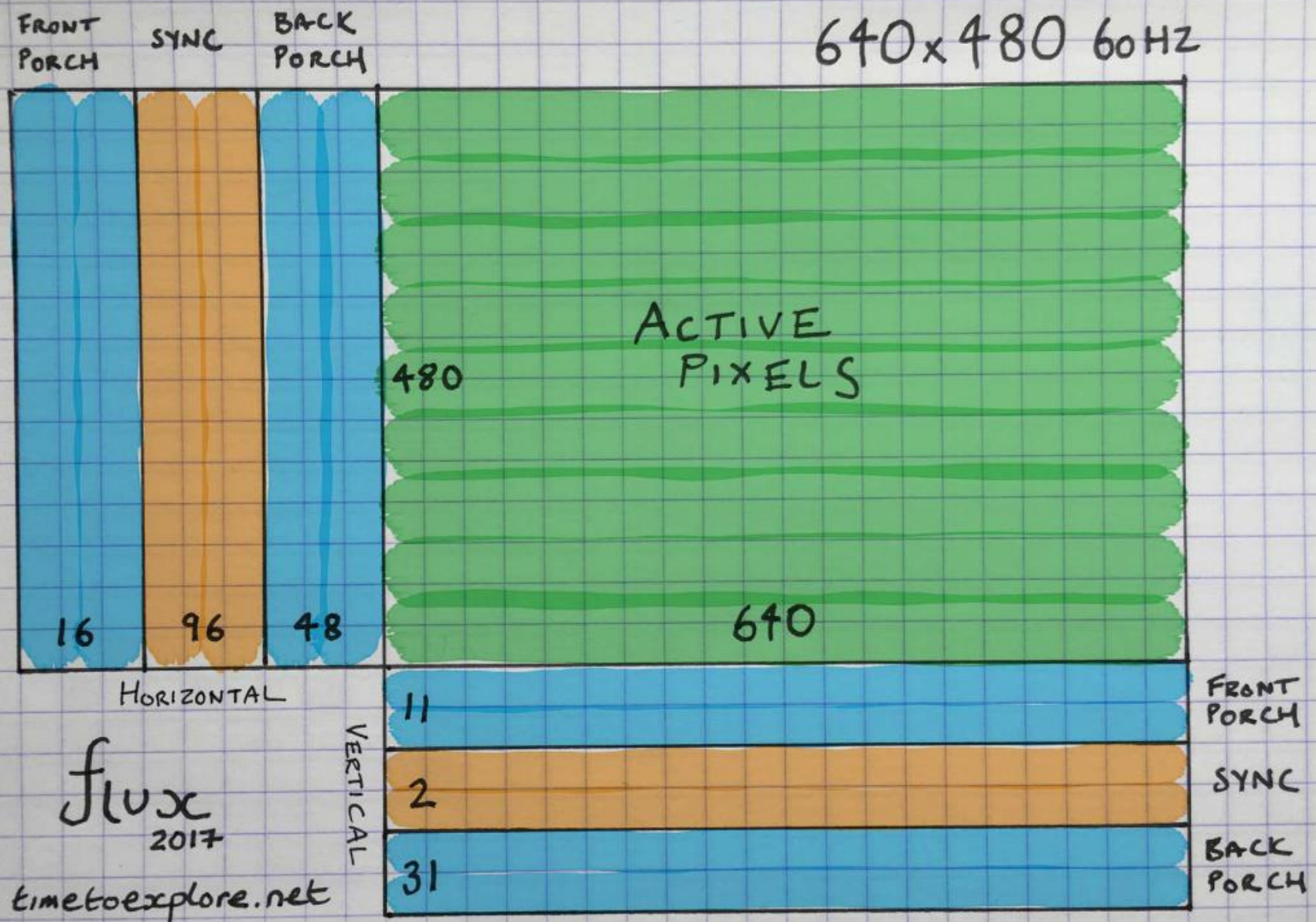



19 Cornell University

United States

>>> ja

# VGA sinhronizacija


FRONT PORCH
SYNC
BACK PORCH
640x480 60Hz
ACTIVE PIXELS
480
16
96
48
640
HORIZONTAL
VERTICAL
11
2
31
FRONT PORCH
SYNC
BACK PORCH
flux
2017
timetoexplore.net

VGA_Param.h

```
1   // Horizontal Parameter ( Pixel )
2   parameter   H_SYNC_CYC  =  96;
3   parameter   H_SYNC_BACK =  45+3;
4   parameter   H_SYNC_ACT  =  640;  // 646
5   parameter   H_SYNC_FRONT=  13+3;
6   parameter   H_SYNC_TOTAL=  800;
7   // Virtical Parameter       ( Line )
8   parameter   V_SYNC_CYC  =  2;
9   parameter   V_SYNC_BACK =  30+2;
10  parameter   V_SYNC_ACT  =  480;  // 484
11  parameter   V_SYNC_FRONT=  9+2;
12  parameter   V_SYNC_TOTAL=  525;
13  // Start Offset
14  parameter   X_START     =  H_SYNC_CYC+H_SYNC_BACK+4;
15  parameter   Y_START     =  V_SYNC_CYC+V_SYNC_BACK;
```

Pixel na poziciji:

(x, y)

obojiti bojom u RGB:

(r, g, b)

gdje su r/g/b vrijednosti:

0-255 (8bitne)

640 (duzina, x osa)

*

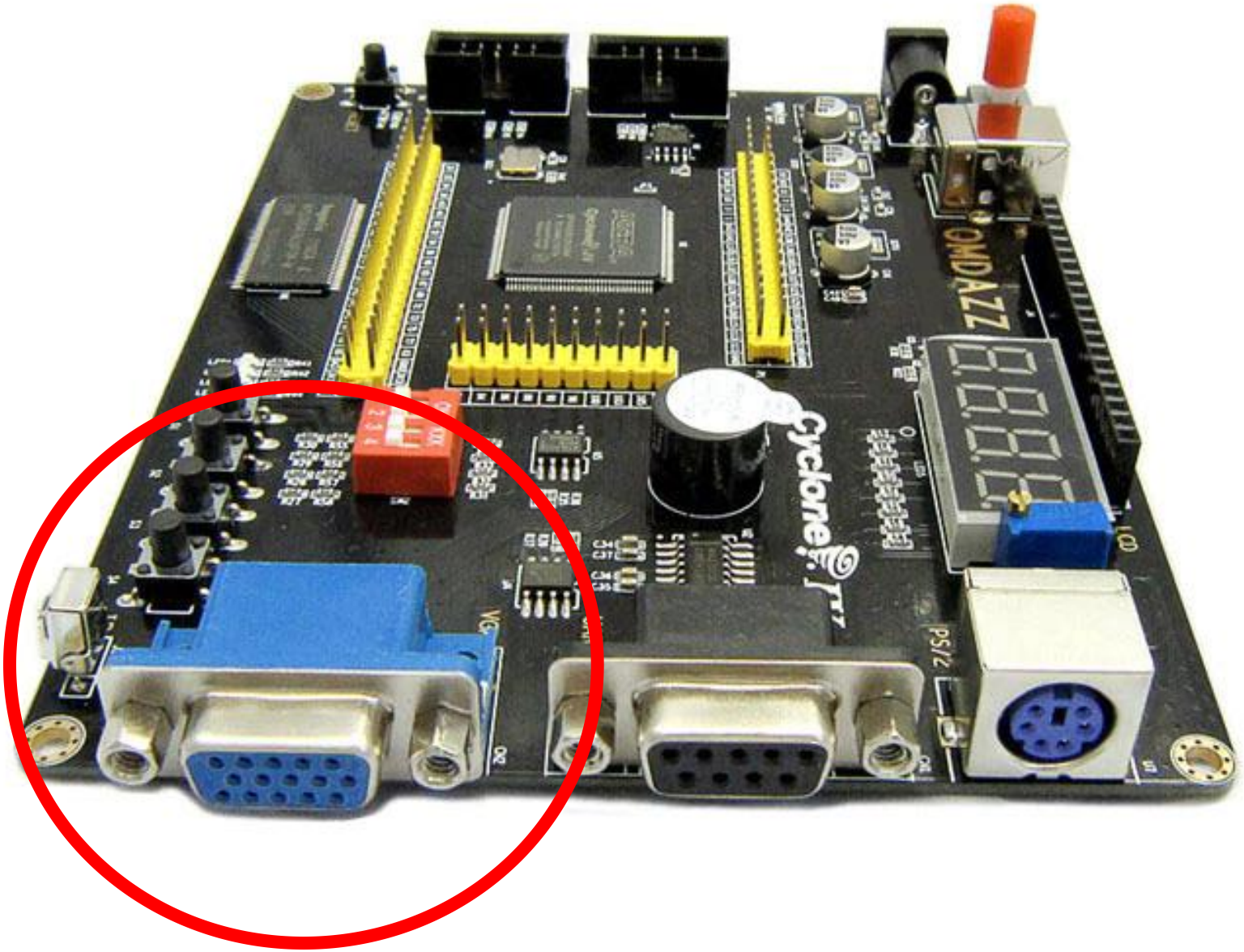
480 (visina, y osa)

*

60 (Hz, refresh rate)

=>

25 MHz clock potreban


OMDAZZ
PS/2

| VGA | Pin number |
| --- | --- |
| VGA_HSYNC | 101 |
| VGA_VSYNC | 103 |
| VGA_B | 104 |
| VGA_G | 105 |
| VGA_R | 106 |

Nema VGA clock-a!

A***c

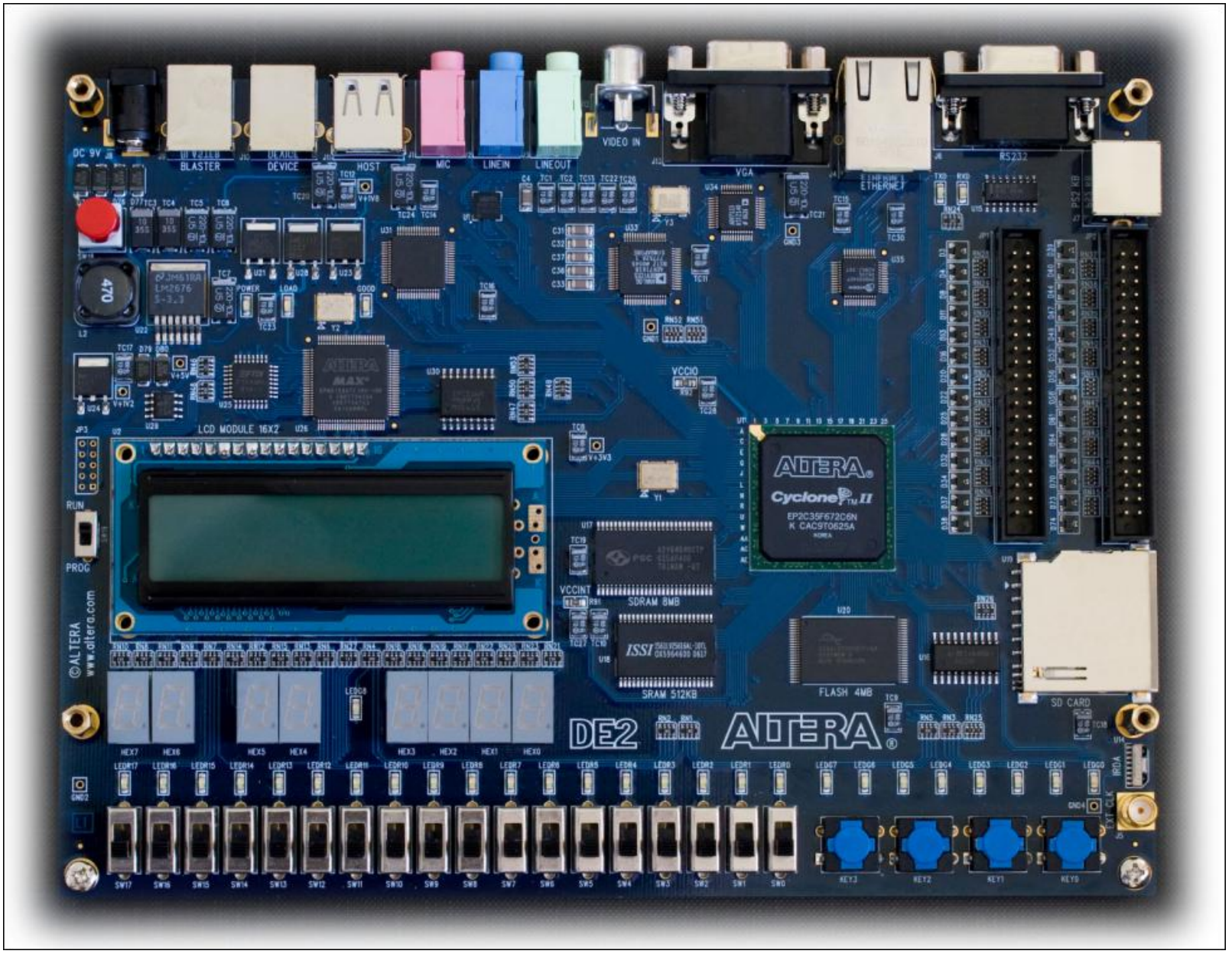
BA

(1)

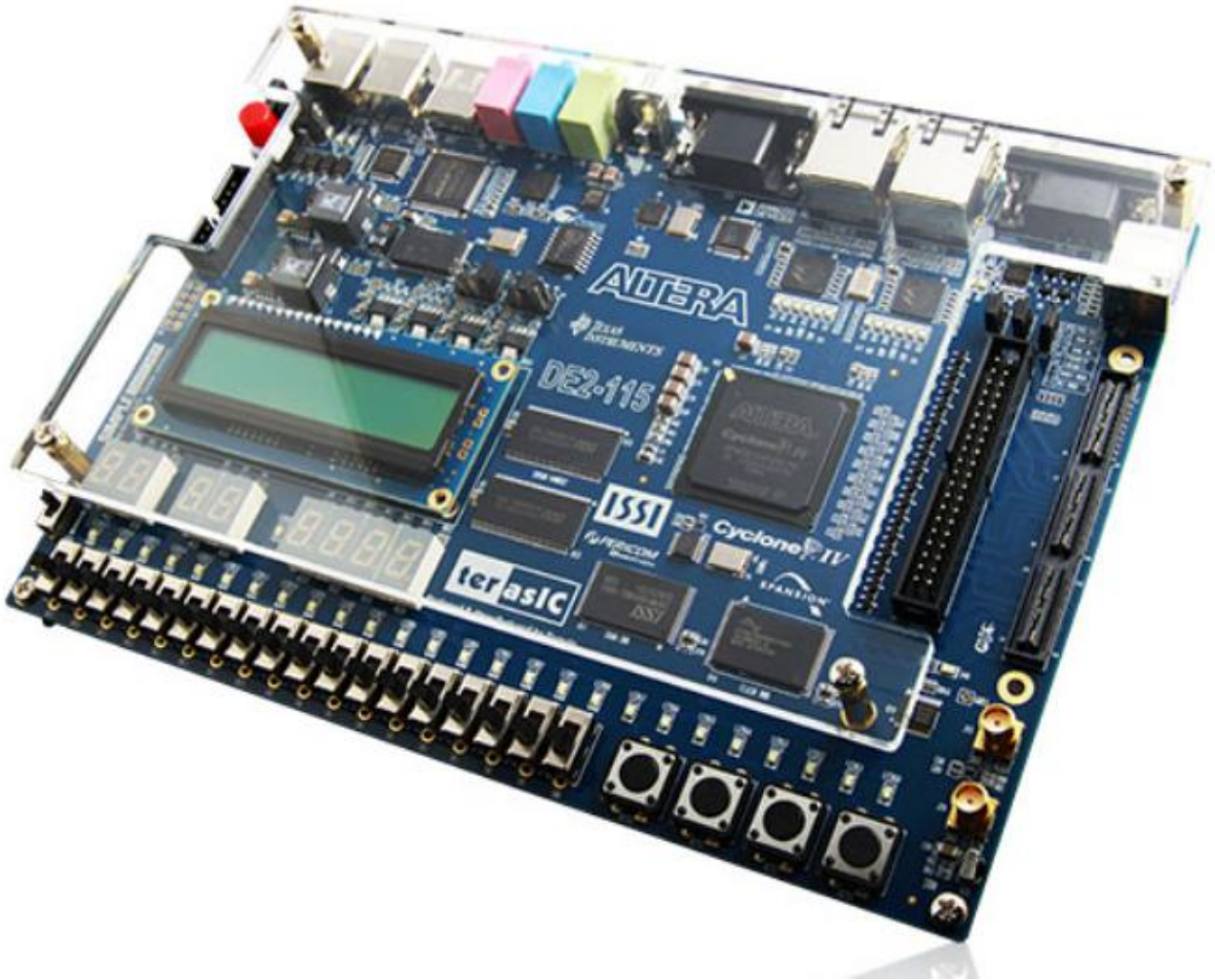
**Color:** EP4CE6 board **Logistics:** China Post Registered Air Mail

I bought this development board because of the VGA output I wanted to create an VGA interface between this FPGA and a monitor Sadly I had to realize this VGA port is just for show. It does not contain a vga clock, neither a bus for R, G, B it dissapointed me a lot now i dont have any need for it description was not accurate

27 Dec 2018 10:36


DC 9V
BLASTER
DEVICE
HOST
MIC
LINEIN
LINEOUT
VIDEO IN
VGA
ETHERNET
RS232
LCD MODULE 16X2
ALTERA
Cyclone II
EP2C35F672C6N
K CAC9T0625A
SDRAM 8MB
SRAM 512KB
FLASH 4MB
SD CARD
DE2
ALTERA
RUN
PROG
©ALTERA
www.altera.com
HEX7
HEX6
HEX5
HEX4
HEX3
HEX2
HEX1
HEX0
SW17
SW16
SW15
SW14
SW13
SW12
SW11
SW10
SW9
SW8
SW7
SW6
SW5
SW4
SW3
SW2
SW1
SW0
KEY3
KEY2
KEY1
KEY0

# Altera DE2-115 Development and Education Board




(Currency: USD)

Price: $595

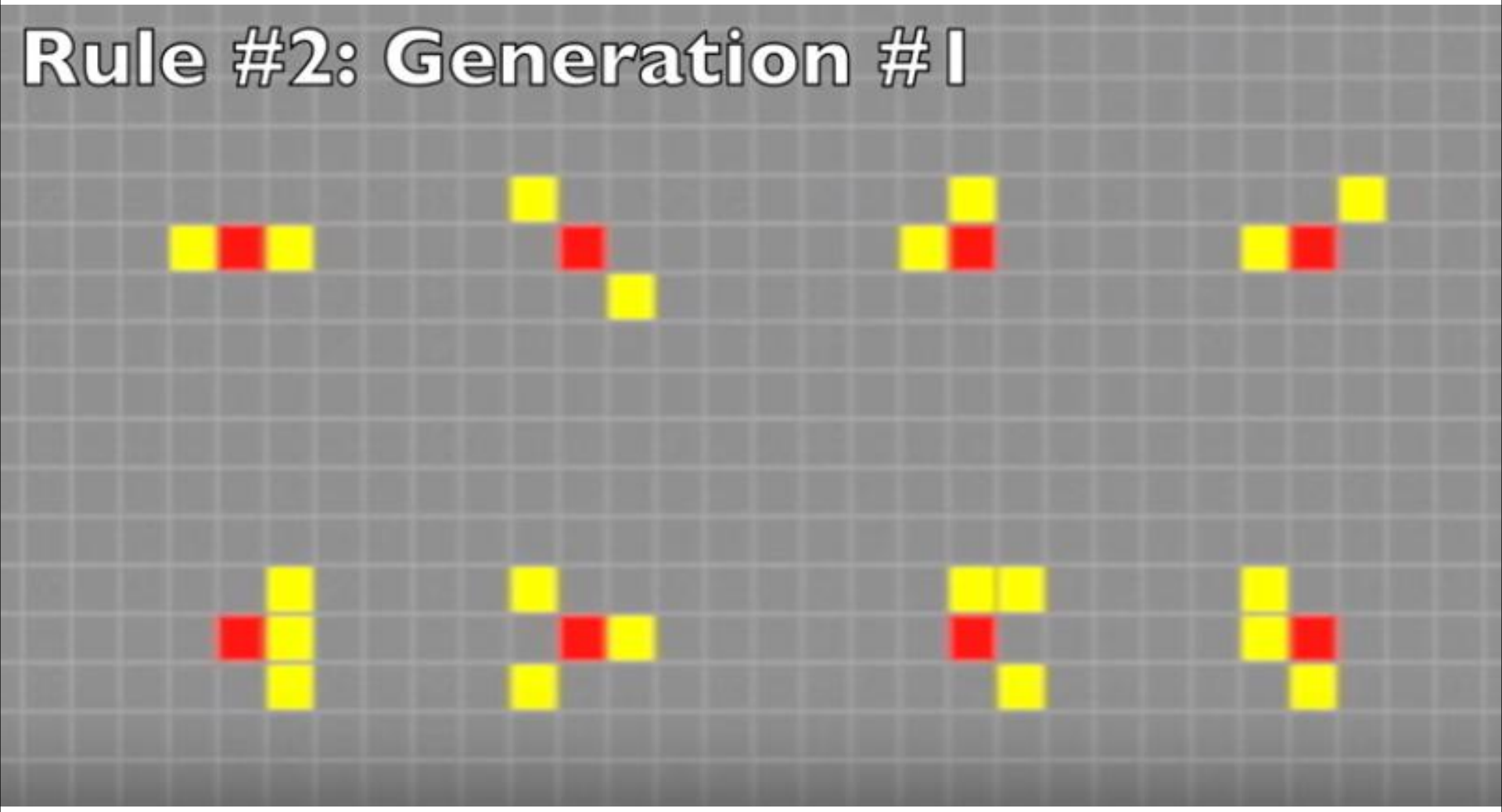
Academic: $309

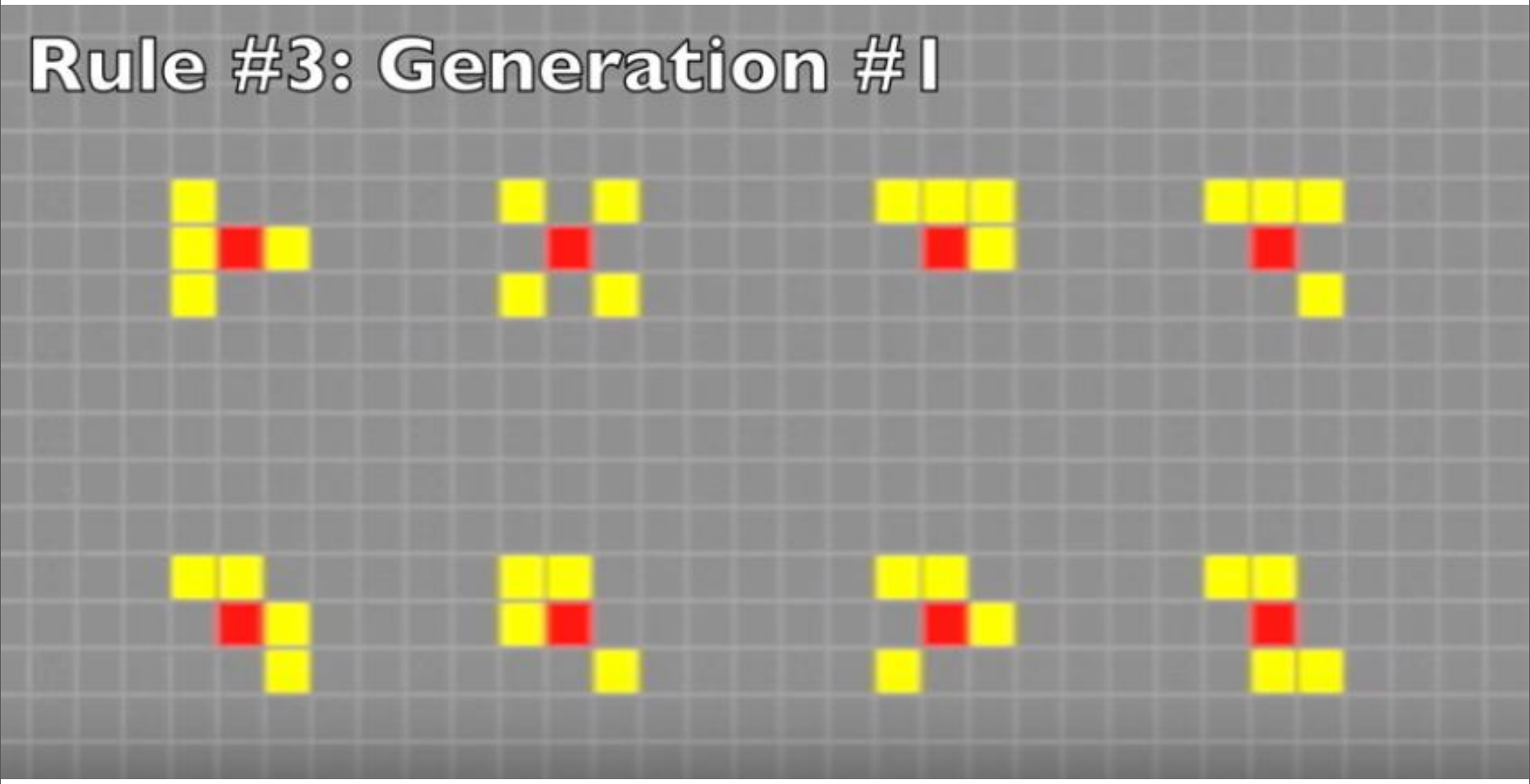
Buy it now

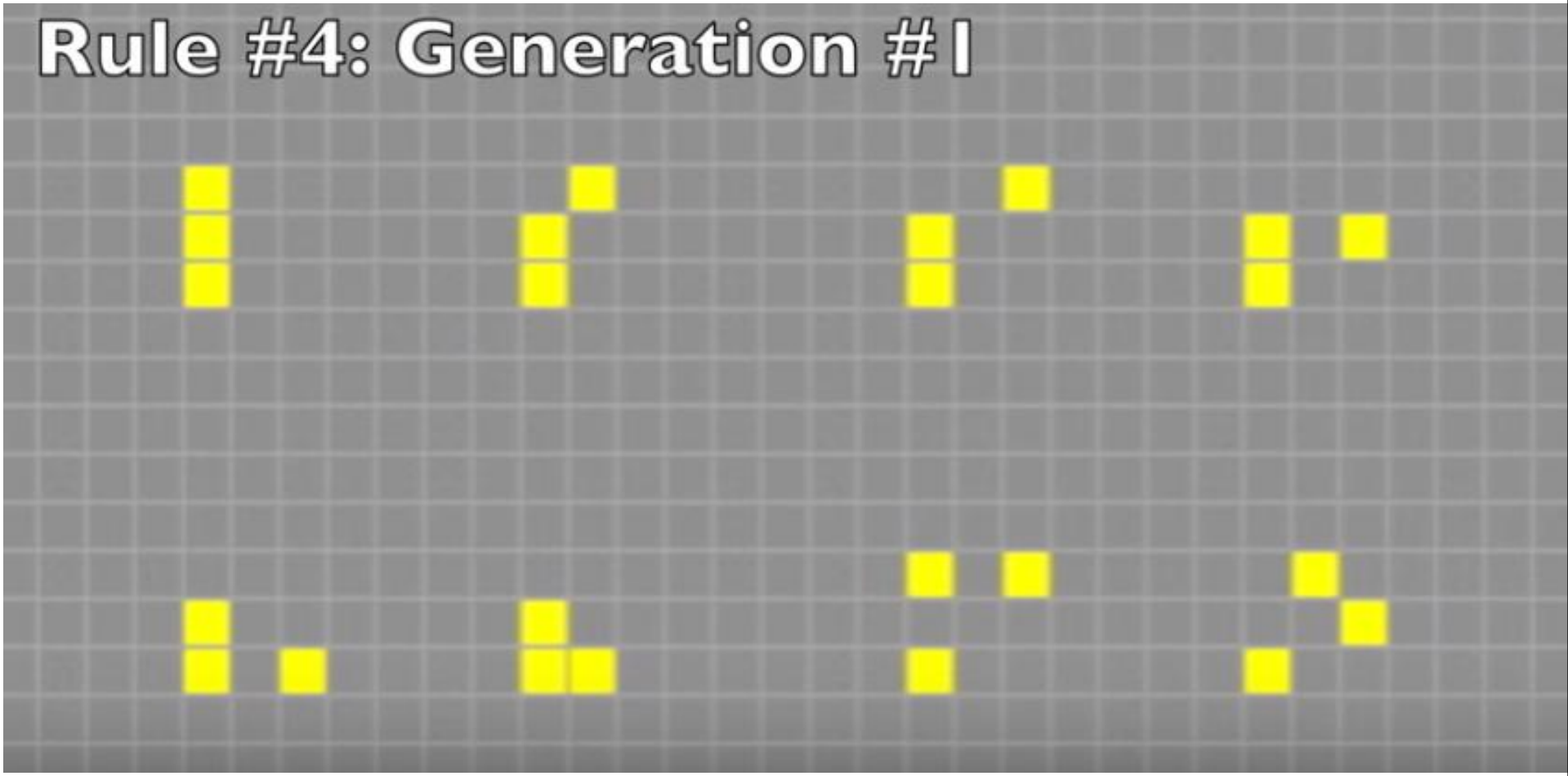
#puno kosta

# Conway's Game of Life

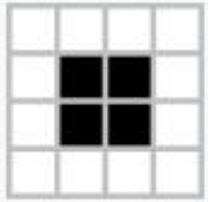
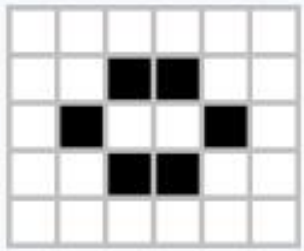
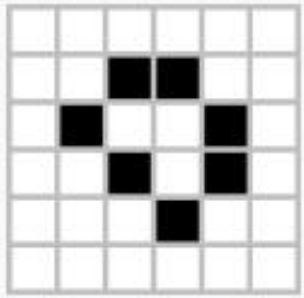
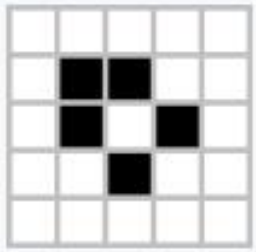
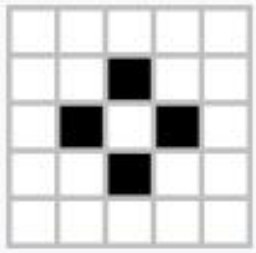
# Rule #1: Possible Generation #1

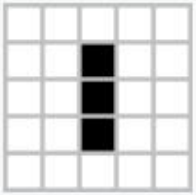
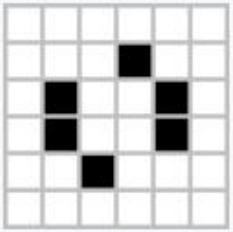
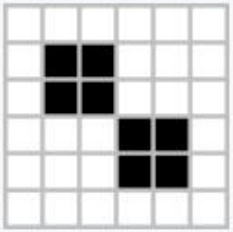
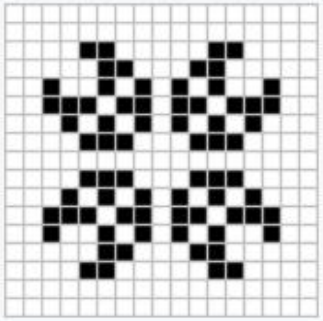
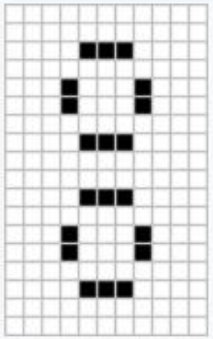

Rule #2: Generation #1

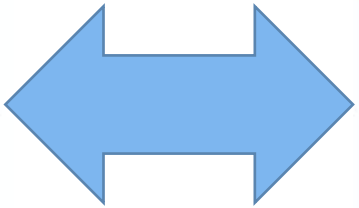

Rule #3: Generation #1

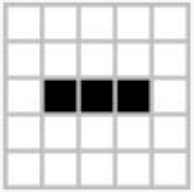
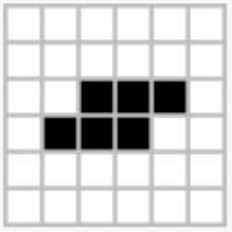
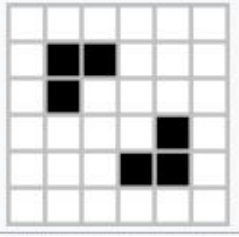
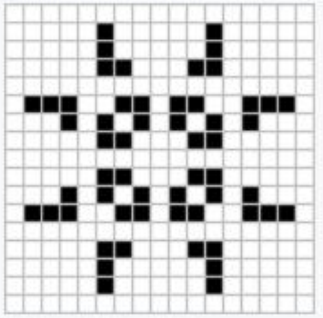
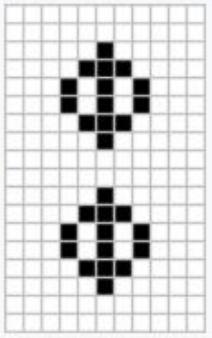

Rule #4: Generation #1

```
cells[i] <=
((cells_preset[i] & (population == 2))
| (population == 3));
```

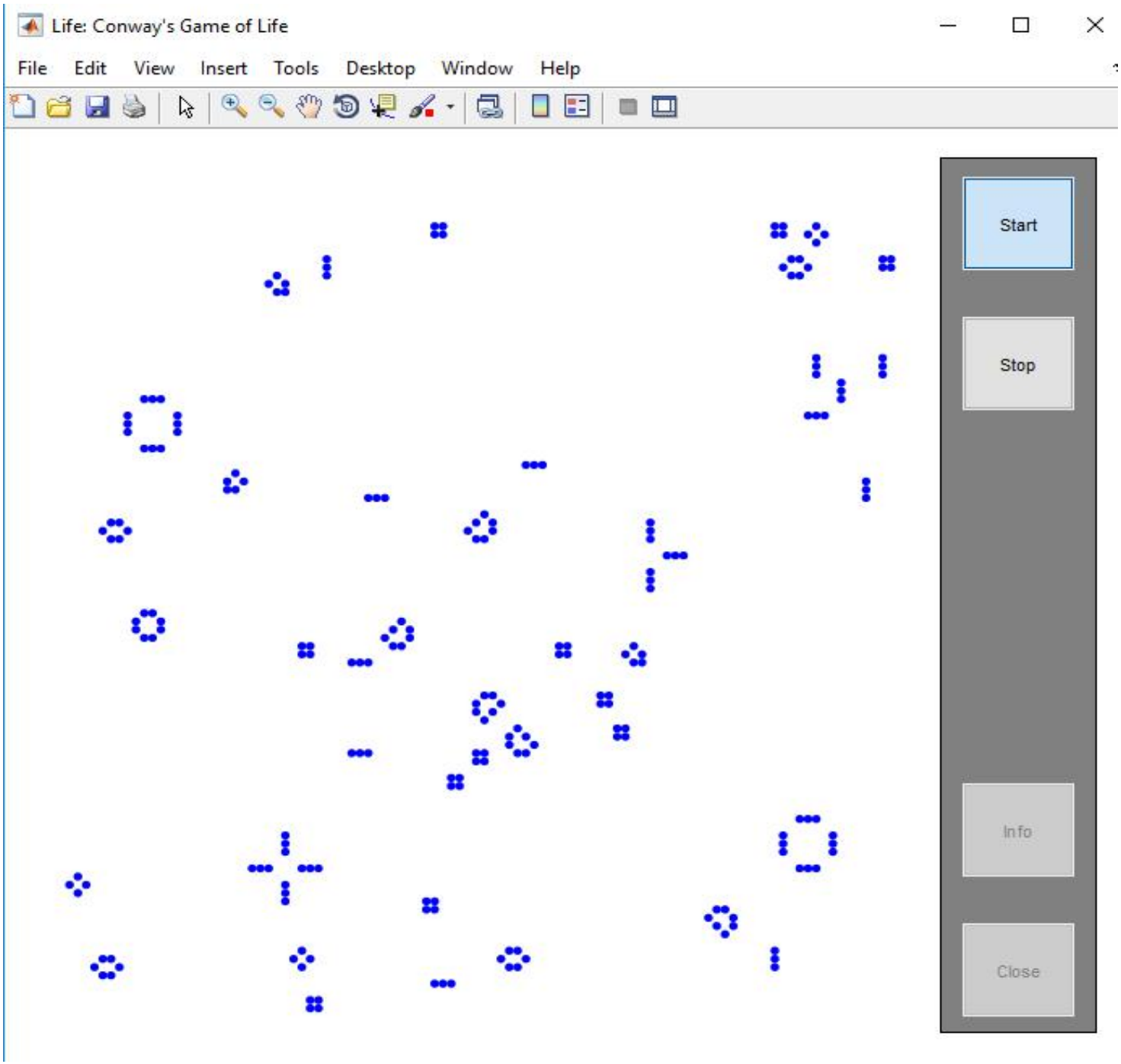
| Still lifes | |
|---|---|
| Block |  |
| Beehive |  |
| Loaf |  |
| Boat |  |
| Tub |  |

| Oscillators | |
|---|---|
| Blinker (period 2) |  |
| Toad (period 2) |  |
| Beacon (period 2) |  |
| Pulsar (period 3) |  |
| Pentadecathlon (period 15) |  |



| Oscillators | |
|---|---|
| Blinker (period 2) |  |
| Toad (period 2) |  |
| Beacon (period 2) |  |
| Pulsar (period 3) |  |
| Pentadecathlon (period 15) |  |

# Implementacija u Matlabu


Life: Conway's Game of Life
File
Edit
View
Insert
Tools
Desktop
Window
Help
Start
Stop
Info
Close

# Implementacija u C-u

# Raspberry Pi 3 Model B


## Raspberry Pi 3 Specifications

**SoC:** Broadcom BCM2837

**CPU:** 4× ARM Cortex-A53, 1.2GHz

**GPU:** Broadcom VideoCore IV

**RAM:** 1GB LPDDR2 (900 MHz)

# Lenovo Thinkpad T420

- Intel® Core™ i5 processor i5-2410M with dual-core, dual thread
- DDR3 memory controller (up to 1333MHz), Intel Turbo Boost, Hyper-Threading technology; 3MB cache
- RAM: 8GB

# Implementacija u Verilogu

```
cells_preset[0    :64*0+63 ] <= 64'b0000000000000000001101010000000000000000001101010000000000000000;
cells_preset[64*1 :64*1+63 ] <= 64'b0000000000000000000000000000000000000000000000000000000000000000;
cells_preset[64*2 :64*2+63 ] <= 64'b0000000001101010000000001000000000000000001101010000000000000000;
cells_preset[64*3 :64*3+63 ] <= 64'b0000000000000000000000010100000000000000001101010000000000000000;
cells_preset[64*4 :64*4+63 ] <= 64'b0000000000000110000001100000000000011000000000110101000000000000;
cells_preset[64*5 :64*5+63 ] <= 64'b0000000000001000100001100000000000011000000000000000000000000000;
cells_preset[64*6 :64*6+63 ] <= 64'b0110000000010000010001100000000011010100000000000000000000000000;
cells_preset[64*7 :64*7+63 ] <= 64'b0110000000010001011000010100000000011010100000000011010100000000;
cells_preset[64*8 :64*8+63 ] <= 64'b0000000000010000010000000100000000000000000011010100000000000000;
cells_preset[64*9 :64*9+63 ] <= 64'b0000000000001000100000000000000000000000000000000000000000000000;
cells_preset[64*10:64*10+63] <= 64'b0000000000000110000000000000000011010100000000000000011010100;
cells_preset[64*11:64*11+63] <= 64'b0000000000000000000000000000000000000000011010100000000000000000;
cells_preset[64*12:64*12+63] <= 64'b0000000000000000000000000110101000000000000000000000000000000000;
cells_preset[64*13:64*13+63] <= 64'b0000000000000000000000000110101000000000000000000110101000000000;
cells_preset[64*14:64*14+63] <= 64'b0000000000000000000000000110101000000000011010100000000000000000;
cells_preset[64*15:64*15+63] <= 64'b0000000001101010000000000000000011010100000000011010100000000000;
cells_preset[64*16:64*16+63] <= 64'b0000000000000000000011010100000000000000000011010100000000101010;
cells_preset[64*17:64*17+63] <= 64'b0000000000000000000000000110101000000000000000000110101000000000;
cells_preset[64*18:64*18+63] <= 64'b0110101000000000011010100000000011010100000000011010100000000000;
cells_preset[64*19:64*19+63] <= 64'b0000000001101010000000001101010011010100000000011010100000000000;
cells_preset[64*20:64*20+63] <= 64'b0000000000000000000000000110101000000000000000000000000000000000;
cells_preset[64*21:64*21+63] <= 64'b0000000000000000011010100000000000000000011010100000000000000000;
cells_preset[64*22:64*22+63] <= 64'b0000000000000000011010100000000110000000011000000000110101000000;
cells_preset[64*23:64*23+63] <= 64'b0000000000000000000000000000001010000000011011010100000000000000;
cells_preset[64*24:64*24+63] <= 64'b0000000011000000011000000000001100000000011010100000000000000000;
cells_preset[64*25:64*25+63] <= 64'b0000000011000000101000000000000000011010100000000000000000000000;
cells_preset[64*26:64*26+63] <= 64'b0000000000000000110000001100000000000000000011010100000000000000;
cells_preset[64*27:64*27+63] <= 64'b0000000000000000000000001010111010100000000000000000000000000000;
cells_preset[64*28:64*28+63] <= 64'b0000000001101010000000001000000000000000001101010000000000000000;
cells_preset[64*29:64*29+63] <= 64'b0000000000000000011010100000000000000000001101101010000000000000;
cells_preset[64*30:64*30+63] <= 64'b0000000000000000011010100000000011010100001010000000000000000000;
cells_preset[64*31:64*31+63] <= 64'b0000000000000000011010100000000000000000001000000000110101000000;
cells_preset[64*32:64*32+63] <= 64'b0000000000000000000000000110101000000000000000000110101000000000;
cells_preset[64*33:64*33+63] <= 64'b0000000000000000011010100000000000000000011010100000000000000000;
cells_preset[64*34:64*34+63] <= 64'b0000000001101010000000000000000111000000000000000000000000000000;
cells_preset[64*35:64*35+63] <= 64'b0000000000000000011010100000000010000000000000000000000000000000;
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cells_preset[64*41:64*41+63] <= 64'b0000000000000000011010100000000000000000000000000000000000000000;
cells_preset[64*42:64*42+63] <= 64'b0000000000000000000000000000000000000000011010100000000000000000;
cells_preset[64*43:64*43+63] <= 64'b0000000000000000000011010100000000000000001101010011010100000000;
cells_preset[64*44:64*44+63] <= 64'b0110101001101010000000001101010000000000000000000000000000000000;
cells_preset[64*45:64*45+63] <= 64'b0000000001101010000000001101010011010100110101000000000000000000;
cells_preset[64*46:64*46+63] <= 64'b0110101001101010011010100110101001101010011010100110101000000000;
cells_preset[64*47:64*47+63] <= 64'b0110101001101010011010100000000011010100000000000000000000000000;
```
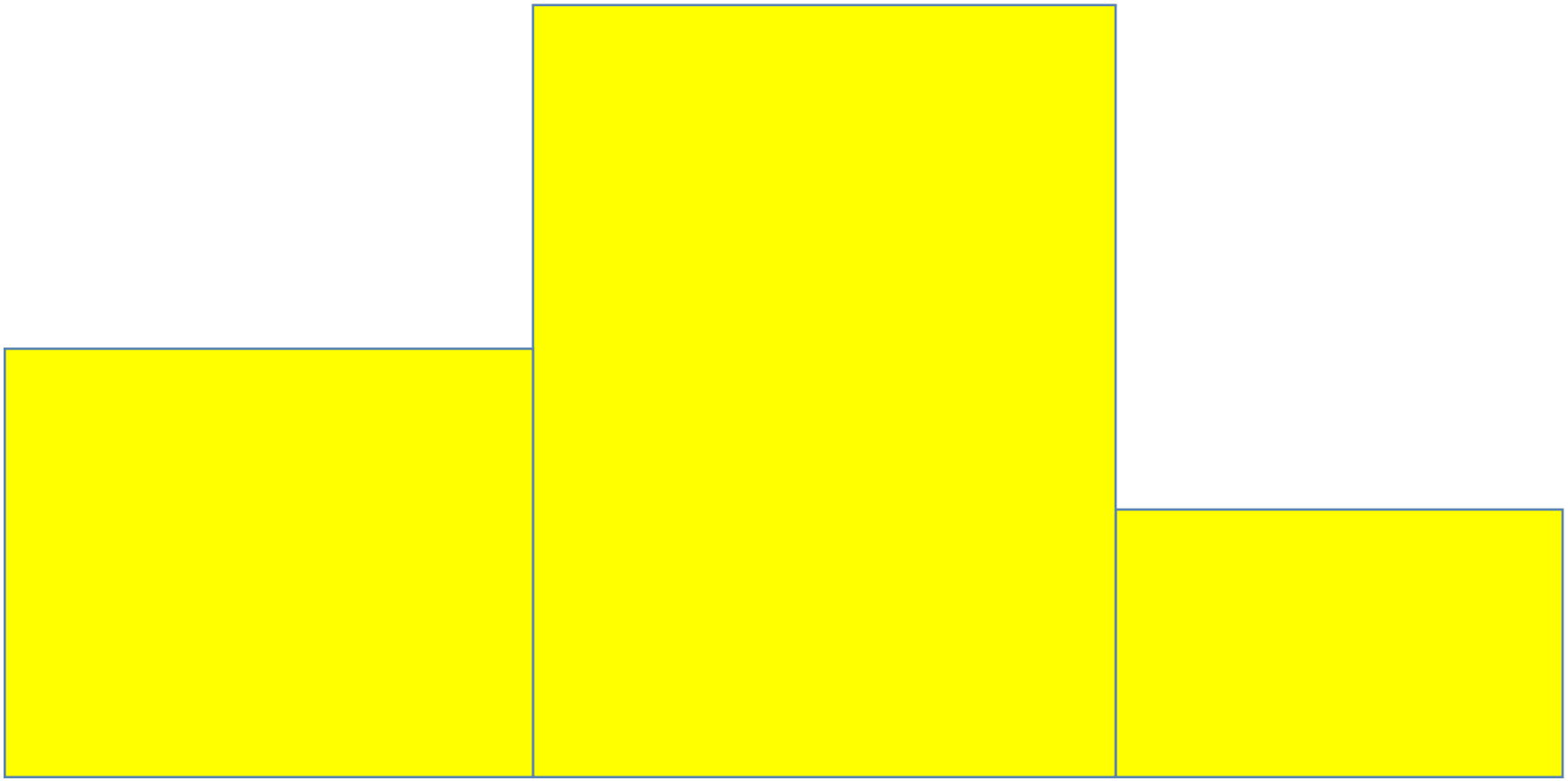
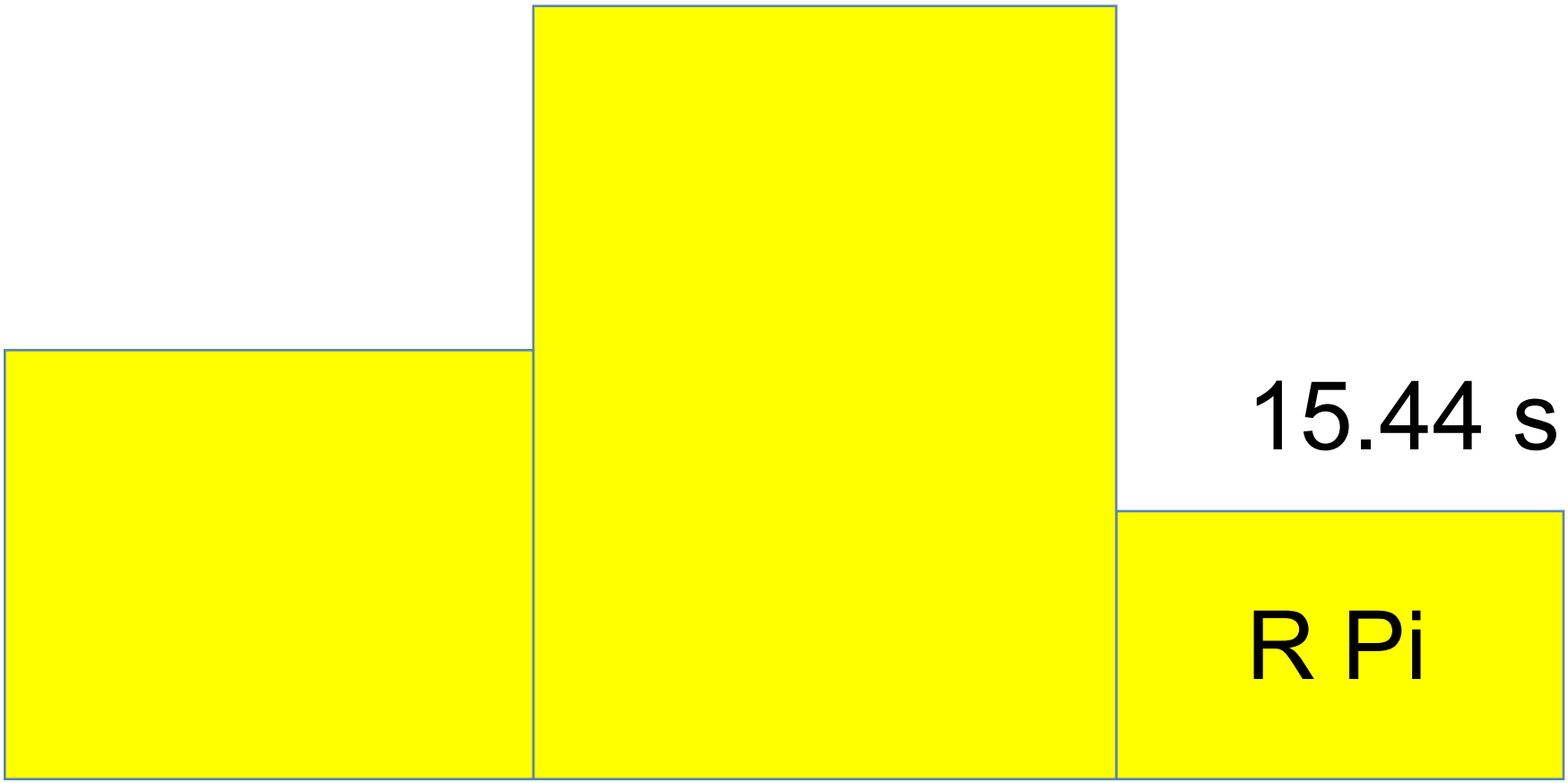
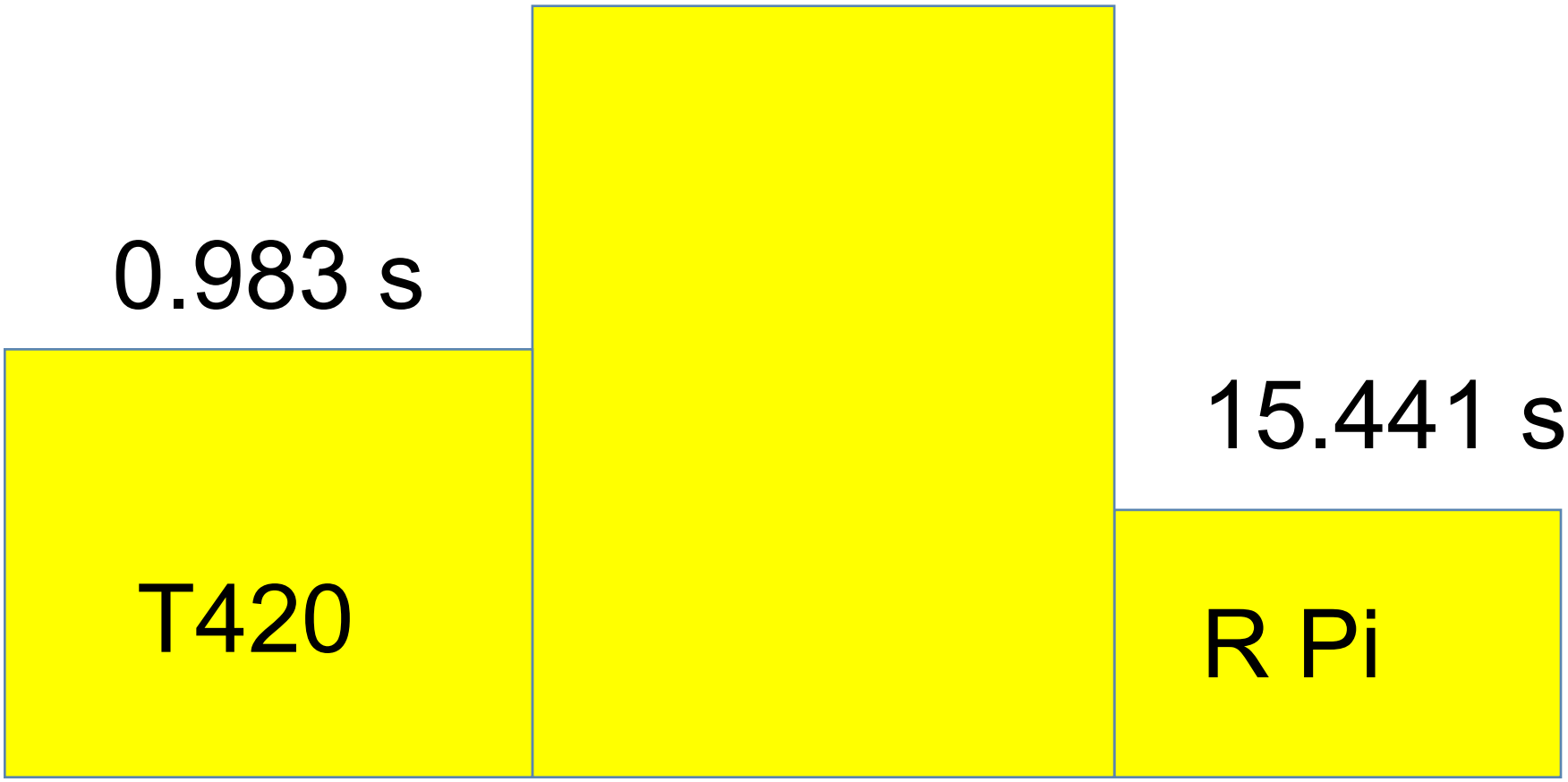

# srednji kvadratici

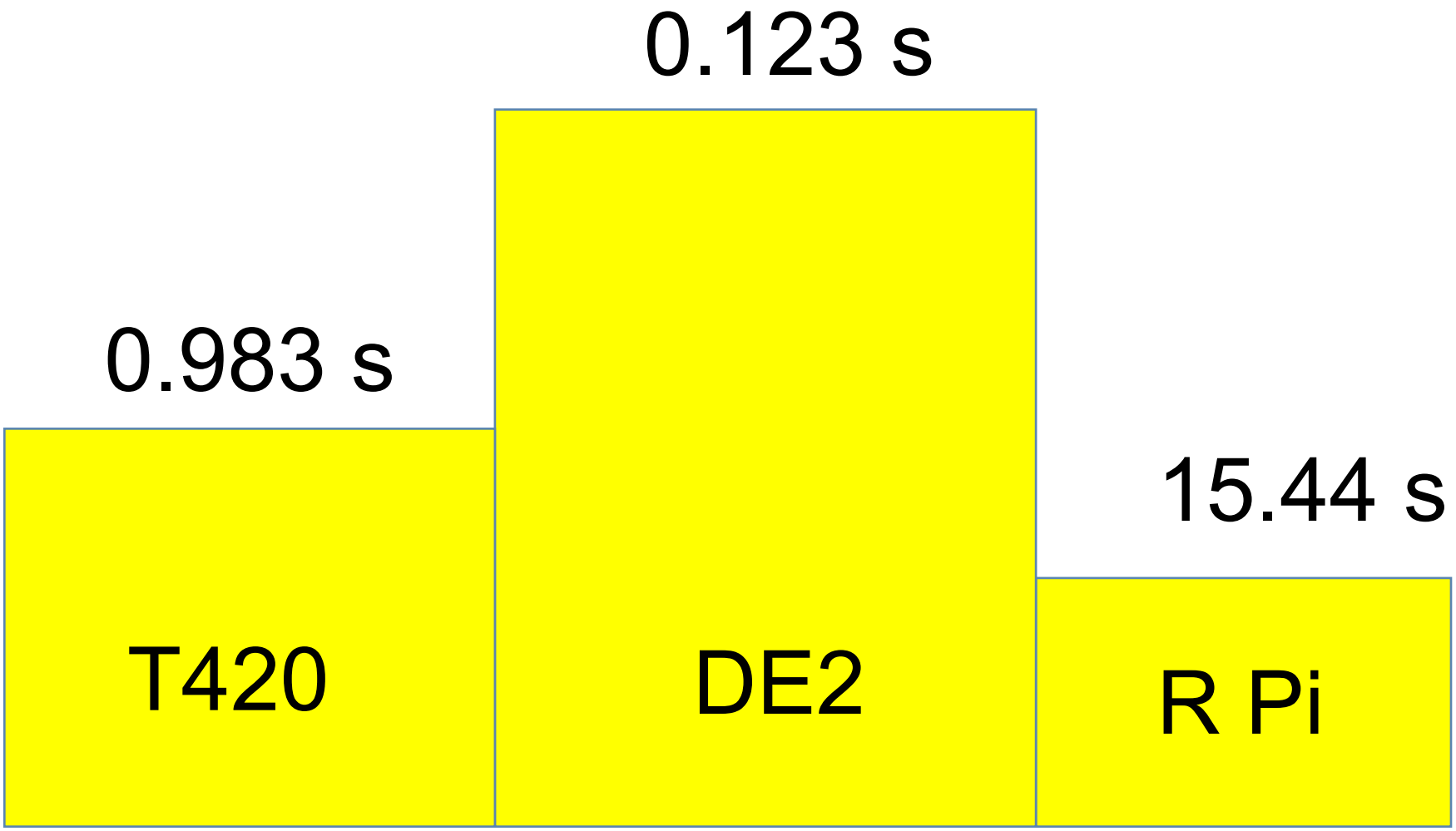
```
begin
    // Middle squares
      population <= cells_preset[i - 64 - 1] +
                    cells_preset[i - 64] +
                    cells_preset[i - 64 + 1] +
                    cells_preset[i - 1] +
                    cells_preset[i + 1] +
                    cells_preset[i + 64 - 1] +
                    cells_preset[i + 64] +
                    cells_preset[i + 64 + 1];
end
```

# 8 specijalnih slucaja




15.44 s
R Pi


0.983 s
15.441 s
T420
R Pi


0.123 s
0.983 s
15.44 s
T420
DE2
R Pi

DE2 = 8x T420

DE2 = 128x RPi