POST LAB 1 – ALEX DUNKER

7.1 Sensor Detector

Truth Table

Combination (4,3,2,1)	Logic
0000	0
0001	1
0010	0
0011	1
0100	0
0101	1
0110	1
0111	1
1000	0
1001	1
1010	1
1011	1
1100	0
1101	1
1110	1
1111	1

K-map

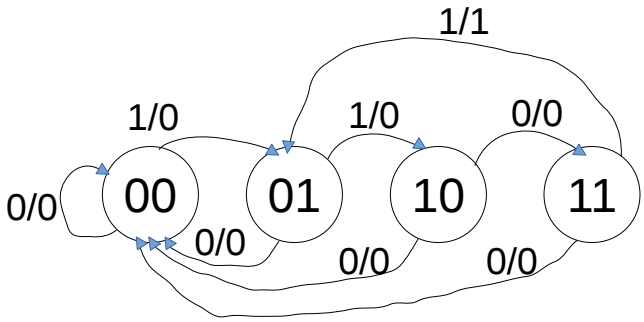
	S1		S1'		
S2	1	1	1	0	S3'
	1	1	1	1	S3
S2'	1	1	0	0	
	1	1	0	0	S3'
	S4'	S4		S4'	

SOP Equation

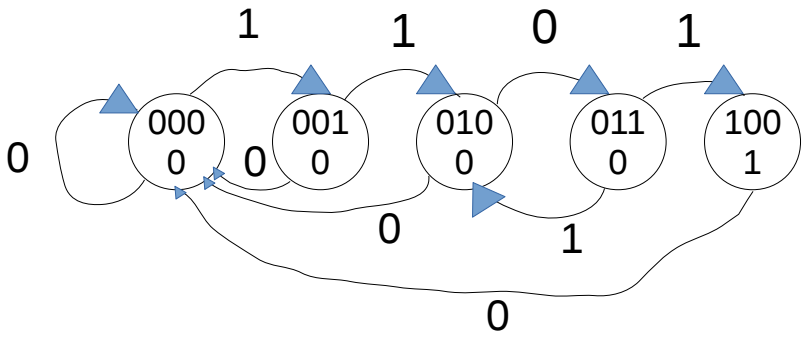
F(S1,S2,S3,S4) = S1 + S3 * S2 + S4 * S2

7.2 “1101” Detector

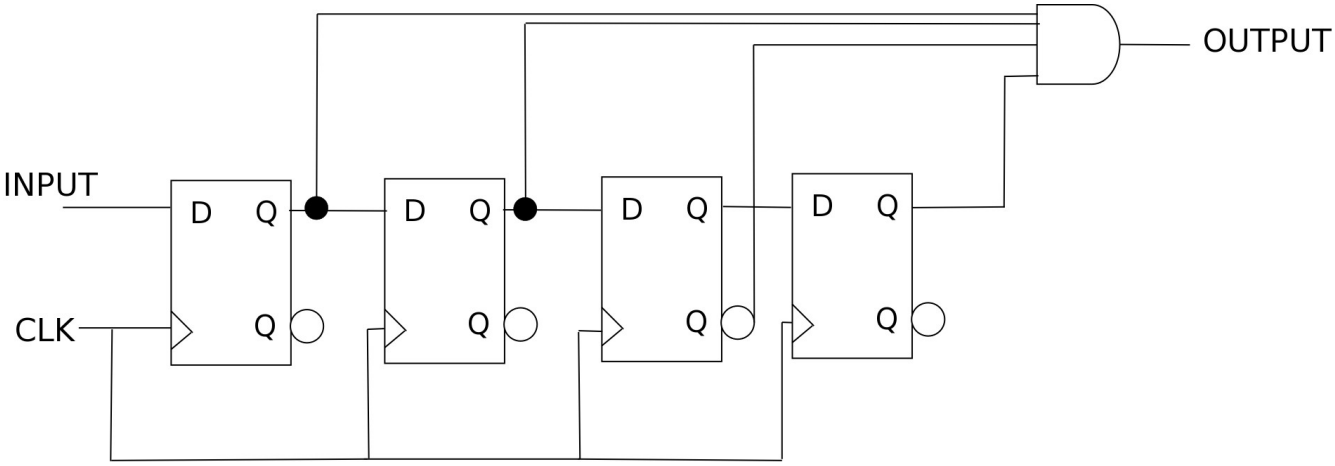
Mealy State Machine



Moore State Machine



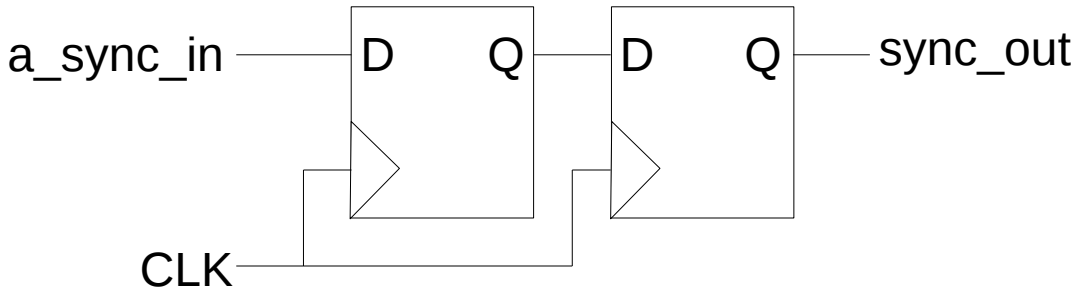
Moore Schematic (in place of diagram)



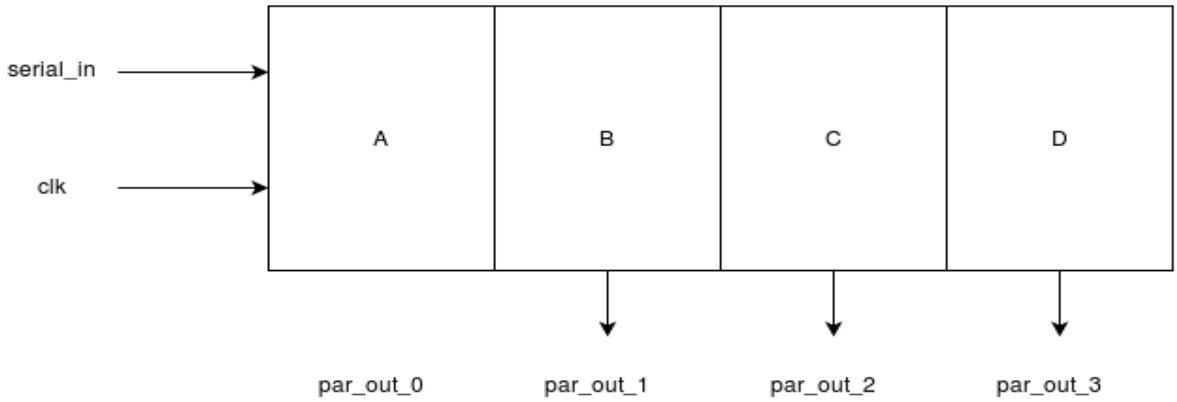
7.3 Hardware Building Blocks

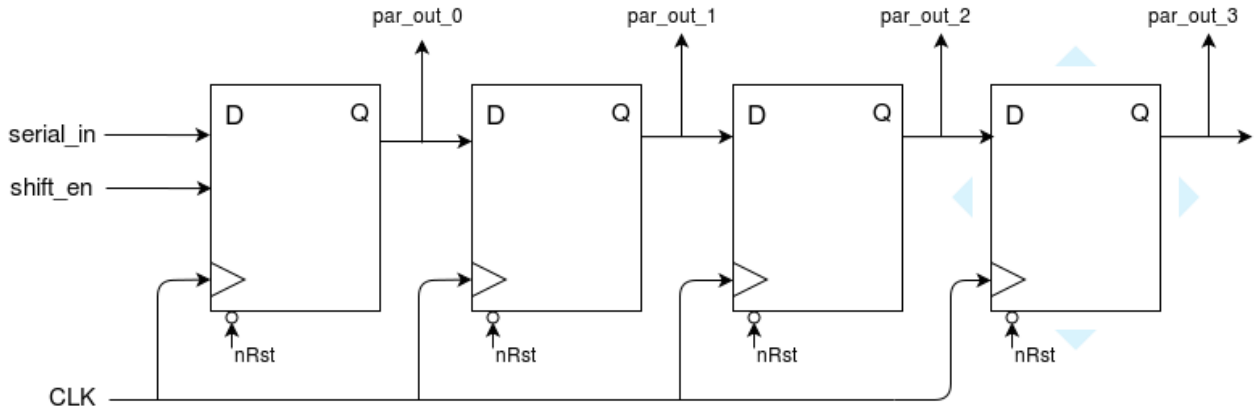
7.3.1 Synchronizer

Schematic diagram of a 2 Flip-Flop synchronizer:



7.3.2 Most Significant Bit First Serial to Parallel Shift Register





7.3.3 Most Significant Bit First Parallel to Serial Shift Register