Andrew Jeddeloh

github.com/ajeddeloh jeddelog.com

andrew.jeddeloh@gmail.com
(503) 806-3536

3410 California Street
Berkeley, CA 94703

Objective Senior Software Engineer position developing embedded and bare metal systems
Skills / Tools Go, C, Python, ARM assembly, Git, Linux, LaTeX

Work Experience:

Red Hat Inc. Senior Software Engineer — Spring 2019 - Winter 2020
Software Engineer — Spring 2018 - Spring 2019

- Developed and maintained Fedora CoreOS and Container Linux (formerly CoreOS Linux)
- Led development of Ignition, a declarative first-boot configuration utility, and its incorporation into Fedora CoreOS's initramfs environment
- Built the Fedora CoreOS Config Transpiler, a tool for generating Ignition configuration from a human-readable YAML format
- Streamlined the Fedora CoreOS build process, halving build time and improving predictability while removing dependencies
- Presented on the Fedora CoreOS build process and boot process at DevConf.cz in Brno, Czech Repulic and DevConf.us in Boston, MA

CoreOS Inc. Software Engineer — Summer 2017 - Spring 2018
Software Engineering Intern — Summer 2016

- Developed and maintained Container Linux, Ignition, and related tooling
- Investigated and fixed Container Linux bugs in upstream projects, such as systemd

Intuit - Software Engineer Co-op — Summer 2015 - Fall 2015

- Expanded prototype co-browsing technology for supporting customers
- Worked on prototype app for proactively managing your finances

Intel - Software Development and Validation Intern — Summer 2014

- Helped port the Intel RealSense SDK to Android
- Designed and wrote an OpenGL renderer and camera view API for non-standard video formats

Personal Projects:

STM32 Inductance meter *Aug 2020* — jeddelog.com/posts/stm32-lmeter

- C project to measure inductance using the STM32L476G microcontroller's DAC and ADC
- Uses Fourier analysis and linear regression to reduce noise and improve precision
- Successor to my python script to control my function generator and oscilloscope to do the same thing (github.com/ajeddeloh/lrc)

Software S/PDIF Decoder *May 2021* — jeddelog.com/posts/soft-spdif

- C project decoding S/PDIF in software on the STM32L476G
- Implements software clock recovery and biphase mark decoding

VueScan Reverse Engineering *Dec 2020* — jeddelog.com/posts/vuescan-autofocus

- Wrote a shim to intercept calls to Epson's proprietary V550 scanner plugin
- Used the shim to determine that VueScan's (scanning software) autofocus feature is nonfunctional
- Featured on Hackaday

Education

Rochester Institute of Technology — 2013 - 2017

- Computer Science Major / Computer Engineering Minor
- Cumulative GPA: 3.98
- Computer Science House Member (csh.rit.edu)