II B. E (Electronics & Telecommunication) **2024033**

December 2023 Examination

Sub: 3ETRC2 Digital Electronics

Time: 3 hrs. **Max Marks: 60**

Note: Attempt all five questions. Attempt any two part of each question. All questions carry equal marks.

Q.1	a) (i)	Determine the value of base r1 and r2, if $(121)_{r1} = (100)_{r2}$ and $(34)_{r1} = (41)_{r2}$. Base of the numbers r1 and r2 are positive integers.	3
	a)(ii)	Perform following subtraction using 2's complement (8 bit number) subtraction 68 - 95. Also give answer in 8 bit 2's complement form.	3
Q.1	b) (i)	A code has four-bit code word has following valid codes. 0001,0010,0100,0111,1000,1011,1101,1110. How many errors can be detected in this code? Give reason for your answer.	3
	b)(ii)	Following sequence is received at the receiver of a system. 1010 0110 1011. It is given that the sequence contains 8 bit of message and coded in Hamming code. Determine message. (Correct it if required.)	3
Q.1	c) (i)	What are open collector gates? Explain the concept of Wired AND operation.	3
	c) (ii)	Draw and explain the working CMOS Inverter gate.	3
Q.2	a)(i)	Obtain the minimal expression in SOP form for $F(a,b,c,d) = \Sigma m(0,1,2,3,5,7,8,9,11,14)$ using K-Map method. Draw the NAND-NAND circuit.	3
	a) (ii)	Using K-map method obtain NOR-NOR circuit for following function and draw the circuit. $F(a,b,c,d) = \pi M(1,4,6,9,10,11,14,15)$	3
	b) (i)	Prove that. $((AB'+ABC)'+A(B+AB'))' = 0$	3
	b) (ii)	Prove that if $AB'+A'B = C$, then $AC'+A'C = B$	3

P.T.O.

c)(i) Implement the following multiple output combinational circuit using a 3 line to 8 line decoder.

$F_1 = \sum m(0,1,5,7)$

$F_2 = \sum m(2,5,6,7)$

$F_3 = \sum m(0,3,4,6)$

c(ii) Implement following expression using appropriate multiplexer. **3**

$f_1(a,b,c,d) = \Sigma\, m(0,2,3,6,8,9,12,14)$ **3**

Q.3 a) Design a full adder circuit using only NAND gates. Also draw the circuit.

b) Design negative edge triggered T-flip-flop with an active low PRESET and CLEAR asynchronous input. **6**

c) Design a four-bit parity generator circuit. Also design a parity checker circuit to check the output generator circuit. **6**

Q.4 a) Design a negative edge triggered mod-13 asynchronous up counter using JK-flip-flop. **6**

b) Design a synchronous counter goes through states 0, 5, 4,2,0… . Is this counter self-starting? Use negative edge triggered T flip-flops. **6**

c) Design a combinational circuit to convert a R-S flip-flop to T-flip-flop. **6**

Q.5 a) Explain working 4 bit switched current source type D/A converter. If logic 1 = 5V and Logic 0 =0V, then determine analog value of digital input 1010. **6** **6**

b) An 8-bit successive approximation type ADC has resolution of 10 mV. What is the digital output for analog value 1.62V **6**

c) Design a Schmitt trigger circuit using 555 timer IC. **6**