FPGA RADIATION HARDENING

By

Name: Ajmal M Ali

Roll No: 02

Guide: Mr. Jagadeesh Kumar P

INTRODUCTION

- Reduction in Size and Power results in increased sensitivity to Radiation.
- Reconfigurable components are sensitive to single event upset (SEU) induced soft errors
- Error in memory may result in a range of potential effects.

Contd..

- Various techniques have been developed to harden CMOS logic against SEU.
- Techniques like Triple Modular Redundancy (TMR), Scrubbing.
- Difficult to justify the cost in terms of area and power compared to the level of extra robustness achieved by the techniques.

Contd..

- Silicon on insulator (SOI) technology
- The active silicon layer is separated from an underlying substrate by a layer of insulating material.
- Complete electrical isolation
- Provides
  - resistance to radiation,
  - low gate and interconnect capacitance,
  - high noise immunity and
  - relative insensitivity to voltage variation.

RADIATION EFFECTS

- Reduction in size and operating voltages in IC technology, makes Radiation effect severe.
- Potentially affecting both the physical structure as well as its functionality.
- Radiation effects can be divided into two:
  - Total ionization dose (TID)
  - Single event effect (SEE)

TOTAL IONIZATION DOSE (TID)

- Cumulative effect due long-term exposure to protons and neutrons.
- High energy electrons or protons pass through a device and produce electron-hole pairs
- This interact with its gate and field oxide.
- Changes the threshold voltage and mobility of the transistors, thereby changing their characteristics.

SINGLE EVENT EFFECT (SEE)

- Change of state in a memory cell or register due to single ion/particle interaction.
- With the amount of charge representing the stored information dropping, the sensitivity to single particle charge collection is also increasing.
- SEUs are now the biggest contributor to soft errors in many modern CMOS technologies.

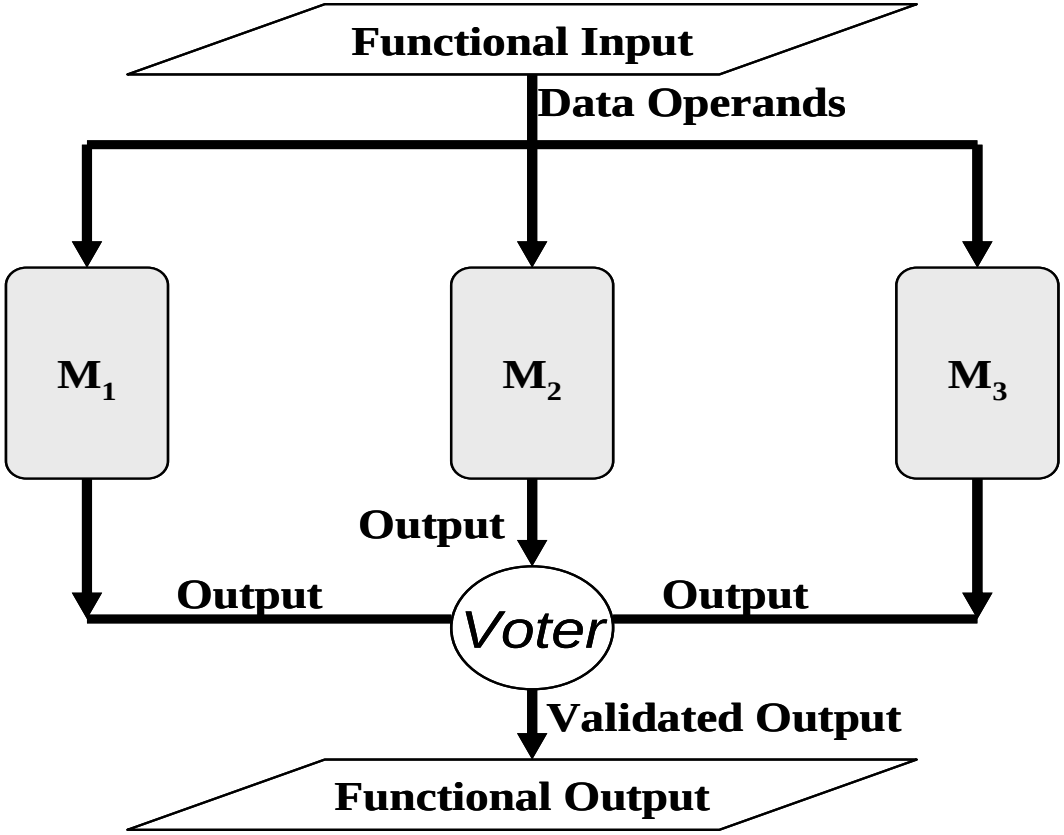
RADIATION HARDENING

- Techniques used to harden an overall design against soft errors are known as mitigation techniques.
- FPGA devices includes regular arrays of programmable memory.
- Any upset in the configuration memory can be catastrophic as it may change the operation.

SCRUBBING

- Involves checking the memory, detecting an error, and rewriting the correct data in the right memory location.
- Three scrubbing techniques are in common use:
  - Read-back with correction upon error detection;
  - Internal configuration access port (ICAP) and FRAME ECC cores;
  - Blind writes (also called blind scrubbing).

TRIPLE MODULAR REDUNDANCY(TMR)



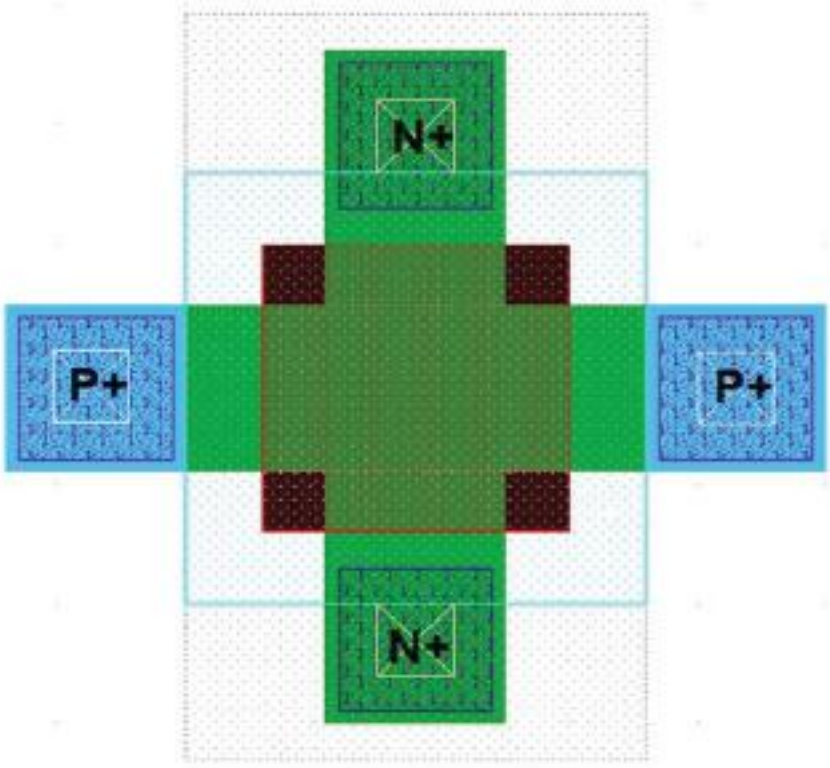
SILICON ON INSULATOR

- SOI technology is more radiation resistant.
- When the Insulating layer is Sapphire(Al_2O_3), it is called Silicon On Sapphire.
- Complete electrical isolation is created between active devices, and between the devices and the substrate

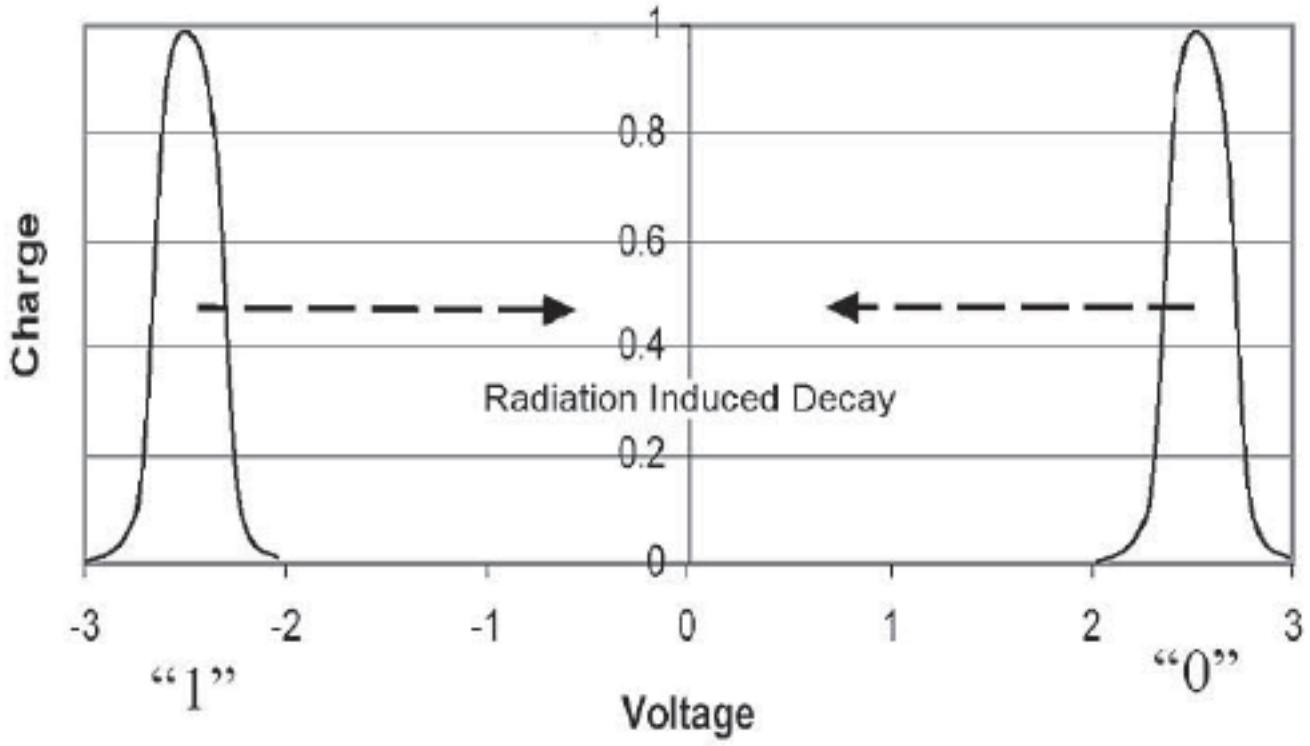
SILICON ON SAPPHIRE EEPROM

- The EEPROM cell comprises a pair of cross coupled nMOS and pMOS transistor with common floating gate.
- The floating gate can be charged positive or negative via the injection of either holes or electrons.
- Rather than just the presence or absence of charge on the gate both logic levels are established, indicating the programmed logic value.

SILICON ON SAPPHIRE EEPROM



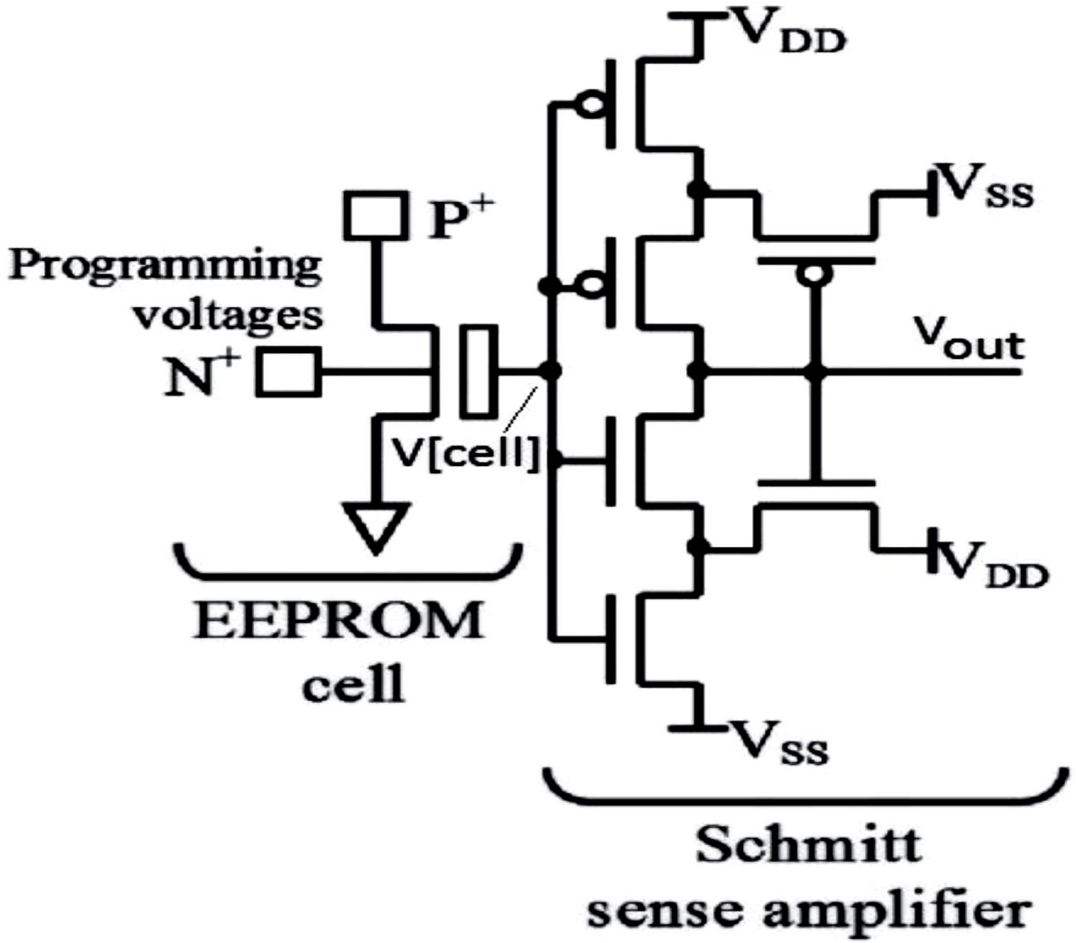
CHARGE STORAGE CHARACTERISTICS



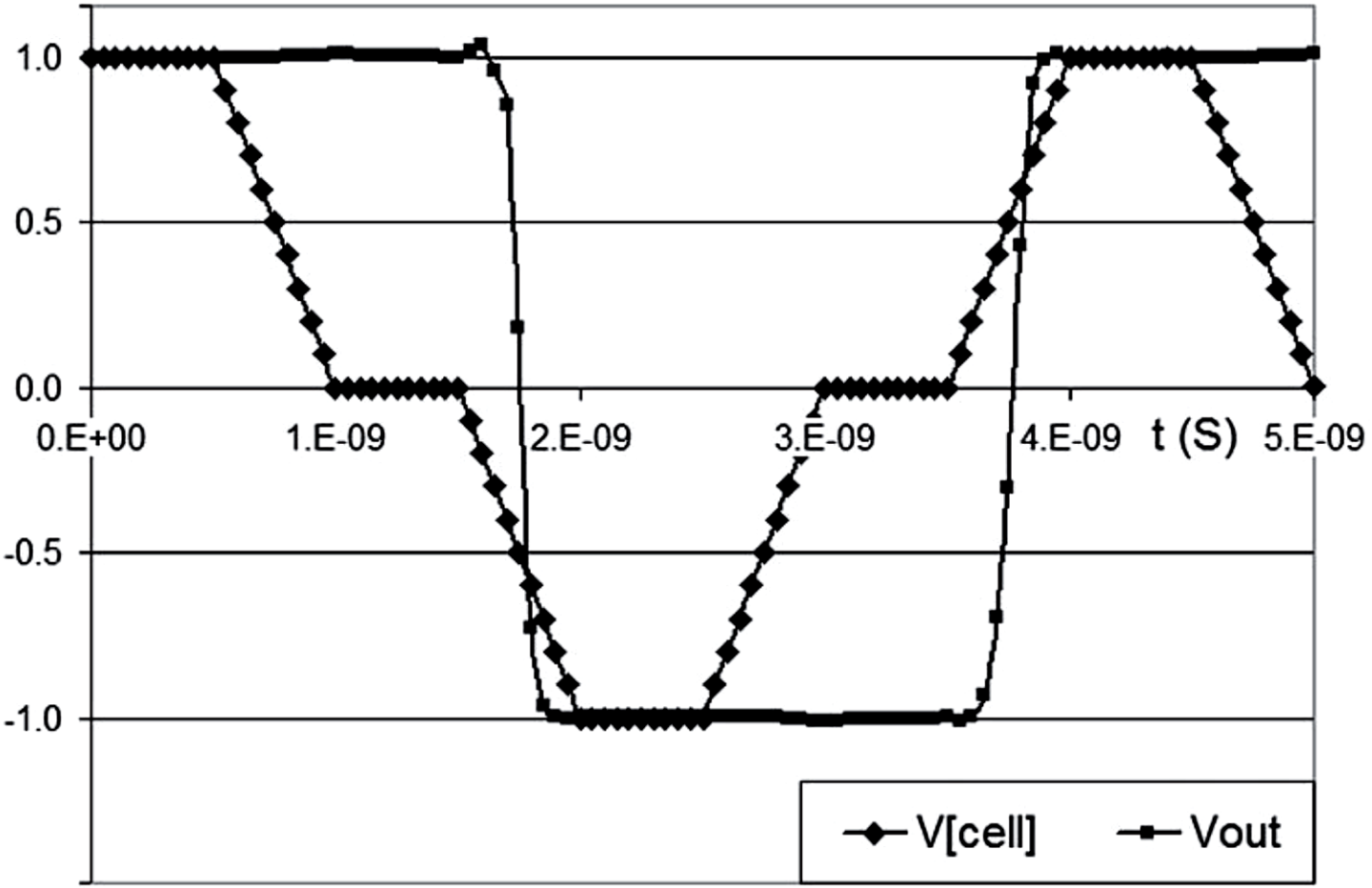
EEPROM CONFIGURATION CELL

- The floating EEPROM gate is integrated with a simple built-in sense amplifier($V_{DD}/2$).
- The Schmitt sense amplifier offers two main advantages
  - The hysteresis of the Schmitt will ensure the correct output logic value is maintained.
  - A particle strike will increase the static current of the Schmitt sense amplifier

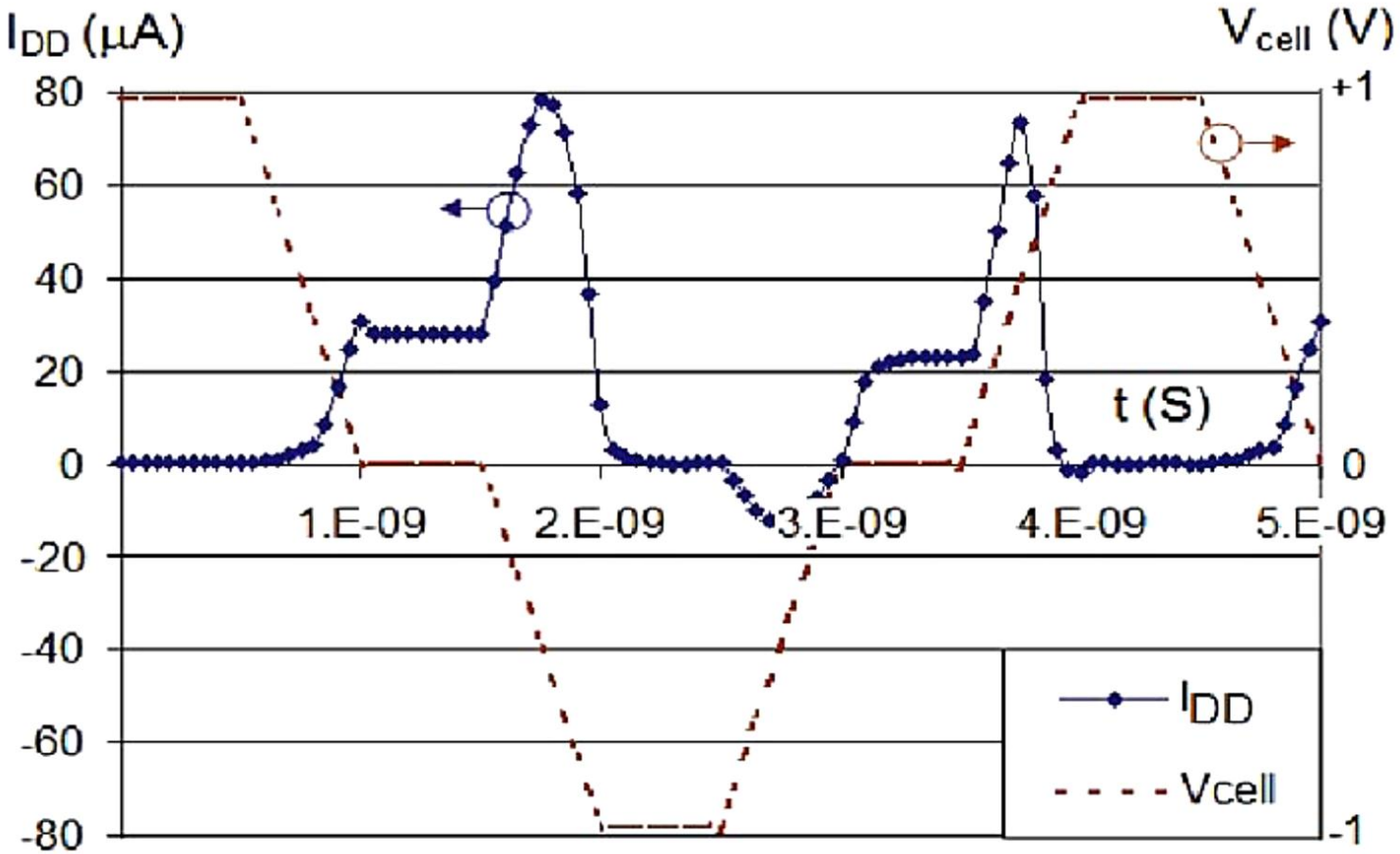
EEPROM CONFIGURATION CELL



DC CHARACTERISTICS



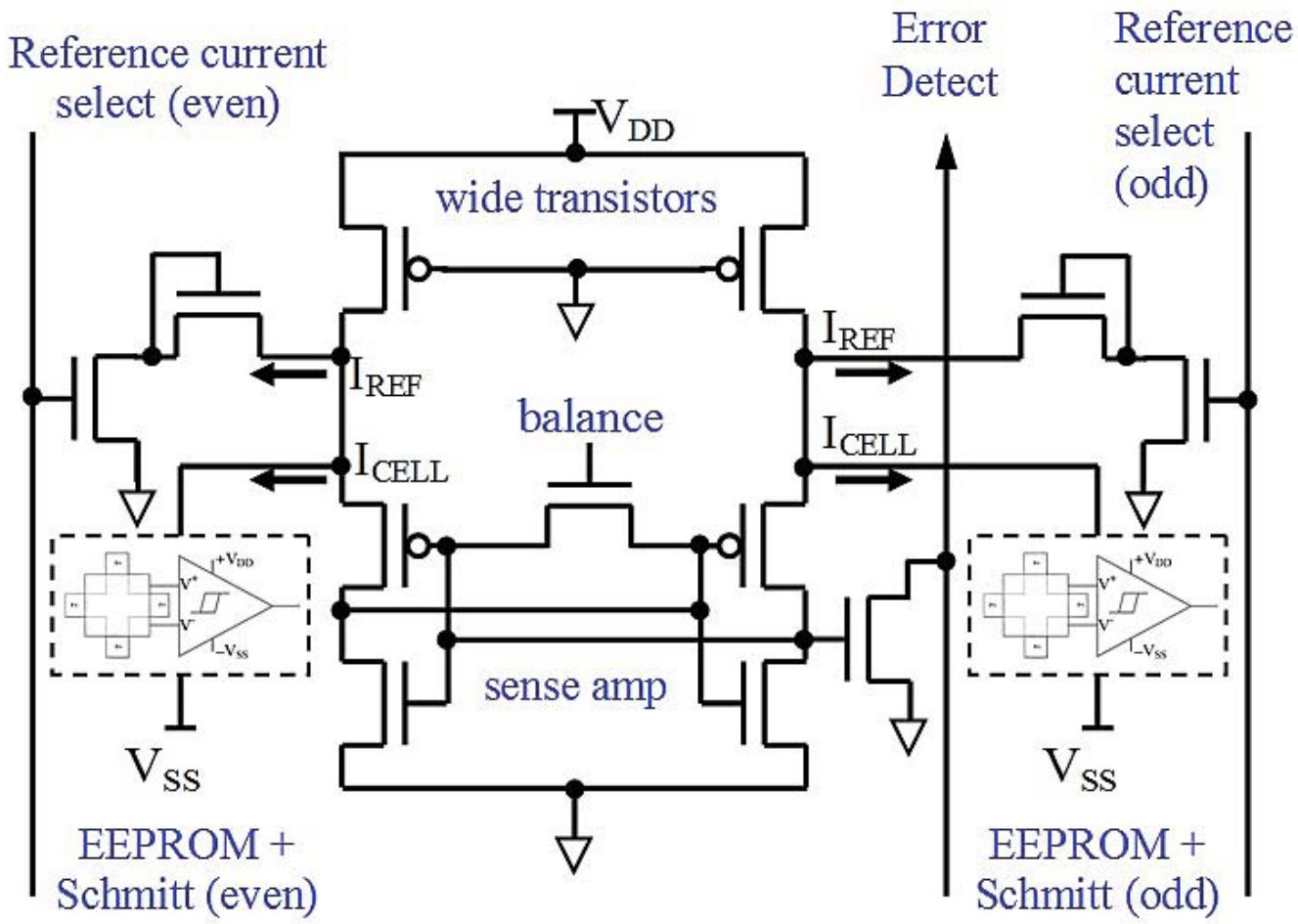
STATIC CURRENT BEHAVIOUR



CURRENT SENSING

- Large increase in current arises in the Schmitt when EEPROM cell suffers an upset.
- A conventional cross-coupled current sensor can be set up to compare the supply current with a reference current.
- The large difference between the currents to be sensed means that an error could be readily detected.

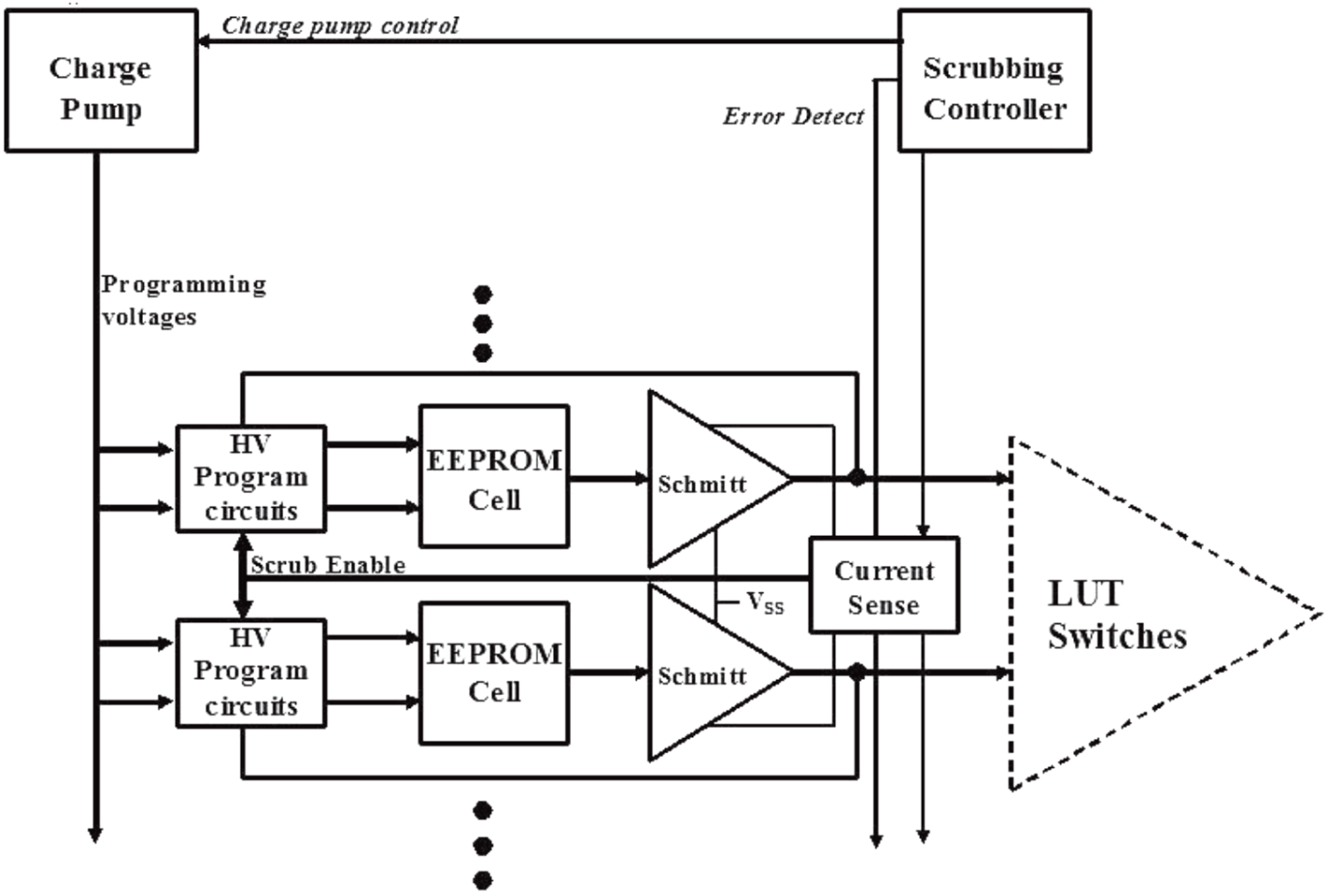
CURRENT SENSING



AUTO-SCRUBBING

- Allows individual configuration memory cells to be monitored and scrubbed when a SEU is detected.
- This behaviour is called auto-scrubbing.

AUTO-SCRUBBING



DRAWBACKS

- While resistant to isolated particle strikes, it is still possible for a sequence of two events to permanently upset the configuration value.
- An error will occur only when two particles with charge above the critical charge hit the EEPROM and the Schmitt within the same write window

CONCLUTION

- Various techniques have been developed to harden CMOS logic against SEU.
- Difficult to justify the cost in terms of area and power compared to the level of extra robustness achieved by the SOS.

REFERENCES

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[2] K. Haque and P. Beckett, “A SOI EEPROM based configuration cell with simple scrubbing detection,” in *Proc. 24th Int. Conf. VLSI Design*, Jan. 2011, pp. 24–29

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