ABSTRACT

Continuous reduction in size and power of CMOS transistors have resulted in their increased sensitivity to radiation effects. With the amount of charge representing the stored information dropping at successive technology nodes, the sensitivity of CMOS devices to single particle charge collection is increasing. The configuration memories within reconfigurable components, such as EEPROM-based FPGA are particularly vulnerable to radiation-induced single event effects. The Seminar presents a Silicon on Insulator (SOI) based configuration memory system for use in a radiation hard reconfigurable system. A non-volatile storage cell, able to be manufactured in a standard single Polysilicon SOI CMOS process with no special layers, is combined with a Schmitt amplifier. A simple current detector of the type used in conventional RAM circuit allows the configuration memory to be setup to exhibit self-correcting, or "Auto Scrubbing" behaviour which results in a final structure that exhibit characteristics enhancing its resistance to radiation. Other circuit design techniques have been used to make systems more radiation tolerant, it is often difficult to justify the cost in terms of area and power compared to the level of extra robustness achieved by the techniques.