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E_E 466 LAB Assignment 2

Six- Transistor SRAM cell

1. The three width values (WPTR, WP, WN)
   - WPTR = 200
   - WP = 1200
   - WN = 600

2. A short description on how I found the width values.

   Initially, I considered the WP and WN ratio, and I used the symmetrical CMOS Inverter design as the basis for calculating the ratio between WP and WN, where the beta ratio for a CMOS inverter with one PMOS and NMOS is equal to 1, meaning that the W/L ratio of the PMOS is equivalent to two or three times the W/L ratio of the NMOS.

   By guessing the values for WP, starting from values below 100n, I noticed that the waveform output for Y drops too quickly. So, I increased the value of WP to a larger value starting from 500n, and I noticed that at above 1000n for WP and keeping WN to half of WP, the output Y wasn't dropping too quickly as it did before.

   Thus, for the inverters W/L ratios:

$$\frac{W}{L}_{\text{PMOS}} = 2\frac{W}{L}_{\text{NMOS}}$$

$$\frac{1200}{45} = \frac{600}{45}$$

$$26.66 = 13.33$$

   Also, while toggling the values of WP, I kept WTRN and WN the same; I observed that the rise delay for Y was bigger than 500ps. So, decreasing the value from 500n helped reduce the rise delay of Y.

3. A screenshot showing the waveforms: