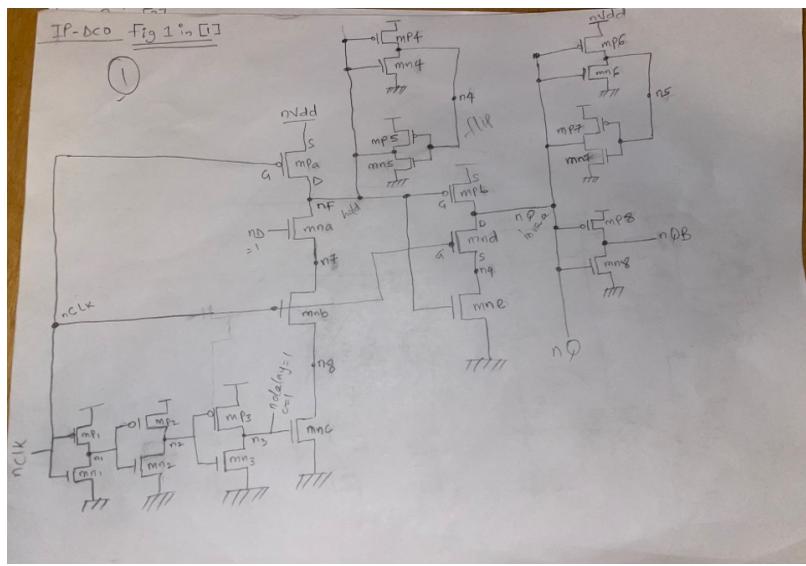


# Ajeigbe Oluwafemi J. E\_E 466 Final Project, Fall 2021.

## **1. The Implicit Pulsed Data Close to Output flip-flop (ip-DCO)**

**a. Circuit Diagram-Transistor Design:**



**b. Operation of the ip-DCO as per the circuit-transistor design:**

The flip-flop consists of two parts, a clock ( $nClk$ ) and a latch for data storage ( $nF$ ). This flip flop uses Inverters 6 & 7 to latch data, while it uses inverters 4 and 5 to hold the internal node signal. The clock signal is inverted and applied as the input of to the pulse generator to generate a transparent window that is equal to the delay of the inverter stacks at the input (Inverters 1,2,3). It is a semi-dynamic flip flop in that the internal node  $nF$  should be 1 before evaluation.

### 1. When nClk = 0

$$\begin{aligned} m_{pa} &= nF = m_{nc} = m_{ne} = 1 \\ m_{nb} &= m_{nd} = m_{pb} = 0 \end{aligned}$$

Therefore, since  $m_{pb}$  and  $m_{nd}$  is 0,  $nQ$  cannot charge to 1 or discharge to 0.

## 2. When nClk changes from 0 to 1

$m_{nc} = 0$  (after some delay)

mnb = mnd = 1 (as nClk changes to 1)

mpa = 0, If nD = 1, nF will be discharged to 0 and as such mpb = 1 thus charging nO to 1 while if nD changes to 0, nF will remain at 1 after some delay (due to the

inverter stack holding the internal node signal). Then, mpb will become 0 while mnd and mne will be open to discharge nQ to zero.

That is:

When nClk changes from 0 to 1 and nD = 1 , nQ = 1,

When nClk changes from 0 to 1 and nD changes from 1 to 0, nQ = 0

### 3. When nClk = 1

After certain delay, mnc goes off (as the nClk is inverted at n3)

mnc = mpa = 0, thus nF is floating (not charging or discharging). So, no matter the change of nD at this window, nQ will not change.

### c. Waveform and delays:



Rise Delay for nQ: 34.1p

Fall Delay for nQ: 11.9p

Rise delay for nOb: 71p

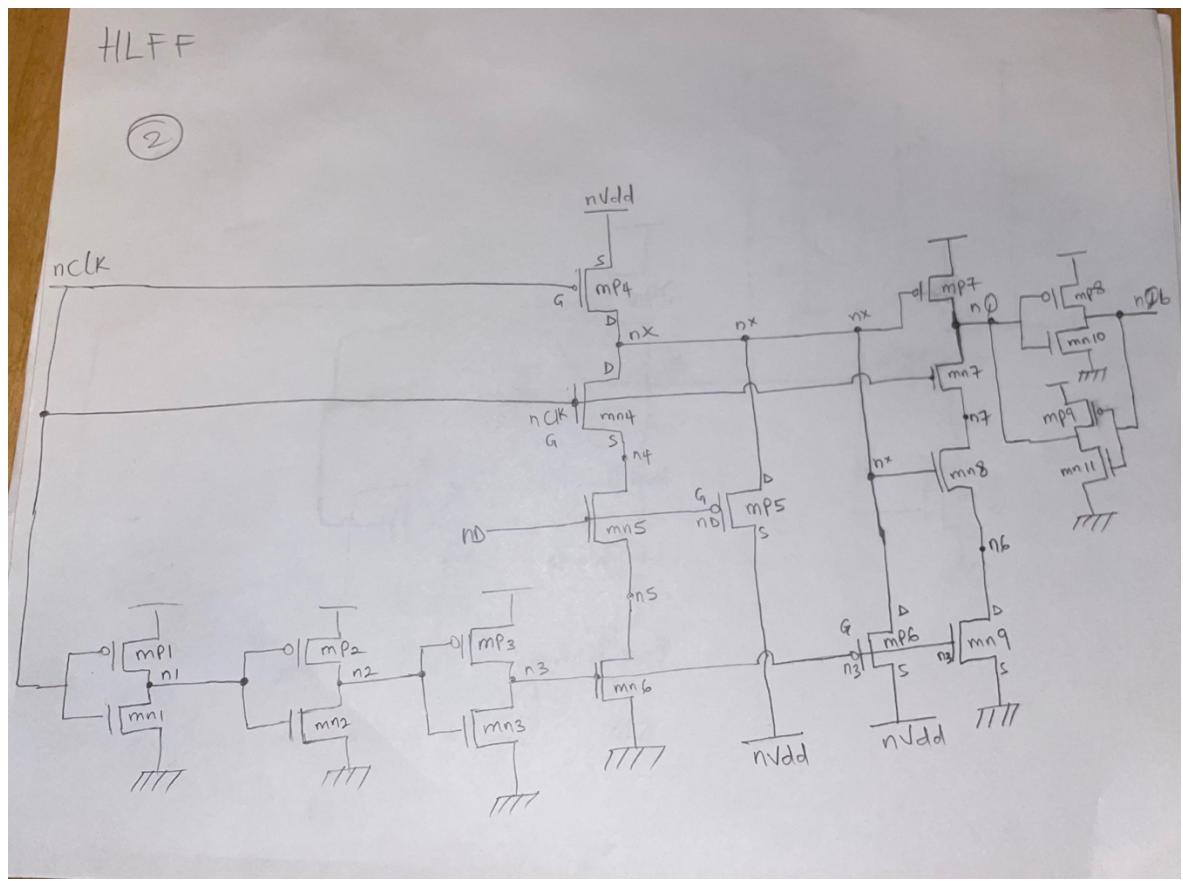
Fall delay for nOb: 32p

### d. Power Consumption: 1.2673e-05

### e. Total Device Area: L (1305) x W (3085) = 4965525n

## 2. Hybrid Latch-Flip Flop

### a. Circuit Diagram-Transistor Design:



### b. Waveform and delays:



Rise Delay for nQ: 54.2p

Fall Delay for nQ: 70.8p

Fall delay for nOb: 43.3p

Rise delay for nOb: 55.3p

c. **Operation of the HLFF as per the circuit-transistor design:**

The HLFF provides a soft clock edge while minimizing the effects of clock skew created by capturing the input signal using an implicit brief pulse. This is a semi-dynamic type of flip flop.

1. When  $nClk = 0$

$mp4 = nX = mn6 = mn8 = mn9 = 1$

$mn4 = mp6 = mp7 = mn7 = 0$

2. When  $nClk$  changes from 0 to 1

$mp4 = 0$

$mn4 = mn7 = 1$

$mn6 = mn9 = 0$  after a certain delay

$mp6 = 1$  after a certain delay.

In this window, the  $nD$  state is important:

If  $nD = 0$ ,  $mn5 = 0$ .

$mp5$  will open to keep the state of  $nX$  at 1. Thus, discharging  $nQ$  through  $n7$ ,  $n6$  to the ground as  $mp7$  will be disconnected (disconnecting  $nQ$  from  $nVdd$ ).

so,  $nQ = 0$ .

If  $nD = 1$ ,  $mn5$  will open thus discharging  $nX$  to 0.  $mp7$  will then open to charge  $nQ$  to 1

Thus:  $nD = nQ$  in this window.

3. When  $nClk = 1$ ,

$mp4$  will be closed, at this window,  $nX$  will not be charged or discharged.

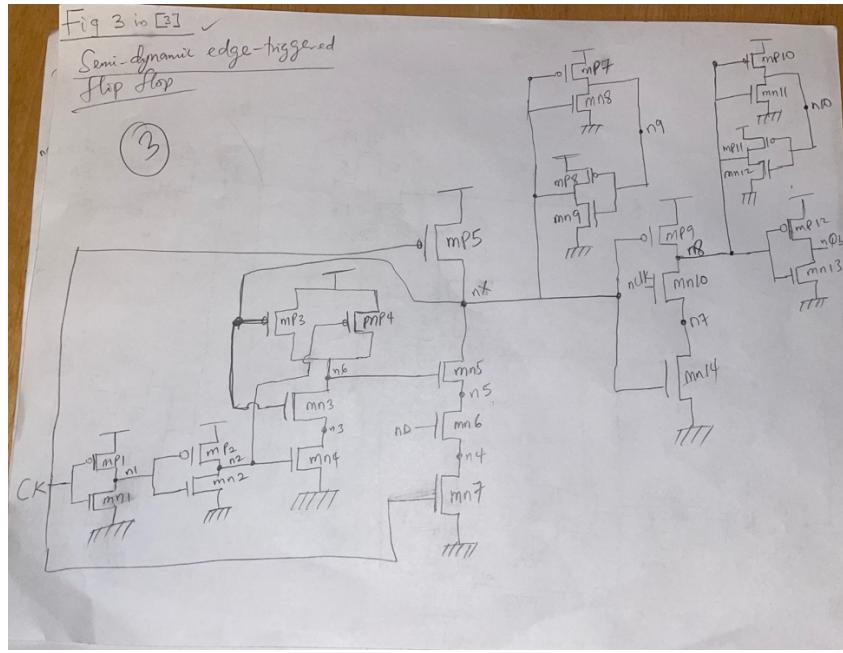
Also,  $mp6$  will open as  $nClk = 1$ .  $mp7$  will be closed because of this. There will be no path to charge or discharge  $nQ$ . That means at this window, no matter the change in  $nD$ , the signal from  $nD$  cannot pass through to  $nQ$ .

d. **Power Consumption:** 1.0252e-05

e. **Total Device Area:** L (1830) x W (2245) = 4108350n

### 3. Semi-dynamic edge triggered flip flop

#### a. Circuit Diagram-Transistor Design:



#### b. Waveform and delays:



Rise Delay for nQ: 27.7p  
Fall Delay for nQ: 11.2p

Fall delay for nOb: 32.6p  
Rise delay for nOb: 71.7p

**c. Operation of the Semi-dynamic Flip Flop as per the circuit-transistor design:**

This flip flop uses a NAND gate to reduce the width of the sampling window; this reduces the hold time. It is also a semi-dynamic flip flop, thus it needs the nD signal to charge or discharge its output.

1. When  $nClk = 0$ , Note that  $nQ = n8$  per my circuit.

At this window,

$mp5 = nx = 1$ ;  $nX$  is charged to 1 through  $mp5$ .

The output of the NAND gate will be 1 so  $mn5$  is open. Although,  $mn7$  will be closed as  $nClk = 0$ .

$mp9$  will be closed, thus disconnecting  $n8$  from  $nVdd$ . At this time as well,  $mn10$  will be closed as  $nClk = 0$ . Disconnecting  $n8$  from the Ground.

Therefore, in this window,  $n8$  does not change.

2. When  $nClk$  changes from 0 to 1,

$mn7$  will open,  $mp5$  will close.  $mn5$  will remain open for some delay.

$nX$  will hold the charged signal (1) from when  $nClk$  was 0, as such  $mp9$  will remain close for a certain delay.

Here, the state of  $nD$  is important.

If  $nD$  is set to 0 at this window,  $mn10$  and  $mn14$  will open then discharging  $n8$  to 0. While if  $nD$  is set to 1,  $nX$  will be discharged through  $mn5$ ,  $mn6$ ,  $mn7$ . Then  $mp9$  opens while  $mn14$  closes; thus, charging  $n8$  to  $nVdd$ .

So  $nD = nQ$  at this window.

3. When  $nClk = 1$

At this point,  $nX$  is disconnected from  $nVdd$  and Gnd.

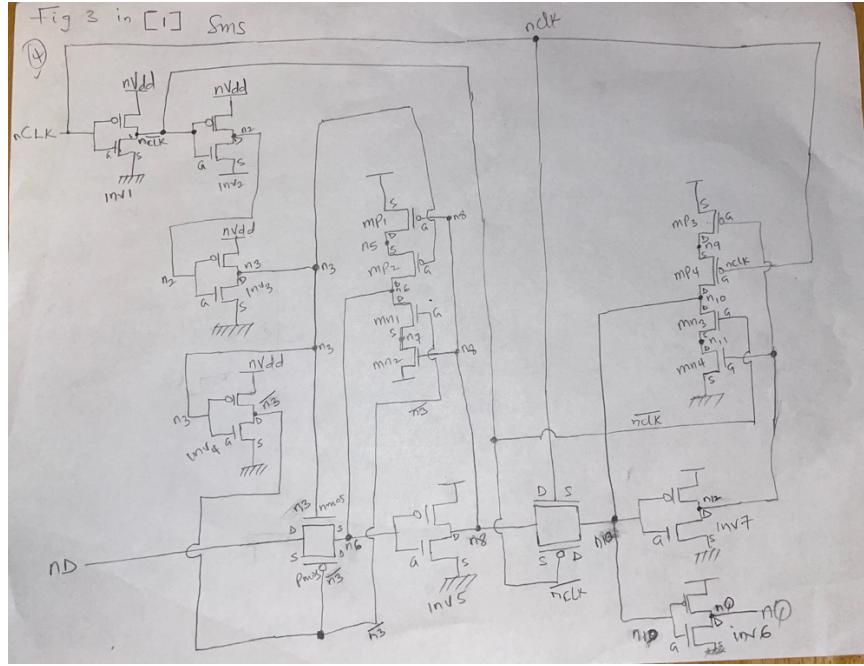
$Mp5$  will be closed and  $mn5$  will also be closed, thus disconnecting  $nQ$  from the internal node. Thus  $nQ$  will not change no matter the state of  $nD$ .

**d. Power Consumption: 1.0951e-05**

**e. Total Device Area: L (1305) x W (3800) = 4959000n**

#### 4. Time-borrowing static master-slave

##### a. Circuit Diagram-Transistor Design:



##### b. Operation of the tb-SMS as per the circuit-transistor design:

The tb\_SMS has a static structure (no charge). It achieves a transparency window through an implicitly generated pulse (the transmission gates). It has two edges: the master and slave edges. Thus, D passes to Q at the positive edge. Two stages will be controlled by the master and slave edges.

###### 1. When nClk = 0:

Since the input 4 stacks of transistors does not invert nClk input, the first transmission gate is open (both mtg1p and mtg1n is open) allowing the nD (1 or 0) signal to pass through to n6. If nD = 1 during this window, the inverter 5 will invert the signal so n8 = 0, this stage will be stored. Same as when nD = 0

The second transmission gate is closed (mtg2p and mtg2n) at this stage.

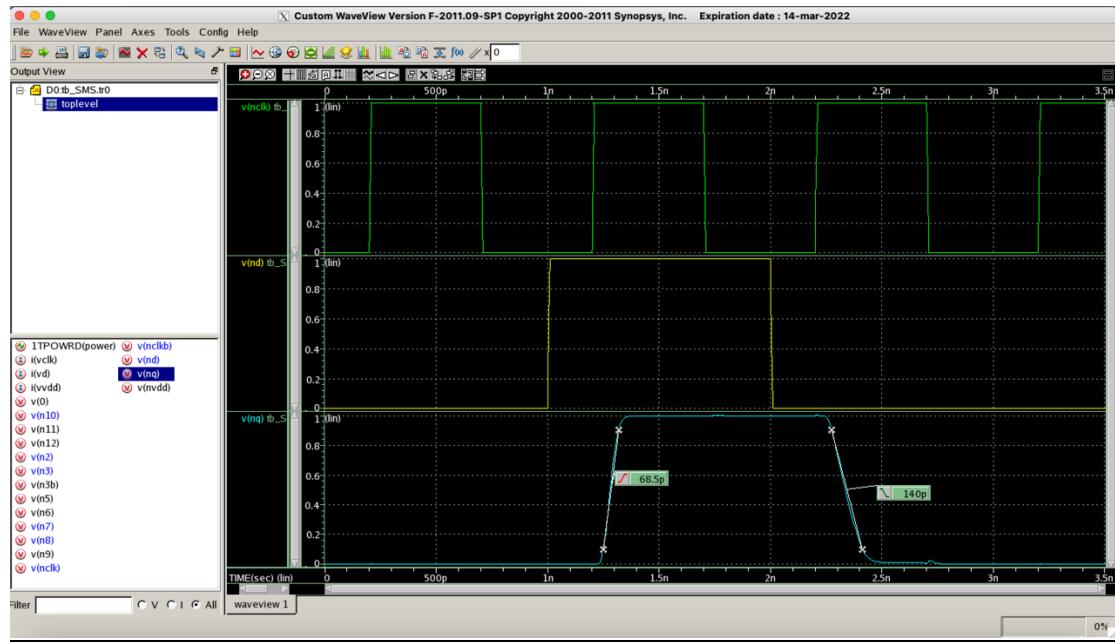
###### 2. When nClk switches from 0 to 1:

At this window, the first transmission gate will close after some delay, (thus, the first transmission gate will be open for some little delay) and the second transmission gate will be open. As such, nD signal will pass through to nQ at this stage. (nD = nQ)

3. When nClk = 1:

After a certain delay, the first transmission gate will close. nD signal cannot pass through. Although the second transmission gate will be open, nD signal cannot go through node 6. Thus, nQ does not change.

c. **Waveform and delays:**



**Rise Delay for nQ:** 68.5p

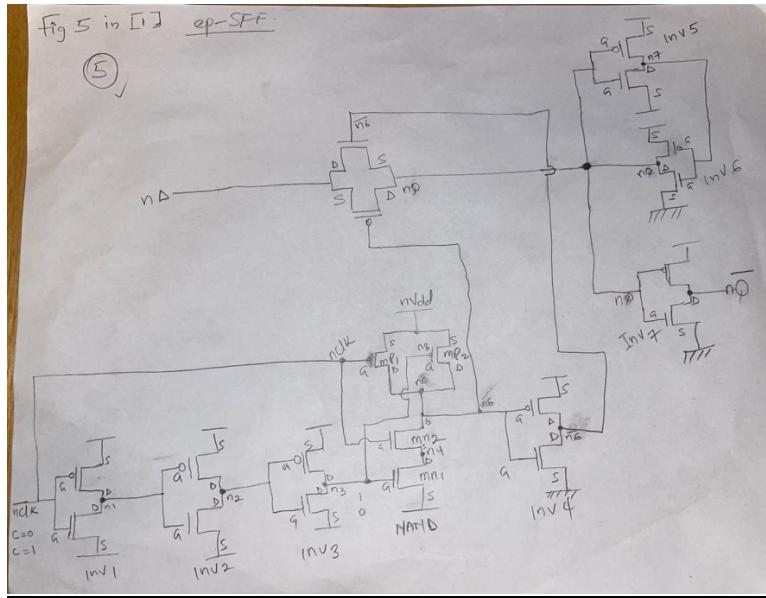
**Fall Delay for nQ:** 140p

d. **Power Consumption:** 2.1182e-05

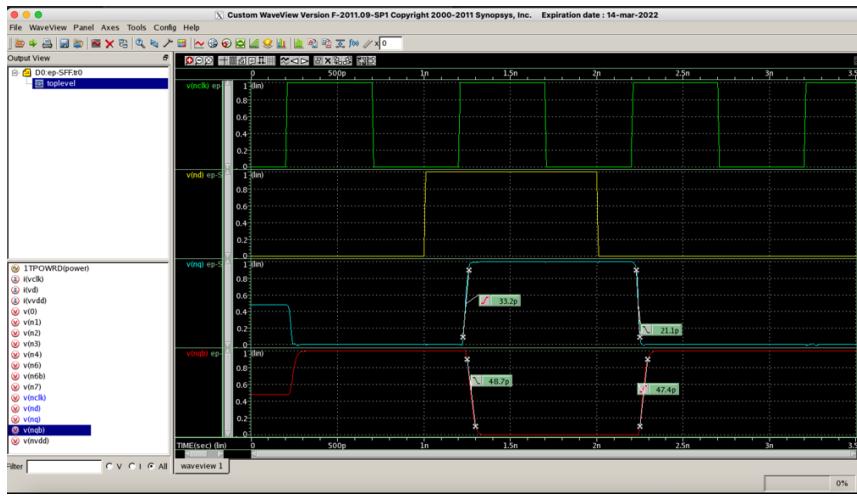
e. **Total Device Area:** L (1530) x W (6835) = **10457550n**

## 5. Explicit-pulsed semi-dynamic flip-flops

### a. Circuit Diagram-Transistor Design:



### b. Waveform and delays:



When nClk is 0, the first input of the NAND gate will be 0 and the second input of the NAND gate will be 1, the output of the NAND gate will be 1, the PMOS and NMOS of the transmission gate will be closed. At this window, nD will not pass through to nQ.

2. When nClk changes from 0 to 1:

The value of the first output from the generated by the stack of inverters at the input will be stored for some delay, thus when nClk changes from 0 to 1 both inputs of the NAND gate will be 1 for some certain delay as such, the output of the NAND gate will be zero. The PMOS and NMOS of the transmission gate will open to allow nD to pass to nQ.

nD passes to nQ only at this window.

3. When nClk = 1:

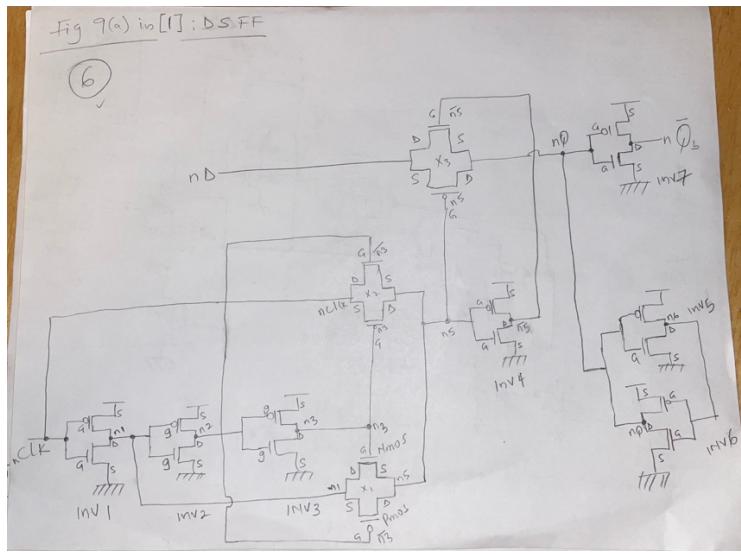
When nClk is 1, the first input of the NAND gate will be 1 and the second input of the NAND gate will be 0, the output of the NAND gate will be 1, the PMOS and NMOS of the transmission gate will be closed. At this window, nD will not pass through to nQ.

d. **Power Consumption:** 1.1492e-05

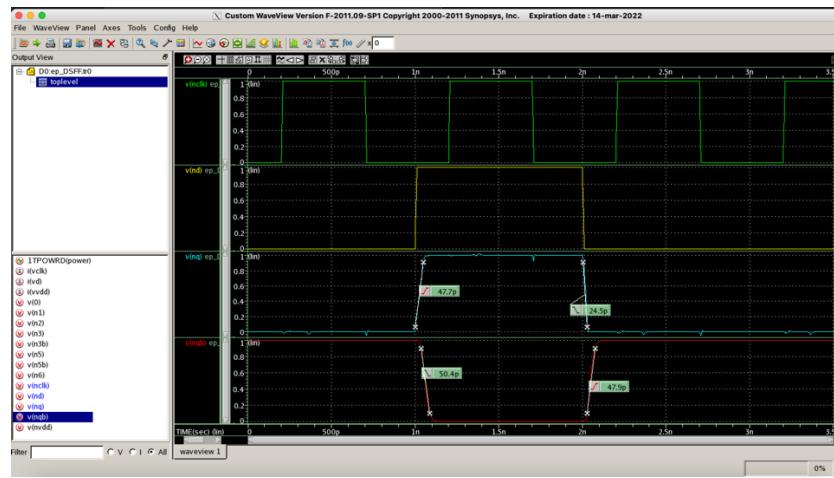
e. **Total Device Area:** L (1170) x W (2900) = 3393000n

## 6. Explicit-Pulsed Dual Edge-Triggered Flip Flop:

### a. Circuit Diagram-Transistor Design:



### b. Waveform and delays:



Rise Delay for  $nQ$ : 47.7p  
Fall Delay for  $nQ$ : 24.5p

Rise delay for  $nQ_b$ : 50.4p  
Fall delay for  $nQ_b$ : 47.9p

### c. Operation of the ep-DSFF as per the circuit-transistor design:

1. When  $nClk = 0$

After the second and third inversion of the nClk signal, the first transmission gate will open to allow 1 to pass through to node 5. The third transmission gate will be closed as both the NMOS and PMOS will not open.

Also, when nClk = 0, the second transmission gate is closed. So, only the signal through the first transmission gate goes through to the third transmission gate.

2. When nClk changes from 0 to 1,

After a series of signal inversion, the second transmission gate will open after a certain delay, and the first transmission gate will close after some delay. Note that the first transmission gate's signal will allow 0 to pass through to node 5 for a little time. The signal will now pass through to node 5. The third transmission gate will then open to allow nD pass through to nQ. nQ will only open at this window after a certain delay.

3. When nClk = 1,

The first transmission gate X1 will close and the transmission gate X2 will open to allow the nClk signal (1) pass through to node 5. The third transmission gate will then close since a 1 is being passed through X2 to node 5. Thus, the nD signal will not be able to pass to nQ.

d. **Power Consumption:** 3.2814e-05

e. **Total Device Area:** L (1170) x W (7475) = 8745750n