

Name: Ajita Shree

Indian Institute of Technology Kanpur  
CS637 Embedded and Cyber-Physical SystemsRoll No 20111262  
e.g. 170001Dept. Computer Science Engineering  
e.g. CSE

Homework Assignment 2

Deadline: October 11, 2020

## Instructions:

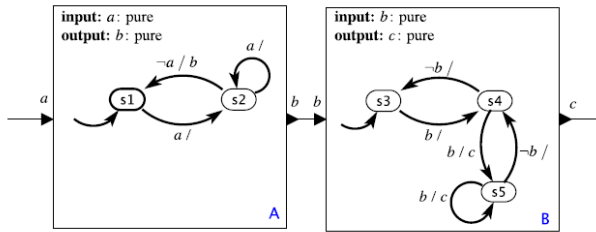
Total: 40 marks

1. This question paper contains a total of 9 pages (9 sides of paper). Please verify.
2. Write your name, roll number, department, section on **every side of every sheet** of this booklet
3. Write final answers **neatly** in the given boxes.

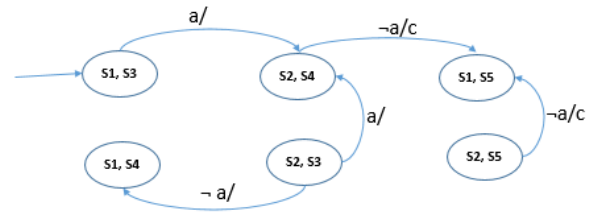
**Problem 1.** (10 points) Problem 3 in the Exercises of Chapter 5 in [LS15]. [LS15] Edward A. Lee and Sanjit A. Seshia, Introduction to Embedded Systems, A Cyber-Physical Systems Approach, Second Edition, <http://LeeSeshia.org>, ISBN 978-1-312-42740-2, 2015.

## Answer

We need to create a state machine C representing the synchronous composition of state machine A and B and identify the states that are not reachable. Below diagram shows the representation of synchronous state machine C. As per the definition,  $States_c = States_a * States_b$ , and the outgoing edges from these states will be as follows:



State Machine A and B



State Machine C

- **{s1, s3}**: edge to {s2, s4} with condition a/ (as s1 → s2, a/; s3 → s4, b/). Transition to {s1, s5}, {s1, s4}, {s2, s3}, {s2, s5} does not exist as edges doesn't exist for both the states in A as well as B.
- **{s2, s4}**: edge to {s1, s5} with condition ¬a/c (as s2 → s1, ¬a/b; s4 → s5, b/c)
- **{s1, s5}**: No out-edge possible; two candidate set but update condition will fail i.e. edge to {s2, s5} not possible because s1 → s2; a/ and s5 → s5; b/c; edge to {s2, s4} not possible because s1 → s2/a and s5 → s4; ¬b/
- **{s1, s4}**: no out-edges; **{s2, s5}**: edge to {s1, s5} with condition ¬a/c (as s2 → s1, ¬a/b and s5 → s5, b/c)
- **{s2, s3}**: edge to {s2, s4} with condition a/ (as s2 → s2, a/ and s3 → s4, b/); edge to {s1, s4} with condition ¬a/ (as s2 → s1, ¬a/b; s3 → s4, b/)

The number of unreachable states in the state machines are 3 i.e. {s1, s4}, {s2, s3}, {s2, s5}

Name:

**Indian Institute of Technology Kanpur**  
**CS637 Embedded and Cyber-Physical Systems**

**Roll No**   
e.g. 170001

**Dept.**   
e.g. CSE

**Homework Assignment 2**  
*Deadline:* October 11, 2020

---

Name: Ajita Shree

Indian Institute of Technology Kanpur  
CS637 Embedded and Cyber-Physical SystemsRoll No 20111262  
e.g. 170001Dept. Computer Science Engineering  
e.g. CSE

Homework Assignment 2

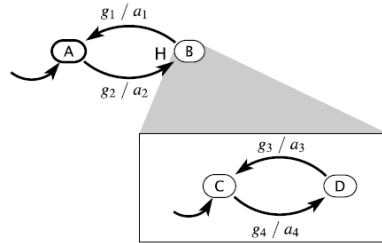
Deadline: October 11, 2020

**Problem 2.** (10 points) In the hierarchical state machine in Figure 5.17 of [LS15], suppose that the transition from state B to state A is a preemptive transition. Construct an equivalent flat finite state machine giving the semantics of the hierarchical state machine.

[LS15] Edward A. Lee and Sanjit A. Seshia, Introduction to Embedded Systems, A Cyber-Physical Systems Approach, Second Edition, <http://LeeSeshia.org>, ISBN 978-1-312-42740-2, 2015.

### Answer

As per the question, we need to construct equivalent flat finite state machine giving the semantics of hierarchical state machine (as shown below which has the history transition) under the condition that the transition from state B to A is preemptive.



Hierarchical State Machine

Figure on the left hand side represents that flat finite state machine for above diagram with history transition and figure on the right hand side represents the hierarchical state machine with history transition under the condition that B to A is preemptive.

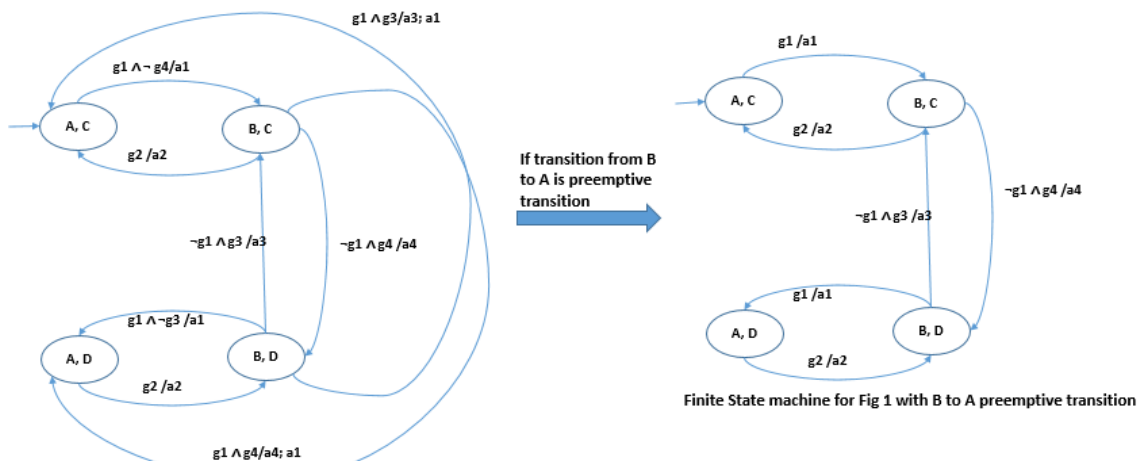


Fig 1: Hierarchical State machine with a history transition

Finite State machine for Fig 1 with B to A preemptive transition

Flat finite state machine

Name:

**Indian Institute of Technology Kanpur**  
**CS637 Embedded and Cyber-Physical Systems**

**Roll No**   
e.g. 170001

**Dept.**   
e.g. CSE

**Homework Assignment 2**  
*Deadline:* October 11, 2020

---

Name: Ajita Shree

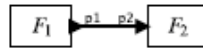
Indian Institute of Technology Kanpur  
CS637 Embedded and Cyber-Physical SystemsRoll No 20111262  
e.g. 170001Dept. Computer Science Engineering  
e.g. CSE

Homework Assignment 2

Deadline: October 11, 2020

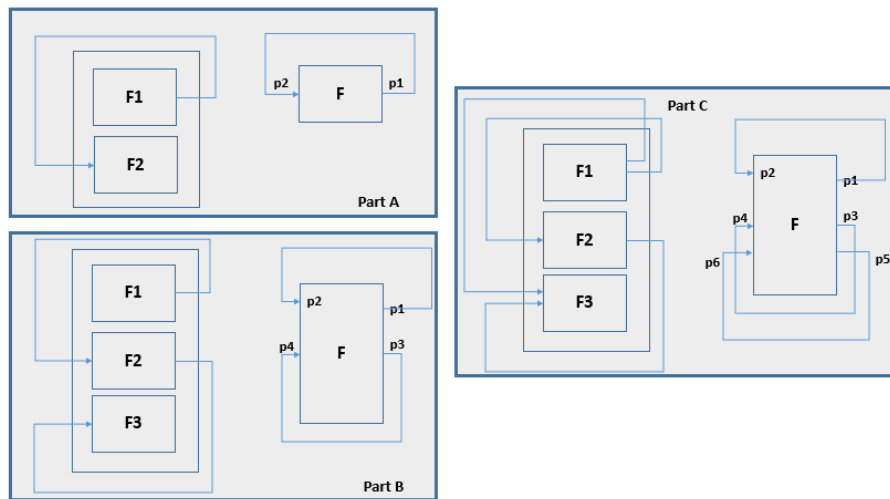
**Problem 3.** (10 points) Problem 1 in the Exercises of Chapter 6 in [LS15].[LS15] Edward A. Lee and Sanjit A. Seshia, Introduction to Embedded Systems, A Cyber-Physical Systems Approach, Second Edition, <http://LeeSeshia.org>, ISBN 978-1-312-42740-2, 2015.**Answer**

We need to create the transformation of the following actor models into the feedback system:



Actor models

Below diagram represents the feedback system representation for the above actor models (a, b, c in that order).



Feedback System

Name:

**Indian Institute of Technology Kanpur**  
**CS637 Embedded and Cyber-Physical Systems**

**Roll No**   
e.g. 170001

**Dept.**   
e.g. CSE

**Homework Assignment 2**  
*Deadline:* October 11, 2020

---

Name: Ajita Shree

Indian Institute of Technology Kanpur  
CS637 Embedded and Cyber-Physical SystemsRoll No 20111262  
e.g. 170001Dept. Computer Science Engineering  
e.g. CSE

Homework Assignment 2

Deadline: October 11, 2020

**Problem 4.** (10 points) Problem 8 in the Exercises of Chapter 6 in [LS15].[LS15] Edward A. Lee and Sanjit A. Seshia, Introduction to Embedded Systems, A Cyber-Physical Systems Approach, Second Edition, <http://LeeSeshia.org>, ISBN 978-1-312-42740-2, 2015.**Answer**Below is the SDF model where  $q_a$ ,  $q_b$ ,  $q_c$  denote the number of firing actors A, B and C respectively.

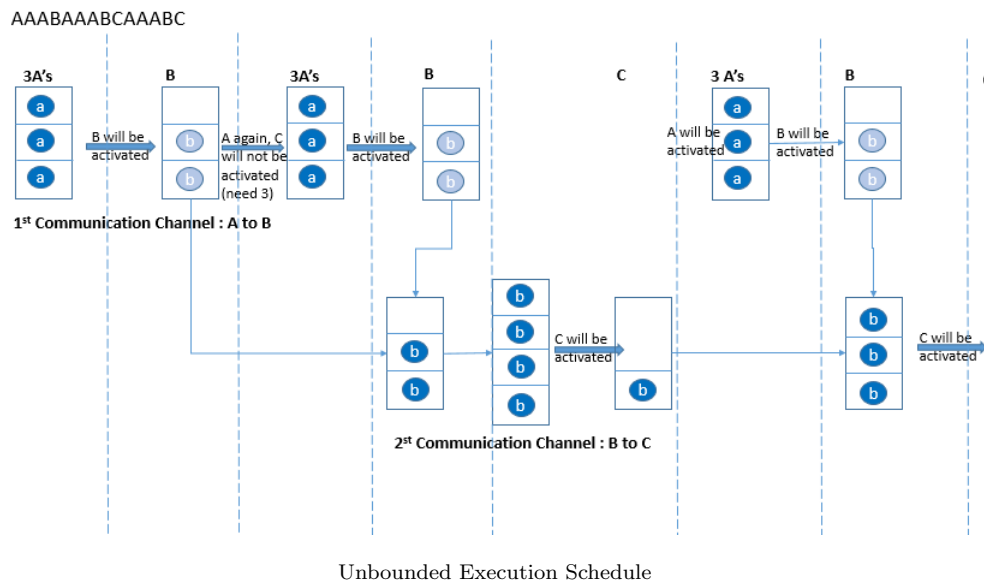
SDF Model

a) As per the above diagram, A produce 1 token at a time; B will be activated after receiving 3 tokens from A and will produce 2 tokens as output. Further, C will be activated after receiving 3 tokens from B. Hence, the equation will be the following form.

- **Balanced Equation:**  $q_a = 3q_b$  and  $2q_b = 3q_c$
- **Least positive integer solution:** If we multiply equation 1 with 2 and equation 2 by 3, we have  $2q_a = 6q_b$  and  $6q_b = 9q_c$  giving  $2q_a = 6q_b = 9q_c$ .  
Hence, the least integer that satisfies this is  $q_a = 9$ ,  $q_b = 3$ ,  $q_c = 2$

b) The Schedule for an unbounded execution that minimizes the buffer sizes on both the communication channels is **AAABAAABCAAABC**.

- The following diagram shows the sequence of steps.



- As shown in the above diagram, in the 1st communication channel from A  $\rightarrow$  B, the size of buffer needed is 3 while communicating channel from B  $\rightarrow$  C needs the buffer of size 4.

Name: Ajita Shree

**Indian Institute of Technology Kanpur**  
**CS637 Embedded and Cyber-Physical Systems**Roll No 20111262  
e.g. 170001Dept. Computer Science Engineering  
e.g. CSE**Homework Assignment 2**  
*Deadline:* October 11, 2020

---

BLANK SPACE: Any answers written here will be left ungraded.  
No exceptions.  
You may use this space for rough work.