Hdmi 2 USB

Generated by Doxygen 1.8.1

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Class Documentation

4.1 Behavioral Architecture Reference

Processes

- PROCESS_1(clkMain)
- PROCESS_2(stEppCur ,stEppNext ,ctlEppAstb ,ctlEppDstb ,ctlEppWr)
- PROCESS_3(clkMain ,ctlEppAwr)
- PROCESS_4(clkMain ,regEppAdr ,ctlEppDwr ,busEppIn)
- PROCESS_5(clkMain ,regEppAdr ,ctlEppDwr ,busEppIn)
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- PROCESS_7(clkMain ,regEppAdr ,ctlEppDwr ,busEppIn)
- PROCESS_8(clkMain ,regEppAdr ,ctlEppDwr ,busEppIn)
- PROCESS_9(clkMain ,regEppAdr ,ctlEppDwr ,busEppIn)
- PROCESS_10(clkMain ,regEppAdr ,ctlEppDwr ,busEppIn)
- PROCESS_11(clkMain ,regEppAdr ,ctlEppDwr ,busEppIn)
- PROCESS_12(clkMain ,regEppAdr ,ctlEppDwr ,busEppIn)

Constants

- stEppReady std_logic_vector(7 downto 0):=" 0000 "&" 0000 "
- stEppAwrA std_logic_vector(7 downto 0):=" 0001 "&" 0100 "
- stEppAwrB std_logic_vector(7 downto 0):=" 0010 "&" 0001 "
- stEppArdA std_logic_vector(7 downto 0):=" 0011 "&" 0010 "
- stEppArdB std_logic_vector(7 downto 0):=" 0100 "&" 0011 "
- stEppDwrA std_logic_vector(7 downto 0):=" 0101 "&" 1000 "
- stEppDwrB std_logic_vector(7 downto 0):=" 0110 "&" 0001 "
- stEppDrdA std_logic_vector(7 downto 0):=" 0111 "&" 0010 "
- stEppDrdB std_logic_vector(7 downto 0):=" 1000 "&" 0011 "

Signals

- stEppCur std_logic_vector(7 downto 0):=stEppReady
- stEppNext std_logic_vector(7 downto 0)
- clkMain std_logic
- ctlEppWait std_logic
- ctlEppAstb std_logic
- ctlEppDstb std_logic
- ctlEppDir std_logic

- ctlEppWr std_logic
- ctlEppAwr std_logic
- ctlEppDwr std_logic
- busEppOut std_logic_vector(7 downto 0)
- busEppIn std_logic_vector(7 downto 0)
- busEppData std_logic_vector(7 downto 0)
- regEppAdr std_logic_vector(3 downto 0)
- regData0 std_logic_vector(7 downto 0)
- regData1 std_logic_vector(7 downto 0)
- regData2 std_logic_vector(7 downto 0)
- regData3 std_logic_vector(7 downto 0)
- regData4 std_logic_vector(7 downto 0)
- regData5 std_logic_vector(7 downto 0)
- regData6 std_logic_vector(7 downto 0)
- regData7 std_logic_vector(7 downto 0)
- regLed std_logic_vector(7 downto 0)
- cntr std_logic_vector(7 downto 0)

4.1.1 Member Function Documentation

4.1.1.1 PROCESS_1(clkMain) [Process]

4.1.1.2 PROCESS_10(clkMain ,regEppAdr ,ctlEppDwr ,busEppIn) [Process]

4.1.1.3 PROCESS_11(clkMain ,regEppAdr ,ctlEppDwr ,busEppIn) [Process]

4.1.1.4 PROCESS_12(clkMain ,regEppAdr ,ctlEppDwr ,busEppIn) [Process]

4.1.1.5 PROCESS_2(stEppCur ,stEppNext ,ctlEppAstb ,ctlEppDstb ,ctlEppWr) [Process]

4.1.1.6 PROCESS_3(clkMain ,ctlEppAwr) [Process]

4.1.1.7 PROCESS_4(clkMain ,regEppAdr ,ctlEppDwr ,busEppIn) [Process]

4.1.1.8 PROCESS_5(clkMain ,regEppAdr ,ctlEppDwr ,busEppIn) [Process]

4.1.1.9 PROCESS_6(clkMain ,regEppAdr ,ctlEppDwr ,busEppIn) [Process]

4.1.1.10 PROCESS_7(clkMain ,regEppAdr ,ctlEppDwr ,busEppIn) [Process]

4.1.1.11 PROCESS_8(clkMain ,regEppAdr ,ctlEppDwr ,busEppIn) [Process]

4.1.1.12 PROCESS_9(clkMain ,regEppAdr ,ctlEppDwr ,busEppIn) [Process]

4.1.2 Member Data Documentation

4.1.2.1 busEppData std_logic_vector(7 downto 0) [Signal]

4.1.2.2 busEppIn std_logic_vector(7 downto 0) [Signal]

4.1.2.3 busEppOut std_logic_vector(7 downto 0) [Signal]

4.1.2.4 clkMain std_logic [Signal]

4.1.2.5 cntr std_logic_vector(7 downto 0) [Signal]

4.1.2.6 ctlEppAstb std_logic [Signal]

4.1.2.7 ctlEppAwr std_logic [Signal]

4.1.2.8 ctlEppDir std_logic [Signal]

4.1.2.9 ctlEppDstb std_logic [Signal]

4.1.2.10 ctlEppDwr std_logic [Signal]

4.1.2.11 ctlEppWait std_logic [Signal]

4.1.2.12 ctlEppWr std_logic [Signal]

4.1.2.13 regData0 std_logic_vector(7 downto 0) [Signal]

4.1.2.14 regData1 std_logic_vector(7 downto 0) [Signal]

4.1.2.15 regData2 std_logic_vector(7 downto 0) [Signal]

4.1.2.16 regData3 std_logic_vector(7 downto 0) [Signal]

4.1.2.17 regData4 std_logic_vector(7 downto 0) [Signal]

4.1.2.18 regData5 std_logic_vector(7 downto 0) [Signal]

4.1.2.19 regData6 std_logic_vector(7 downto 0) [Signal]

4.1.2.20 regData7 std_logic_vector(7 downto 0) [Signal]

4.1.2.21 regEppAdr std_logic_vector(3 downto 0) [Signal]

4.1.2.22 regLed std_logic_vector(7 downto 0) [Signal]

4.1.2.23 stEppArdA std_logic_vector(7 downto 0):=" 0011 "&" 0010 " [Constant]

4.1.2.24 stEppArdB std_logic_vector(7 downto 0):=" 0100 "&" 0011 " [Constant]

4.1.2.25 stEppAwrA std_logic_vector(7 downto 0):=" 0001 "&" 0100 " [Constant]

4.1.2.26 stEppAwrB std_logic_vector(7 downto 0):=" 0010 "&" 0001 " [Constant]

4.1.2.27 stEppCur std_logic_vector(7 downto 0):=stEppReady [Signal]

4.1.2.28 stEppDrdA std_logic_vector(7 downto 0):=" 0111 "&" 0010 " [Constant]

4.1.2.29 stEppDrdB std_logic_vector(7 downto 0):=" 1000 "&" 0011 " [Constant]

4.1.2.30 stEppDwrA std_logic_vector(7 downto 0):=" 0101 "&" 1000 " [Constant]

4.1.2.31 stEppDwrB std_logic_vector(7 downto 0):=" 0110 "&" 0001 " [Constant]

4.1.2.32 stEppNext std_logic_vector(7 downto 0) [Signal]

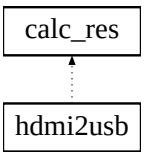
4.1.2.33 stEppReady std_logic_vector(7 downto 0):=" 0000 "&" 0000 " [Constant]

The documentation for this class was generated from the following file:

- **dpimref.vhd**

4.2 calc_res Enum Reference

Inheritance diagram for calc_res:



4.2.1 Detailed Description

This module calculates the resolution of the image being displayed so that we can use it in the header of jpeg encoder.

4.2.2 Member Function Documentation

4.2.2.1

4.2.3 Member Data Documentation

4.2.3.1 rst_n wire

4.2.3.2 pclk_q

4.2.3.3 vsync_q

4.2.3.4 hsync_q

4.2.3.5 de_q

4.2.3.6 pclk_risingedge

4.2.3.7 hsync_risingedge

4.2.3.8 vsync_risingedge

4.2.3.9 de_risingedge

4.2.3.10 clk wire

4.2.3.11 de

4.2.3.12 hsync

4.2.3.13 vsync

4.2.3.14 resX reg[15 : 0]

4.2.3.15 resY reg[15 : 0]

4.2.3.16 pclk

4.2.3.17 resX_q

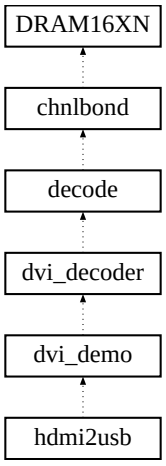
4.2.3.18 resY_q

The documentation for this enum was generated from the following file:

- **calc_res.v**

4.3 chnlbond Enum Reference

Inheritance diagram for chnlbond:



Additional Inherited Members

4.3.1 Member Function Documentation

4.3.1.1

4.3.1.2

4.3.1.3

4.3.1.4

4.3.1.5

4.3.1.6

4.3.1.7

4.3.1.8

4.3.1.9

4.3.2 Member Data Documentation

4.3.2.1 clk wire

4.3.2.2 rawdata wire[9 : 0]

4.3.2.3 iamvld wire

4.3.2.4 other_ch0_vld wire

4.3.2.5 other_ch1_vld wire

4.3.2.6 other_ch0_rdy wire

4.3.2.7 other_ch1_rdy wire

4.3.2.8 iamrdy reg

4.3.2.9 sdata reg[9 : 0]

4.3.2.10 CTRLTOKEN0

4.3.2.11 CTRLTOKEN1

4.3.2.12 CTRLTOKEN2

4.3.2.13 CTRLTOKEN3

4.3.2.14 rawdata_vld

4.3.2.15 wa

4.3.2.16 ra

4.3.2.17 we

4.3.2.18 dpfo_dout

4.3.2.19 rcvd_ctkn

4.3.2.20 rcvd_ctkn_q

4.3.2.21 blnkbgn

4.3.2.22 next_blnkbgn

4.3.2.23 skip_line

4.3.2.24 rawdata_vld_q

4.3.2.25 rawdata_vld_rising

4.3.2.26 ra_en

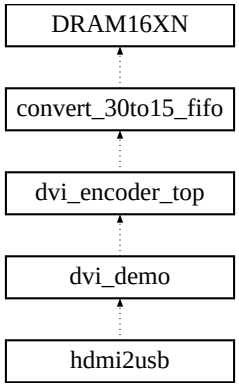
4.3.2.27 DRAM16XN cbfifo_i

The documentation for this enum was generated from the following file:

- **chnlbond.v**

4.4 convert_30to15_fifo Enum Reference

Inheritance diagram for convert_30to15_fifo:



Additional Inherited Members

4.4.1 Member Function Documentation

4.4.1.1

4.4.1.2

4.4.2 Member Data Documentation

4.4.2.1 rst wire

4.4.2.2 clk wire

4.4.2.3 clkx2 wire

4.4.2.4 datain wire[29 : 0]

4.4.2.5 dataout wire[14 : 0]

4.4.2.6 wa

4.4.2.7 wa_d

4.4.2.8 ra

4.4.2.9 ra_d

4.4.2.10 dataint

4.4.2.11 ADDR0

4.4.2.12 ADDR1

4.4.2.13 ADDR2

4.4.2.14 ADDR3

4.4.2.15 ADDR4

4.4.2.16 ADDR5

4.4.2.17 ADDR6

4.4.2.18 ADDR7

4.4.2.19 ADDR8

4.4.2.20 ADDR9

4.4.2.21 ADDR10

4.4.2.22 ADDR11

4.4.2.23 ADDR12

4.4.2.24 ADDR13

4.4.2.25 ADDR14

4.4.2.26 ADDR15

4.4.2.27 rstsync

4.4.2.28 rstsync_q

4.4.2.29 rstp

4.4.2.30 sync

4.4.2.31 db

4.4.2.32 mux

4.4.2.33 DRAM16XN fifo_u

4.4.2.34 FD fd_rstsync

4.4.2.35 FD fd_rstp

4.4.2.36 FD fd_out0

4.4.2.37 FD fd_out1

4.4.2.38 FD fd_out2

4.4.2.39 **FD fd_out3**

4.4.2.40 **FD fd_out4**

4.4.2.41 **FD fd_out5**

4.4.2.42 **FD fd_out6**

4.4.2.43 **FD fd_out7**

4.4.2.44 **FD fd_out8**

4.4.2.45 **FD fd_out9**

4.4.2.46 **FD fd_out10**

4.4.2.47 **FD fd_out11**

4.4.2.48 **FD fd_out12**

4.4.2.49 **FD fd_out13**

4.4.2.50 **FD fd_out14**

4.4.2.51 **FDC fdc_wa0**

4.4.2.52 **FDC fdc_wa1**

4.4.2.53 **FDC fdc_wa2**

4.4.2.54 **FDC fdc_wa3**

4.4.2.55 **FDE fd_db0**

4.4.2.56 **FDE fd_db1**

4.4.2.57 **FDE fd_db2**

4.4.2.58 **FDE fd_db3**

4.4.2.59 **FDE fd_db4**

4.4.2.60 **FDE fd_db5**

4.4.2.61 **FDE fd_db6**

4.4.2.62 **FDE fd_db7**

4.4.2.63 **FDE fd_db8**

4.4.2.64 **FDE fd_db9**

4.4.2.65 **FDE fd_db10**

4.4.2.66 **FDE fd_db11**

4.4.2.67 FDE fd_db12

4.4.2.68 FDE fd_db13

4.4.2.69 FDE fd_db14

4.4.2.70 FDE fd_db15

4.4.2.71 FDE fd_db16

4.4.2.72 FDE fd_db17

4.4.2.73 FDE fd_db18

4.4.2.74 FDE fd_db19

4.4.2.75 FDE fd_db20

4.4.2.76 FDE fd_db21

4.4.2.77 FDE fd_db22

4.4.2.78 FDE fd_db23

4.4.2.79 FDE fd_db24

4.4.2.80 FDE fd_db25

4.4.2.81 FDE fd_db26

4.4.2.82 FDE fd_db27

4.4.2.83 FDE fd_db28

4.4.2.84 FDE fd_db29

4.4.2.85 FDP fdp_rst

4.4.2.86 FDR sync_gen

4.4.2.87 FDRE fdc_ra0

4.4.2.88 FDRE fdc_ra1

4.4.2.89 FDRE fdc_ra2

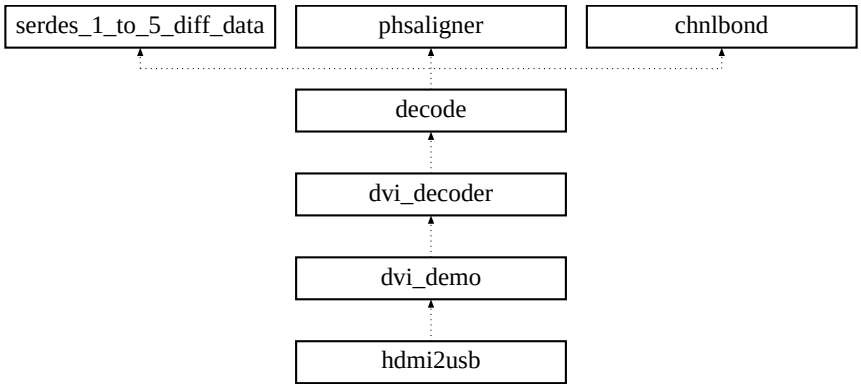
4.4.2.90 FDRE fdc_ra3

The documentation for this enum was generated from the following file:

- **convert_30to15_fifo.v**

4.5 decode Enum Reference

Inheritance diagram for decode:



Additional Inherited Members

4.5.1 Member Function Documentation

4.5.1.1

4.5.1.2

4.5.1.3

4.5.1.4

4.5.1.5

4.5.2 Member Data Documentation

4.5.2.1 reset wire

4.5.2.2 pclk wire

4.5.2.3 pclkx2 wire

4.5.2.4 pclkx10 wire

4.5.2.5 serdesstrobe wire

4.5.2.6 din_p wire

4.5.2.7 din_n wire

4.5.2.8 other_ch0_vld wire

4.5.2.9 other_ch1_vld wire

4.5.2.10 other_ch0_rdy wire

4.5.2.11 other_ch1_rdy wire

4.5.2.12 iamvld wire

4.5.2.13 iamrdy wire

4.5.2.14 psalgnerr wire

4.5.2.15 c0 reg

4.5.2.16 c1 reg

4.5.2.17 de reg

4.5.2.18 sdout reg[9 : 0]

4.5.2.19 dout reg[7 : 0]

4.5.2.20 flipgear

4.5.2.21 flipgearx2

4.5.2.22 toggle

4.5.2.23 rx_toggle

4.5.2.24 raw5bit

4.5.2.25 raw5bit_q

4.5.2.26 rawword

4.5.2.27 bitslipx2

4.5.2.28 bitslip_q

4.5.2.29 bitslip

4.5.2.30 rawdata

4.5.2.31 sdata

4.5.2.32 CTRLTOKEN0

4.5.2.33 CTRLTOKEN1

4.5.2.34 CTRLTOKEN2

4.5.2.35 CTRLTOKEN3

4.5.2.36 data

4.5.2.37 chnlbond cbnd

4.5.2.38 phsaligner phsalgn_0

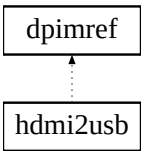
4.5.2.39 serdes_1_to_5_diff_data des_0

The documentation for this enum was generated from the following file:

- **decode.v**

4.6 dpimref Entity Reference

Inheritance diagram for dpimref:



Entities

- **Behavioral** architecture

Ports

- **mclk** **in** **std_logic**
- **pdb** **inout** **std_logic_vector**(7 **downto** 0)
- **astb** **in** **std_logic**
- **dstb** **in** **std_logic**
- **pwr** **in** **std_logic**
- **pwait** **out** **std_logic**
- **rgLed** **out** **std_logic_vector**(7 **downto** 0)
- **rgSwt** **in** **std_logic_vector**(7 **downto** 0)
- **rgBtn** **in** **std_logic_vector**(5 **downto** 0)
- **btn** **in** **std_logic**
- **ldg** **out** **std_logic**
- **led** **out** **std_logic**
- **resX** **in** **std_logic_vector**(15 **downto** 0)
- **resY** **in** **std_logic_vector**(15 **downto** 0)
- **rgb** **in** **std_logic_vector**(23 **downto** 0)

4.6.1 Member Data Documentation

4.6.1.1 astb in std_logic [Port]

4.6.1.2 btn in std_logic [Port]

4.6.1.3 dstb in std_logic [Port]

4.6.1.4 ldg out std_logic [Port]

4.6.1.5 led out std_logic [Port]

4.6.1.6 mclk in std_logic [Port]

4.6.1.7 pdb inout std_logic_vector(7 downto 0) [Port]

4.6.1.8 pwait out std_logic [Port]

4.6.1.9 pwr in std_logic [Port]

4.6.1.10 resX in std_logic_vector(15 downto 0) [Port]

4.6.1.11 resY in std_logic_vector(15 downto 0) [Port]

4.6.1.12 rgb in std_logic_vector(23 downto 0) [Port]

4.6.1.13 rgBtn in std_logic_vector(5 downto 0) [Port]

4.6.1.14 rgLed out std_logic_vector(7 downto 0) [Port]

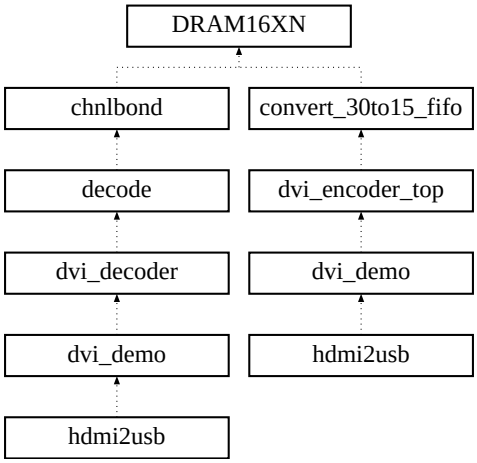
4.6.1.15 rgSwt in std_logic_vector(7 downto 0) [Port]

The documentation for this class was generated from the following file:

- **dpimref.vhd**

4.7 DRAM16XN Enum Reference

Inheritance diagram for DRAM16XN:



4.7.1 Member Data Documentation

4.7.1.1 data_width

4.7.1.2 DATA_IN [data_width - 1 : 0]

4.7.1.3 ADDRESS [3 : 0]

4.7.1.4 ADDRESS_DP [3 : 0]

4.7.1.5 WRITE_EN

4.7.1.6 CLK

4.7.1.7 O_DATA_OUT_DP [data_width - 1 : 0]

4.7.1.8 O_DATA_OUT [data_width - 1 : 0]

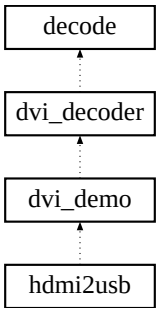
4.7.1.9 RAM16X1D i_RAM16X1D_U

The documentation for this enum was generated from the following file:

- **DRAM16XN.v**

4.8 dvi_decoder Enum Reference

Inheritance diagram for dvi_decoder:



Additional Inherited Members

4.8.1 Member Data Documentation

4.8.1.1 tmdsclk_p wire

4.8.1.2 tmdsclk_n wire

4.8.1.3 blue_p wire

4.8.1.4 green_p wire

4.8.1.5 red_p wire

4.8.1.6 blue_n wire

4.8.1.7 green_n wire

4.8.1.8 red_n wire

4.8.1.9 exrst wire

4.8.1.10 reset wire

4.8.1.11 pclk wire

4.8.1.12 pclkx2 wire

4.8.1.13 pclkx10 wire

4.8.1.14 pllclk0 wire

4.8.1.15 pllclk1 wire

4.8.1.16 pllclk2 wire

4.8.1.17 pll_lckd wire

4.8.1.18 serdesstrobe wire

4.8.1.19 tmdsclk wire

4.8.1.20 hsync wire

4.8.1.21 vsync wire

4.8.1.22 de wire

4.8.1.23 blue_vld wire

4.8.1.24 green_vld wire

4.8.1.25 red_vld wire

4.8.1.26 blue_rdy wire

4.8.1.27 green_rdy wire

4.8.1.28 red_rdy wire

4.8.1.29 psalgnerr wire

4.8.1.30 sdout wire[29 : 0]

4.8.1.31 red wire[7 : 0]

4.8.1.32 green wire[7 : 0]

4.8.1.33 blue wire[7 : 0]

4.8.1.34 sdout_blue

4.8.1.35 sdout_green

4.8.1.36 sdout_red

4.8.1.37 de_b

4.8.1.38 de_g

4.8.1.39 de_r

4.8.1.40 blue_psalgnerr

4.8.1.41 green_psalgnerr

4.8.1.42 red_psalgnerr

4.8.1.43 rxclkint

4.8.1.44 rxclk

4.8.1.45 bufpll_lock

4.8.1.46 BUFG tmdsclk_bufg

Reimplemented in **dvi_demo** (p. 26), and **dvi_demo** (p. 26).

4.8.1.47 BUFG pclkbufg

Reimplemented in **dvi_demo** (p. 26), and **dvi_demo** (p. 26).

4.8.1.48 BUFG pclkx2bufg

Reimplemented in **dvi_demo** (p. 26), and **dvi_demo** (p. 26).

4.8.1.49 BUFIO2 bufio_tmdsclk

4.8.1.50 BUFPLL ioclk_buf

Reimplemented in **dvi_demo** (p. 26).

4.8.1.51 decode dec_b

4.8.1.52 decode dec_g

4.8.1.53 decode dec_r

4.8.1.54 IBUFDS ibuf_rxclk

Reimplemented from **serdes_1_to_5_diff_data** (p. 42).

4.8.1.55 PLL_BASE PLL_ISERDES

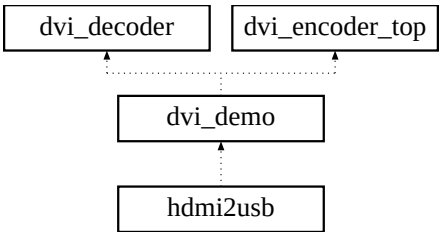
Reimplemented in **dvi_demo** (p. 26).

The documentation for this enum was generated from the following file:

- **dvi_decoder.v**

4.9 dvi_demo Enum Reference

Inheritance diagram for dvi_demo:



Additional Inherited Members

4.9.1 Member Data Documentation

4.9.1.1 rst_n wire

4.9.1.2 clk wire

4.9.1.3 RX0_TMDS wire[3 : 0]

4.9.1.4 RX0_TMDSB wire[3 : 0]

4.9.1.5 TX0_TMDS wire[3 : 0]

4.9.1.6 TX0_TMDSB wire[3 : 0]

4.9.1.7 rgb wire[23 : 0]

4.9.1.8 rgb_de wire

4.9.1.9 hsync wire

4.9.1.10 vsync wire

4.9.1.11 pclk wire

4.9.1.12 SW wire

4.9.1.13 LED wire[4 : 0]

4.9.1.14 clk10x wire

4.9.1.15 rx0_pclk

4.9.1.16 rx0_pclkx2

4.9.1.17 rx0_pclkx10

4.9.1.18 rx0_pllclk0

4.9.1.19 rx0_pllckd

4.9.1.20 rx0_reset

4.9.1.21 rx0_serdesstrobe

4.9.1.22 rx0_hsync

4.9.1.23 rx0_vsync

4.9.1.24 rx0_de

4.9.1.25 rx0_psalgnerr

4.9.1.26 rx0_red

4.9.1.27 rx0_green

4.9.1.28 rx0_blue

4.9.1.29 rx0_sdata

4.9.1.30 rx0_blue_vld

4.9.1.31 rx0_green_vld

4.9.1.32 rx0_red_vld

4.9.1.33 rx0_blue_rdy

4.9.1.34 rx0_green_rdy

4.9.1.35 rx0_red_rdy

4.9.1.36 Y

4.9.1.37 tx0_de

4.9.1.38 tx0_pclk

4.9.1.39 tx0_pclkx2

4.9.1.40 tx0_pclkx10

4.9.1.41 tx0_serdesstrobe

4.9.1.42 tx0_reset

4.9.1.43 tx0_blue

4.9.1.44 tx0_green

4.9.1.45 tx0_red

4.9.1.46 tx0_hsync

4.9.1.47 tx0_vsync

4.9.1.48 tx0_pll_reset

4.9.1.49 tx0_clkfbout

4.9.1.50 tx0_clkfbin

4.9.1.51 tx0_plllckd

4.9.1.52 tx0_pllclk0

4.9.1.53 tx0_pllclk2

4.9.1.54 tx0_bufpll_lock

4.9.1.55 BUFG tx0_clkfb_buf

Reimplemented from **dvi_decoder** (p. 23).

4.9.1.56 BUFG tx0_pclkx2_buf

Reimplemented from **dvi_decoder** (p. 23).

4.9.1.57 BUFGMUX tx0_bufg_pclk

4.9.1.58 BUFPLL tx0_ioclk_buf

Reimplemented from **dvi_decoder** (p. 23).

4.9.1.59 dvi_decoder dvi_rx0

4.9.1.60 dvi_encoder_top dvi_tx0

4.9.1.61 PLL_BASE PLL_OSERDES_0

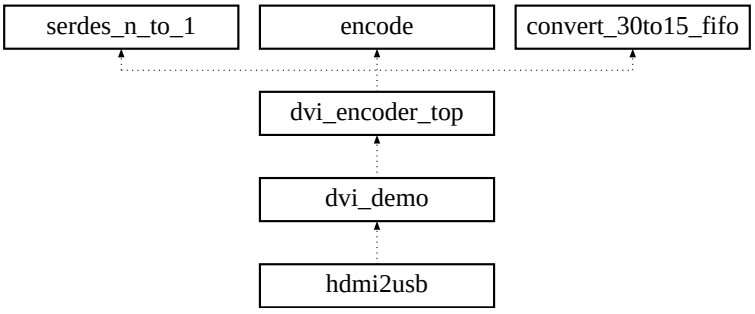
Reimplemented from **dvi_decoder** (p. 23).

The documentation for this enum was generated from the following file:

- **dvi_demo.v**

4.10 dvi_encoder_top Enum Reference

Inheritance diagram for dvi_encoder_top:



Additional Inherited Members

4.10.1 Member Function Documentation

4.10.1.1

4.10.1.2

4.10.2 Member Data Documentation

4.10.2.1 pclk wire

4.10.2.2 pclkx2 wire

4.10.2.3 pclkx10 wire

4.10.2.4 serdesstrobe wire

4.10.2.5 rstin wire

4.10.2.6 blue_din wire[7 : 0]

4.10.2.7 green_din wire[7 : 0]

4.10.2.8 red_din wire[7 : 0]

4.10.2.9 hsync wire

4.10.2.10 vsync wire

4.10.2.11 de wire

4.10.2.12 TMDS wire[3 : 0]

4.10.2.13 TMDSB wire[3 : 0]

4.10.2.14 red

4.10.2.15 green

4.10.2.16 blue

4.10.2.17 tmds_data0

4.10.2.18 tmds_data1

4.10.2.19 tmds_data2

4.10.2.20 tmdsint

4.10.2.21 tmdsclkint

4.10.2.22 toggle

4.10.2.23 tmdsclk

4.10.2.24 s_data

4.10.2.25 convert_30to15_fifo pixel2x

4.10.2.26 encode encb

4.10.2.27 encode encg

4.10.2.28 encode encr

4.10.2.29 OBUFDS TMDS3

4.10.2.30 OBUFDS TMDS0

4.10.2.31 OBUFDS TMDS1

4.10.2.32 OBUFDS TMDS2

4.10.2.33 serdes_n_to_1 clkout

4.10.2.34 serdes_n_to_1 oserdes0

4.10.2.35 serdes_n_to_1 oserdes1

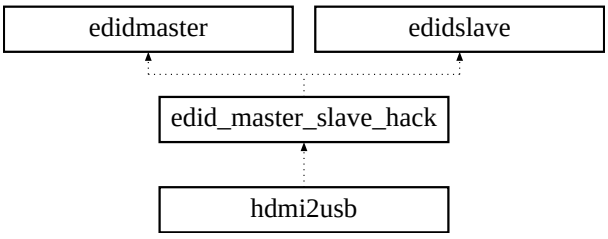
4.10.2.36 serdes_n_to_1 oserdes2

The documentation for this enum was generated from the following file:

- **dvi_encoder_top.v**

4.11 edid_master_slave_hack Enum Reference

Inheritance diagram for edid_master_slave_hack:



Additional Inherited Members

4.11.1 Detailed Description

This module handles the communication of EDID structure with PC and monitor/projector. It contains two sub-modules and one sequaltial logic block. The sequaltial logic block reads the EDID from montor when it detects the HPD from monitor by using edidmaster block. at the same time it pulls the HPD connected with PC HDMI to down, simulating the HDP disconnect. Then PC initiates the i2c communication with FPGA using edidslave block and reads the EDID structure.

4.11.2 Member Function Documentation

4.11.2.1

//% start reading from lcd on the rising edge of hpd

4.11.3 Member Data Documentation

4.11.3.1 rst_n

4.11.3.2 clk

4.11.3.3 sda_lcd

4.11.3.4 scl_lcd

4.11.3.5 sda_pc

4.11.3.6 scl_pc

4.11.3.7 hpd_lcd

4.11.3.8 hpd_pc reg

4.11.3.9 stop

4.11.3.10 dvi_only

4.11.3.11 edid_byte_lcd

4.11.3.12 counter

4.11.3.13 segments

4.11.3.14 segment_count

4.11.3.15 debounce_hpd

4.11.3.16 hpda_stable

4.11.3.17 hpda_stable_q

4.11.3.18 start_reading

4.11.3.19 edid_byte_lcd_en

4.11.3.20 edidmaster edid_master

//% debounce hpd_lcd

//% assuming only edid segment and then will be updated after //% edid segment //% only dvi resolution so dont read further. //% edid extensions //% only dvi resolution so dont read further. //% hdmi detected //% EDID master module for reading edid from LCD

4.11.3.21 edidslave edid_slave

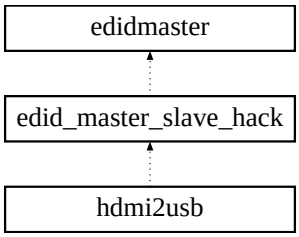
//% EDID slave for transmiting EDID to PC

The documentation for this enum was generated from the following file:

- **edid_master_slave_hack.v**

4.12 edidmaster Enum Reference

Inheritance diagram for edidmaster:



4.12.1 Detailed Description

EDID master for reading edid structure from monitor. the output is in byte format in "sdadata" on the rising edge of out_en

4.12.2 Member Function Documentation

4.12.2.1

4.12.3 Member Data Documentation

4.12.3.1 clk

4.12.3.2 stop_reading

4.12.3.3 rst_n

4.12.3.4 scl reg

4.12.3.5 sda

4.12.3.6 start

4.12.3.7 address_w [7 : 0]

4.12.3.8 address_r [7 : 0]

4.12.3.9 reg0 [7 : 0]

4.12.3.10 sdadata reg[7 : 0]

4.12.3.11 out_en reg

4.12.3.12 sdain

4.12.3.13 sdaout

4.12.3.14 INI

//% state machine states

4.12.3.15 WAIT_FOR_START

4.12.3.16 GEN_START

4.12.3.17 WRITE_BYTE_ADD_W

4.12.3.18 FREE_SDA_ADD_W

4.12.3.19 WAIT_WRITE_BYTE_ACK_ADD

4.12.3.20 WRITE_BYTE_REG

4.12.3.21 FREE_SDA_REG

4.12.3.22 WAIT_WRITE_BYTE_ACK_REG

4.12.3.23 WRITE_BYTE_ADD_R

4.12.3.24 FREE_SDA_ADD_R

4.12.3.25 WAIT_WRITE_BYTE_ACK_ADD_R

4.12.3.26 READ_DATA

4.12.3.27 SEND_READ_ACK

4.12.3.28 RELESASE_ACK

4.12.3.29 GEN_START2

4.12.3.30 SKIP1

4.12.3.31 state

4.12.3.32 scl_counter

4.12.3.33 scl_q

4.12.3.34 middle_scl

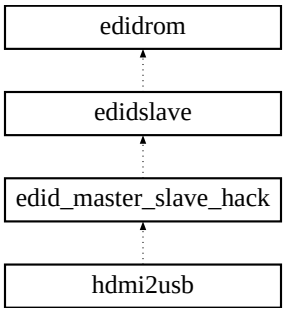
4.12.3.35 bitcount

The documentation for this enum was generated from the following file:

- **edidmaster.v**

4.13 edidrom Enum Reference

Inheritance diagram for edidrom:



4.13.1 Detailed Description

ROM for EDID DVI structure only, not for HDMI.

4.13.2 Member Function Documentation

4.13.2.1

4.13.3 Member Data Documentation

4.13.3.1 clk

4.13.3.2 adr [7 : 0]

4.13.3.3 data [7 : 0]

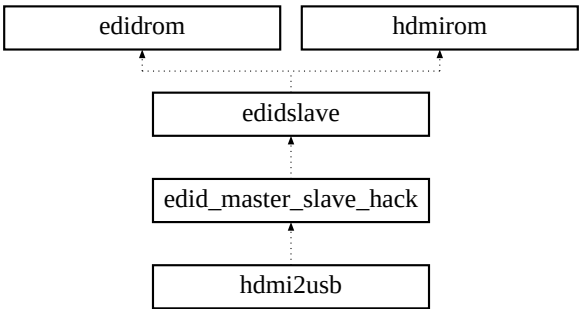
4.13.3.4 data

The documentation for this enum was generated from the following file:

- **edidrom.v**

4.14 edidslave Enum Reference

Inheritance diagram for edidslave:



Additional Inherited Members

4.14.1 Detailed Description

EDID Slave for communication with PC. dvi_only signal will select which rom to send to pc depending on the monitor connected. if no monitor is connected only dvi rom is transmitted.

4.14.2 Member Function Documentation

4.14.2.1

4.14.3 Member Data Documentation

4.14.3.1 RELEASE_SEND_ADDRESS_ACK_AGAIN

4.14.3.2 state

4.14.3.3 scl_risingedge

4.14.3.4 scl_fallingedge

4.14.3.5 start

4.14.3.6 stop

4.14.3.7 bitcount

4.14.3.8 sdadata

address confirmations is not implemeted yet // need to think about it in future. // before sending ack check the address

4.14.3.9 scl_debounce

4.14.3.10 scl_stable

4.14.3.11 sdain_q

4.14.3.12 scl_q

4.14.3.13 clk

4.14.3.14 rst_n

4.14.3.15 scl

4.14.3.16 sda

4.14.3.17 dvi_only

4.14.3.18 adr

4.14.3.19 data

4.14.3.20 data_hdmi

4.14.3.21 sdain

4.14.3.22 sdaout

4.14.3.23 INI

4.14.3.24 WAIT_FOR_START

4.14.3.25 READ_ADDRESS

4.14.3.26 SEND_ADDRESS_ACK

4.14.3.27 READ_REGISTER_ADDRESS

4.14.3.28 SEND_REGISTER_ADDRESS_ACK

4.14.3.29 WAIT_FOR_START_AGAIN

4.14.3.30 READ_ADDRESS_AGAIN

4.14.3.31 SEND_ADDRESS_ACK_AGAIN

4.14.3.32 WRITE_BYTE

4.14.3.33 FREE_SDA

4.14.3.34 WAIT_WRITE_BYTE_ACK

4.14.3.35 RELEASE_SEND_REGISTER_ADDRESS_ACK

4.14.3.36 RELESASE_ADDRESS_ACK

4.14.3.37 edidrom edid_rom

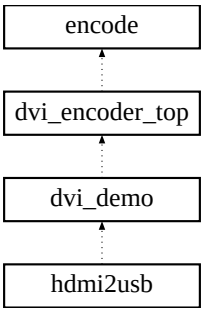
4.14.3.38 hdmirom hdmi_rom

The documentation for this enum was generated from the following file:

- **edidslave.v**

4.15 encode Enum Reference

Inheritance diagram for encode:



4.15.1 Member Function Documentation

4.15.1.1

4.15.1.2

4.15.1.3

4.15.1.4

4.15.2 Member Data Documentation

4.15.2.1 clkin

4.15.2.2 rstin

4.15.2.3 din [7 : 0]

4.15.2.4 c0

4.15.2.5 c1

4.15.2.6 de

4.15.2.7 dout reg[9 : 0]

4.15.2.8 n1d

4.15.2.9 din_q

4.15.2.10 decision1

4.15.2.11 q_m

4.15.2.12 n1q_m

4.15.2.13 n0q_m

4.15.2.14 CTRLTOKEN0

4.15.2.15 CTRLTOKEN1

4.15.2.16 CTRLTOKEN2

4.15.2.17 CTRLTOKEN3

4.15.2.18 cnt

4.15.2.19 decision2

4.15.2.20 decision3

4.15.2.21 de_q

4.15.2.22 de_reg

4.15.2.23 c0_q

4.15.2.24 c1_q

4.15.2.25 c0_reg

4.15.2.26 c1_reg

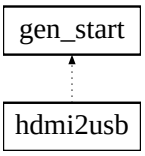
4.15.2.27 q_m_reg

The documentation for this enum was generated from the following file:

- **encode.v**

4.16 gen_start Enum Reference

Inheritance diagram for gen_start:



4.16.1 Detailed Description

This module calculates the resolution of the image being displayed so that we can use it in the header of jpeg encoder.

4.16.2 Member Function Documentation

4.16.2.1

4.16.3 Member Data Documentation

4.16.3.1 rst_n wire

4.16.3.2 clk wire

4.16.3.3 de

4.16.3.4 hsync

4.16.3.5 vsync

4.16.3.6 pclk

4.16.3.7 rgb [23 : 0]

4.16.3.8 rgb0 reg[23 : 0]

4.16.3.9 start reg

4.16.3.10 pclk_q

4.16.3.11 vsync_q

4.16.3.12 hsync_q

4.16.3.13 de_q

4.16.3.14 pclk_risingedge

4.16.3.15 hsync_risingedge

4.16.3.16 vsync_risingedge

4.16.3.17 de_risingedge

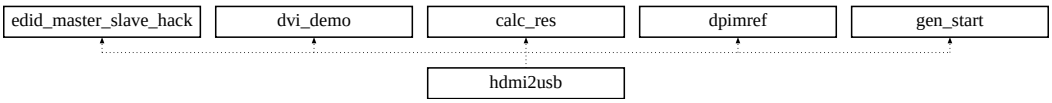
4.16.3.18 vsync_detected

The documentation for this enum was generated from the following file:

- **gen_start.v**

4.17 hdmi2usb Enum Reference

Inheritance diagram for hdmi2usb:



Additional Inherited Members

4.17.1 Detailed Description

HDMI rom for storing edid structure. This structure has one extenstion block contains the HDMI resolutions.

4.17.2 Member Function Documentation

4.17.2.1

4.17.3 Member Data Documentation

4.17.3.1 clk

4.17.3.2 adr [7 : 0]

4.17.3.3 data [7 : 0]

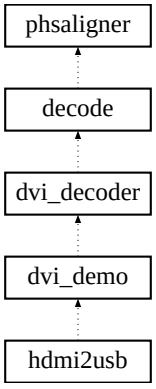
4.17.3.4 data

The documentation for this enum was generated from the following file:

- **hdmirom.v**

4.18 phsaligner Enum Reference

Inheritance diagram for phsaligner:



4.18.1 Member Function Documentation

4.18.1.1

4.18.1.2

4.18.1.3

4.18.1.4

4.18.1.5

4.18.1.6

4.18.1.7

4.18.1.8

4.18.1.9

4.18.2 Member Data Documentation

4.18.2.1 OPENEYE_CNT_WD

4.18.2.2 CTKNCNTWD

4.18.2.3 SRCHTIMERWD

4.18.2.4 rst wire

4.18.2.5 clk wire

4.18.2.6 sdata wire[9 : 0]

4.18.2.7 flipgear reg

4.18.2.8 bitslip reg

4.18.2.9 psaligned reg

4.18.2.10 CTRLTOKEN0

4.18.2.11 CTRLTOKEN1

4.18.2.12 CTRLTOKEN2

4.18.2.13 CTRLTOKEN3

4.18.2.14 rcvd_ctkn

4.18.2.15 rcvd_ctkn_q

4.18.2.16 blnkbgn

4.18.2.17 ctkn_srh_timer

4.18.2.18 ctkn_srh_rst

4.18.2.19 ctkn_srh_tout

4.18.2.20 ctkn_counter

4.18.2.21 ctkn_cnt_rst

4.18.2.22 ctkn_cnt_tout

4.18.2.23 INIT

4.18.2.24 SEARCH

4.18.2.25 BITSLIP

4.18.2.26 RCVDCTKN

4.18.2.27 BLNKPRD

4.18.2.28 PSALGND

4.18.2.29 nSTATES

4.18.2.30 cstate

4.18.2.31 nstate

4.18.2.32 state_ascii

4.18.2.33 BLNKPRD_CNT_WD

4.18.2.34 blnkprd_cnt

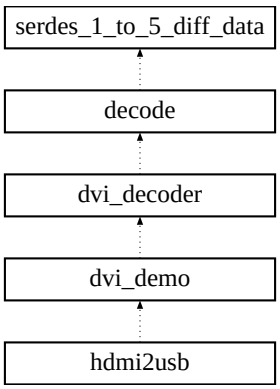
4.18.2.35 bitslip_cnt

The documentation for this enum was generated from the following file:

- **phsaligner.v**

4.19 serdes_1_to_5_diff_data Enum Reference

Inheritance diagram for serdes_1_to_5_diff_data:



4.19.1 Member Function Documentation

4.19.1.1

4.19.1.2

4.19.1.3

4.19.2 Member Data Documentation

4.19.2.1 DIFF_TERM

4.19.2.2 SIM_TAP_DELAY

4.19.2.3 BITSLIP_ENABLE

4.19.2.4 use_phase_detector wire

4.19.2.5 datain_p wire

4.19.2.6 datain_n wire

4.19.2.7 rxioclk wire

4.19.2.8 rxserdesstrobe wire

4.19.2.9 reset wire

4.19.2.10 gclk wire

4.19.2.11 bitslip wire

4.19.2.12 data_out wire[4 : 0]

4.19.2.13 ddly_m

4.19.2.14 ddly_s

4.19.2.15 busys

4.19.2.16 rx_data_in

4.19.2.17 cascade

4.19.2.18 pd_edge

4.19.2.19 counter

4.19.2.20 state

4.19.2.21 cal_data_sint

4.19.2.22 busy_data

4.19.2.23 busy_data_d

4.19.2.24 cal_data_slave

4.19.2.25 enable

4.19.2.26 cal_data_master

4.19.2.27 rst_data

4.19.2.28 inc_data_int

4.19.2.29 inc_data

4.19.2.30 ce_data

4.19.2.31 valid_data_d

4.19.2.32 incdec_data_d

4.19.2.33 pdcounter

4.19.2.34 valid_data

4.19.2.35 incdec_data

4.19.2.36 flag

4.19.2.37 mux

4.19.2.38 ce_data_inta

4.19.2.39 incdec_data_or

4.19.2.40 incdec_data_im

4.19.2.41 valid_data_or

4.19.2.42 valid_data_im

4.19.2.43 busy_data_or

4.19.2.44 all_ce

4.19.2.45 debug_in

4.19.2.46 rxpdcntr

4.19.2.47 IBUFDS data_in

Reimplemented in **dvi_decoder** (p. 23).

4.19.2.48 IODELAY2 iodelay_m

4.19.2.49 IODELAY2 iodelay_s

4.19.2.50 ISERDES2 erdes_m

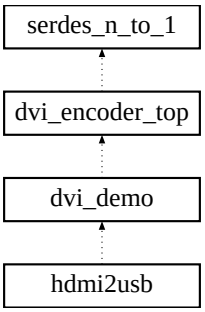
4.19.2.51 ISERDES2 erdes_s

The documentation for this enum was generated from the following file:

- **serdes_1_to_5_diff_data.v**

4.20 serdes_n_to_1 Enum Reference

Inheritance diagram for serdes_n_to_1:



4.20.1 Member Data Documentation

4.20.1.1 SF integer

4.20.1.2 ioclk

4.20.1.3 serdesstrobe

4.20.1.4 reset

4.20.1.5 gclk

4.20.1.6 datain [SF - 1 : 0]

4.20.1.7 iob_data_out

4.20.1.8 cascade_di

4.20.1.9 cascade_do

4.20.1.10 cascade_ti

4.20.1.11 cascade_to

4.20.1.12 mdatain

4.20.1.13 OSERDES2 oserdes_m

4.20.1.14 OSERDES2 oserdes_s

The documentation for this enum was generated from the following file:

- **serdes_n_to_1.v**

Chapter 5

File Documentation

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